MX•COM, INC. MiXed Signal ICs

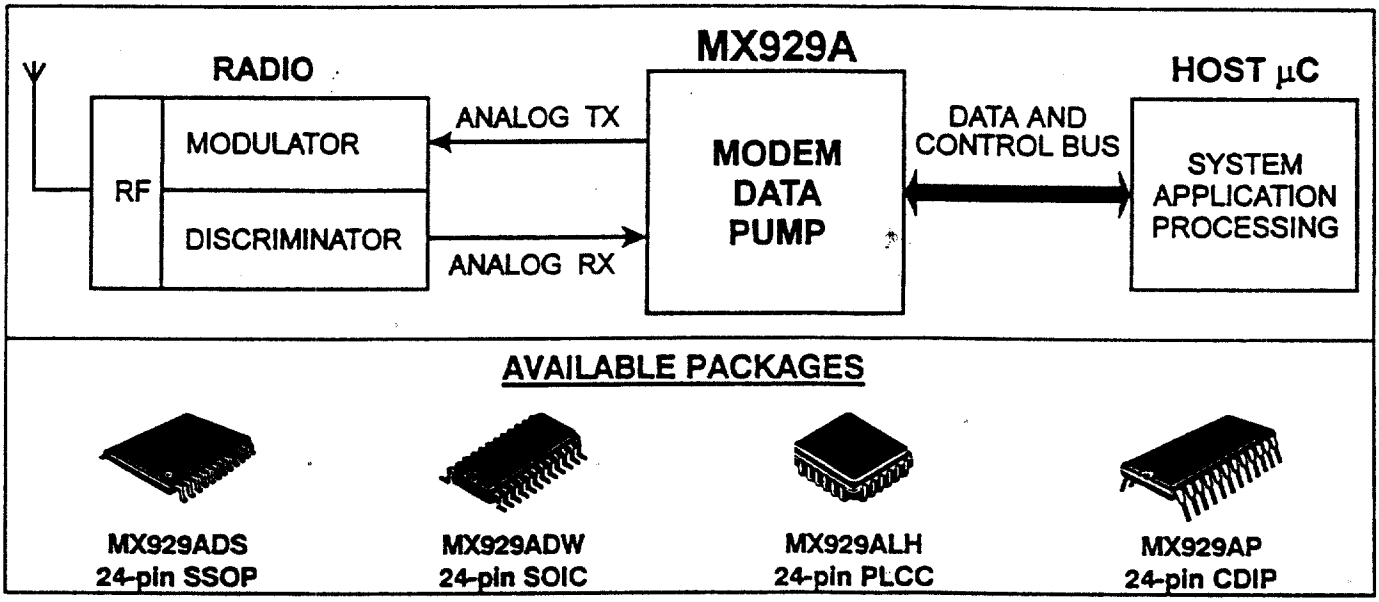
DATA BULLETIN

MX929A 4-Level FSK Modem Data Pump

Document # 20480149.001 MAY 1996

Advanced Information

- 4-Level FSK Modulation
- Half Duplex, 4800 to 19.2k bits/sec
- Full Data Packet Framing
- RD-LAP™ Compatible
- Flexible Operating Modes
- Host µC Interface
- Low Power 3.3V/5.0V Operation
- 24-Pin Small Form Package Option



The MX929A is a low voltage CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host µC and the radio modulation/demodulation circuits to deliver reliable two-way transfer of application data over a wireless link.

The MX929A assembles application data received from the host µC, adds forward error correction (FEC) and error detection (CRC) information and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-level analog signals for modulating into the radio transmitter.

In receive mode, the MX929A performs the reverse function using the analog signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the µC. CRC detected residual uncorrected data errors will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The MX929A uses data block sizes and FEC/CRC algorithms compatible with the RD-LAP™ over-air standard. The format used is suitable for other private applications where the high-speed transfer of data over narrow-band wireless links is required. The device is programmable to operate at standard bit-rates from a wide choice of Xtal/Clock frequencies.

CNSMS019

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1. Block Diagram

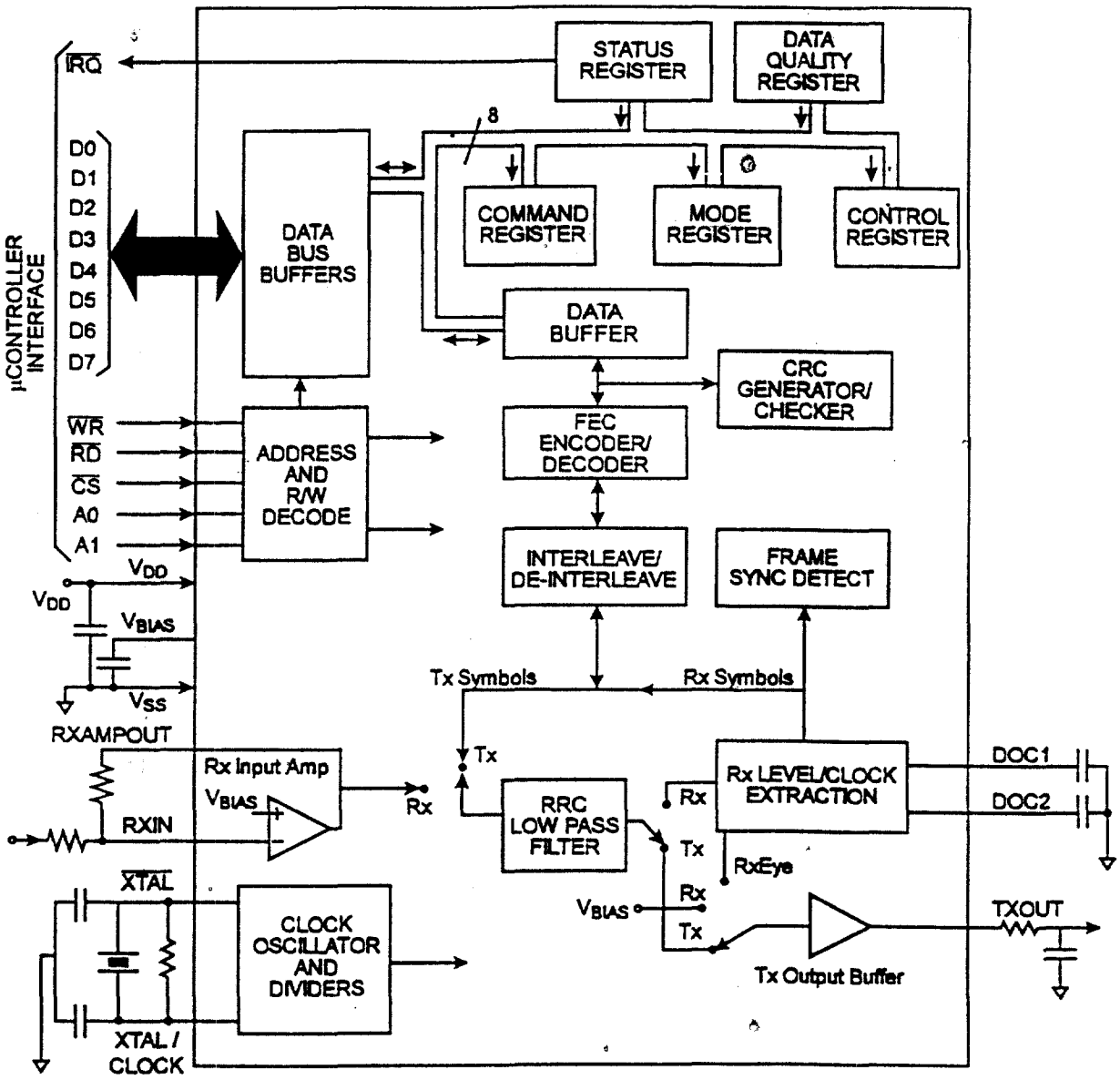

Figure 1: Block Diagram

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7-D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	Power	Negative supply. (ground).
13	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem. It is used to enable a data read or write operation.
14	A0	input	Logic level modem register select input
15	A1	input	Logic level modem register select input
16	$\overline{XTAL}$	output	The output of the on-chip oscillator.
17	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
18	DOC 2	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
19	DOC 1	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
20	TXOUT	output	Tx signal output from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	Output of the Rx input amplifier
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

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3. External Components

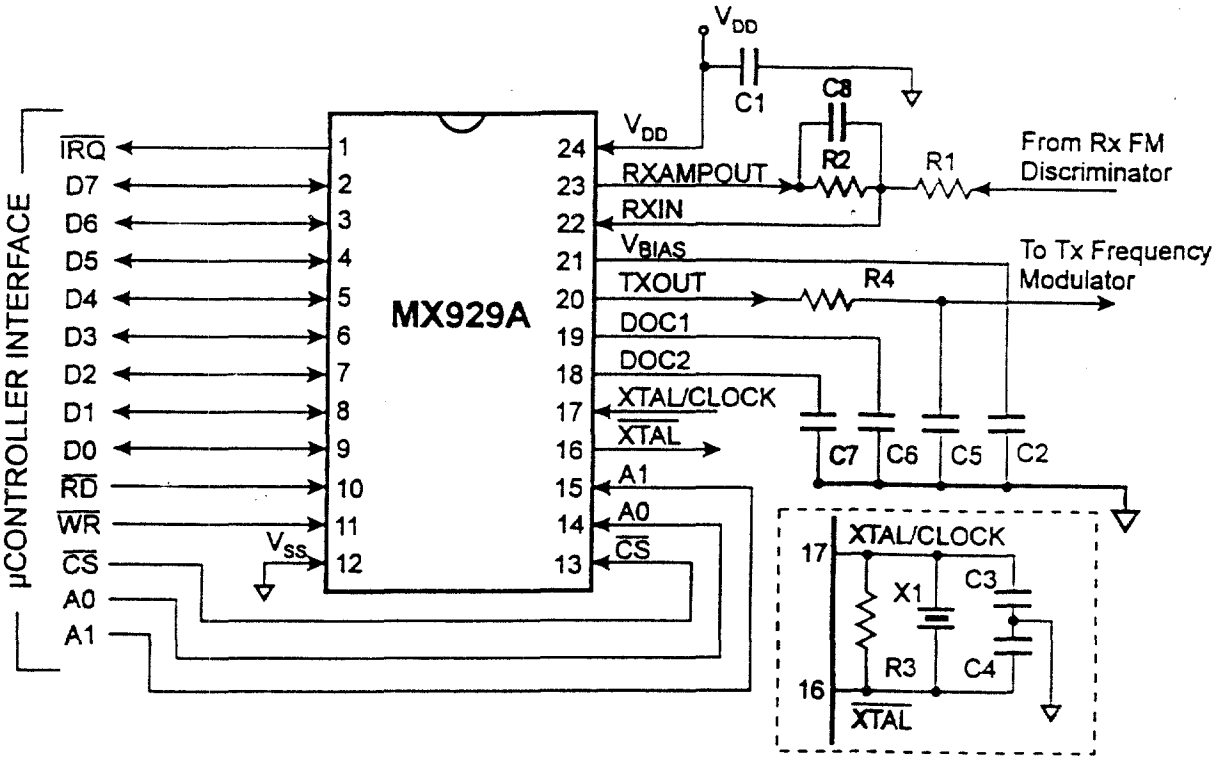


Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		
R2		100kΩ	± 5%
R3		1MΩ	± 20%
R4		100kΩ	± 5%
C1		0.1 µF	± 20%
C2		0.1 µF	± 20%
C3	2		± 20%
C4	2		± 20%
C5	3		± 5%
C6	4		± 20%
C7	4		± 20%
C8	3		± 5%
X1	2, 5		

Recommended External Components Notes

1. See section 4.1.10

2. The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitance) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. For optimum performance the crystal frequency should be ± 10ppm or better to allow use of the Narrow Bandwidth PLL setting (see section 4.5.3). Tolerances as wide as ± 50ppm may be used, but at the cost of a slightly reduced BER performance.

3. Values C5 and C8 should be equal to 750000 ÷ symbol rate, e.g.

Symbol Rate	C5/C8
2400 symbols/second	330pF
4800 symbols/second	150pF
9600 symbols/second	82pF

4. Values C6 and C7 should be equal to 50000 ÷ symbol rate, e.g.

Symbol Rate	C6/C7
2400 symbols/second	0.022µF
4800 symbols/second	0.01µF
9600 symbols/second	4700pF

5. See section 4.5.3

4. General Description

4.1 Description of Blocks

4.1.1 Data Bus Buffers

Eight bi-directional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input ($\overline{CS}$) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

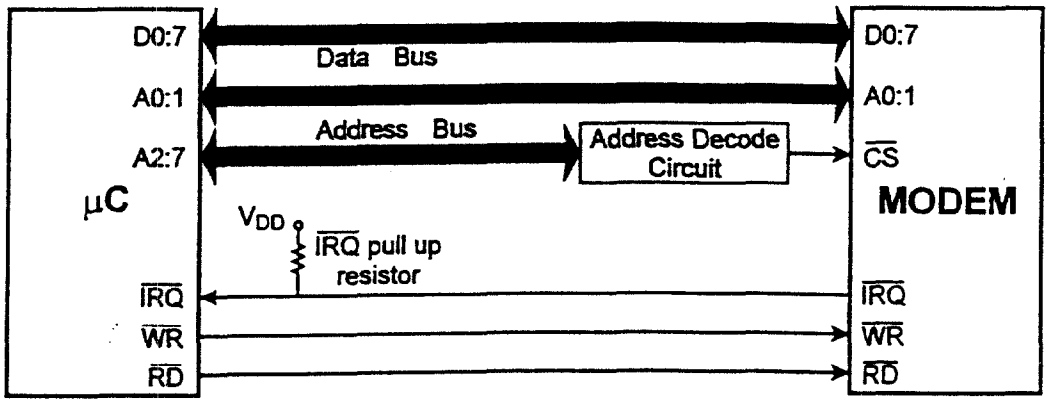


Figure 3: Typical Modem µC Connections

4.1.3 Status and Data Quality Registers

Two 8-bit registers which the µC can read to determine the status of the modem and the received data quality.

4.1.4 Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

4.1.5 Data Buffer

A 12-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in transmitted data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, resulting in the conversion of binary data to 4-level symbols. In receive mode, this circuit translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

4.1.8 Interleave/De-interleave Buffer

This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so the FEC system is best able to handle short noise bursts or fades.

4.1.9 Frame Sync Detect

This circuit, only active in receive mode, is used to look for a 24-symbol Frame Synchronization pattern that is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give $(0.2 \times V_{DD})V_{P-P}$ at the RXAMPOUT pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be placed in series with R1 if ac coupling of the received signal is desired (see section 5.4), otherwise the dc level of the received signal should be adjusted so the signal at the modem's RXAMPOUT is centered around V_{BIAS} ($V_{DD}/2$).

4.1.11 RRC Low Pass Filter

This filter, used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

$$
\begin{aligned}
H(f) \quad &= 1 && \text{for } 0 && \le f < (1-b)/(2T) \\
&= \text{square root of } \{0.5\,[1 - \sin(\pi\, T\, (f - 0.5/T)/b)]\} && \text{for } (1-b)/(2T) && \le f \le (1+b)/(2T) \\
&= 0 && \text{for } (1+b)/(2T) && < f
\end{aligned}
$$

where b = 0.2, T = 1/symbol rate

This frequency response is illustrated in Figure 5

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In receive mode, the filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols.

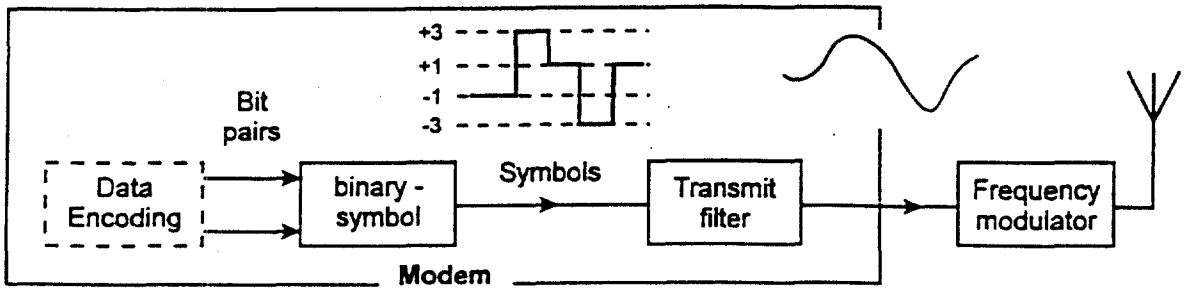


Figure 4: Translation of Binary Data to Filtered 4-Level Symbols in TX Mode

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in the transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS} unless the RXEYE bit of the Control Register is '1', when it is connected to the received signal. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOUT pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitance, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOUT pin is centered around V_{BIAS} and is approx. $(0.2 \times V_{DD})V_{P-P}$ for a continuous '+3 +3 -3 -3 ...' pattern.

A capacitor may be placed in series with the input to the frequency modulator if ac coupling is desired, see section 5.4

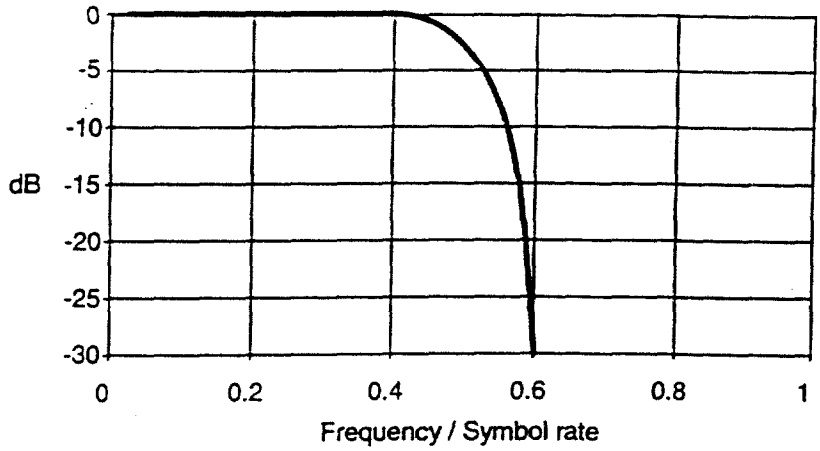


Figure 5: RRC Filter Frequency Response (including the external RC filter R4/C5)

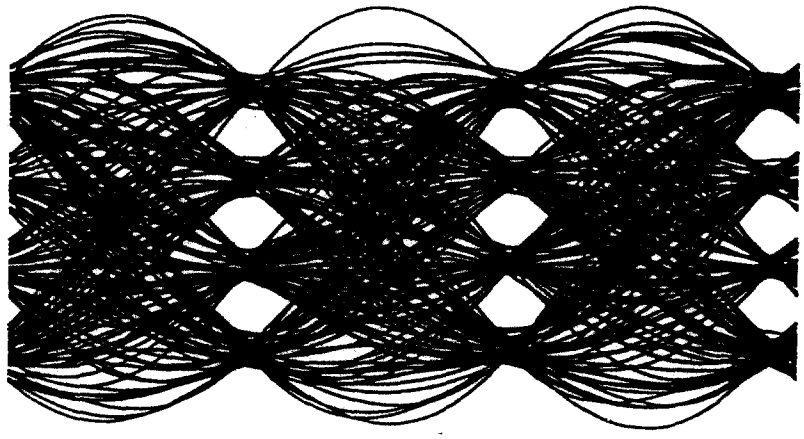


Figure 6: Transmitted Signal Eye Diagram

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

4.1.14 Clock Oscillator and Dividers

These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{XTAL}$ pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

4.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message formats handled by the modem are provided in section 4.3 and Figure 7 and Figure 8.

To reduce the processing load on the associated µC, the MX929A modem has been designed to perform much of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronizing onto the Frame Preamble. In normal operation the modem will only require servicing by the µC once per received or transmitted block.

To transmit a block, the controlling µC only needs to load the - unformatted - 'raw' binary data into the modem's Data Block Buffer, then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding), and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary - using the FEC coding to correct as many errors as possible - and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data for example: to allow for the transmission of Symbol and Frame Synchronization sequences or special test patterns.

4.3 Binary to Symbol Translation

Although the over-air signal, and the signals at the modem TXOUT and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

1. Direct (simplest form) - converts between 2 binary bits and a single symbol, such as the 'S' Channel Status symbol.

symbol	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

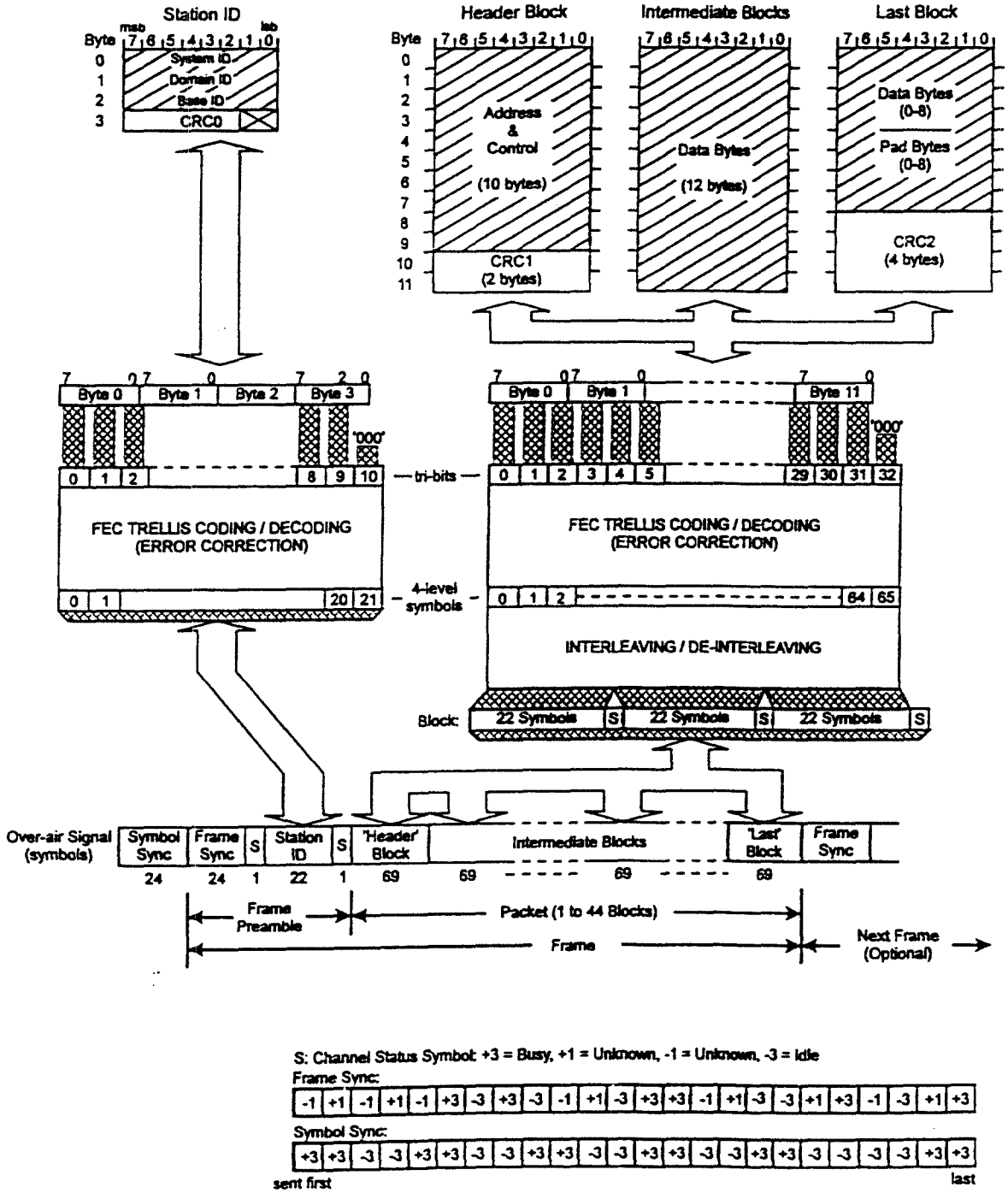
This is expanded so that an 8-bit byte translates to four symbols for the T4S, T24S and R4S tasks described in section 4.5.2

	MSB							LSB
Bits:	7	6	5	4	3	2	1	0
Symbols:	a		b		c		d	
	sent first						sent last	

2. FEC (more complicated), essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, TSID, RHB, RILB and RSID described in section 4.5.2

4.4 Frame Structure

The MX929A Frame Structure (as used in a RD-LAP™ system) is illustrated in Figure 7, and consists of a Frame Preamble (comprising a 24-symbol Frame Synchronization pattern and Station ID block) followed by a 'Header Block', one or more 'Intermediate Blocks and a 'Last Block'. Channel Status (S) symbols are included at regular intervals. The first Frame of any transmission is preceded by a Symbol Synchronization pattern.



S: Channel Status Symbol: +3 = Busy, +1 = Unknown, -1 = Unknown, -3 = Idle

Frame Sync:

-1	+1	-1	+1	-1	+3	-3	+3	-3	-1	+1	-3	+3	+3	-1	+1	-3	-3	+1	+3	-1	-3	+1	+3

Symbol Sync:

+3	+3	-3	-3	+3	+3	-3	-3	+3	+3	-3	-3	+3	+3	-3	-3	+3	+3	-3	-3	-3	-3	+3	+3

sent first last

Figure 7: Over-Air-Signal Format

The 'Header' block is self-contained, includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any), and miscellaneous control information.

The 'Intermediate' block(s) contain only data. The checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks.

Proprietary systems which do not use the RD-LAP™ format may use the block structures provided by the MX929A to build alternative frame formats more suited to the particular application. Some examples are illustrated in Figure 8.

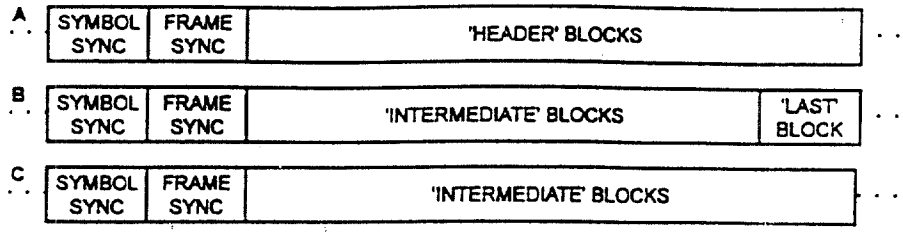


Figure 8: Some Alternative Frame Structures

The MX929A performs all of the block formatting and de-formatting, the binary data transferred between the modem and the µC is indicated by the diagonal lines in Figure 7.

4.5 The Programmer's View

To the programmer, the modem appears as 4 write only, 8-bit registers, and shadowed by 3 read only registers. The individual registers are selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note: There is a minimum time allowance between accesses of the modem's registers, see section 6.1.

4.5.1 Data Block Buffer

This is a 12-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC.

To the µC, the Data Block buffer appears as a single 8-bit register. The modem ensures that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

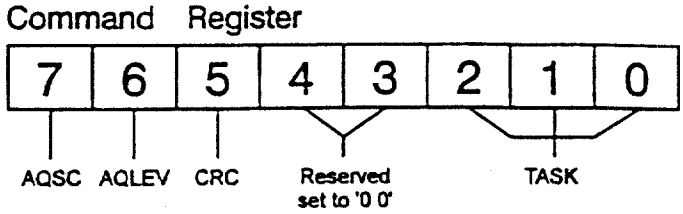
The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode.

Note: In receive mode, the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

4.5.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQSC bits.



When there is no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, otherwise the received data is ignored.

4.5.2.1 Command Register B7: AQSC - Acquire Symbol Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQSC bit set to '1'.

The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFP (Search for Frame Preamble) task is written to the MX929A, however it may also be used independently to re-establish clock Synchronization quickly after a long fade. Alternatively, a SFS or SFP task may be written to the Command Register with the AQSC bit at '0' if it is known that clock Synchronization does not need to be re-established. More details of the clock acquisition sequence are given in section 5.3

4.5.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal immediately. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, therefore improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The AQLEV bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFP (Search for Frame Preamble) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFP task may be written to the Command Register with the AQLEV bit at '0' if it is known that there is no need to re-establish the received signal levels. More details of the level measurement acquisition sequence are given in section 5.3.

4.5.2.3 Command Register B5: CRC

This bit allows the user to select between two different forms of the CRC0, CRC1, and CRC2 check sums. When this bit is set to '1' the CRC generators are initialized to 'all zeros', as required by RD-LAP systems. When this bit is set to '0' the CRC generators are initialized to 'all ones' as required by CCITT X25 based systems. It should always be set to '1' for RD-LAP compatibility, other systems may set this bit as required.

4.5.2.4 Command Register B4, B3

These two bits should always be set to '0'

4.5.2.5 Command Register B2, B1, B0: TASK

Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write a task and the associated data to the modem while the modem is still transmitting the data from the previous task.

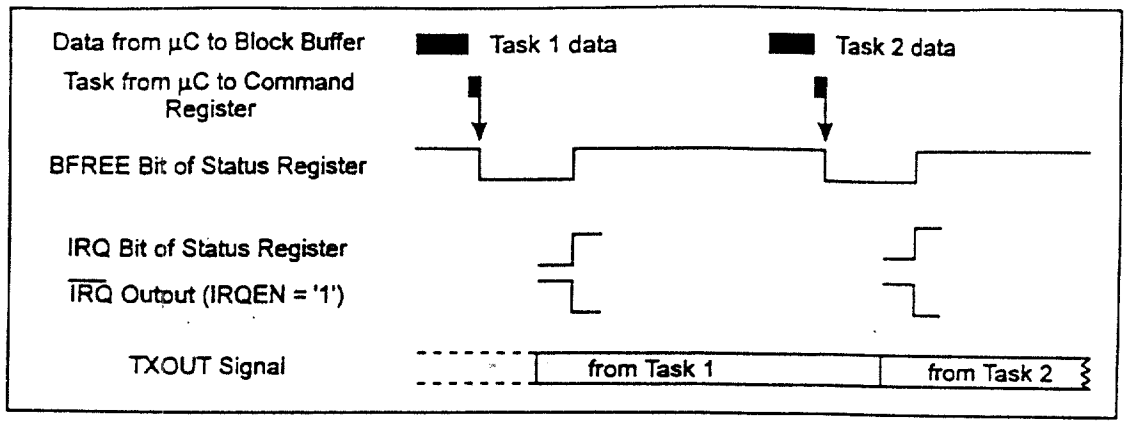


Figure 9: Transmit Task Overlapping

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed, and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

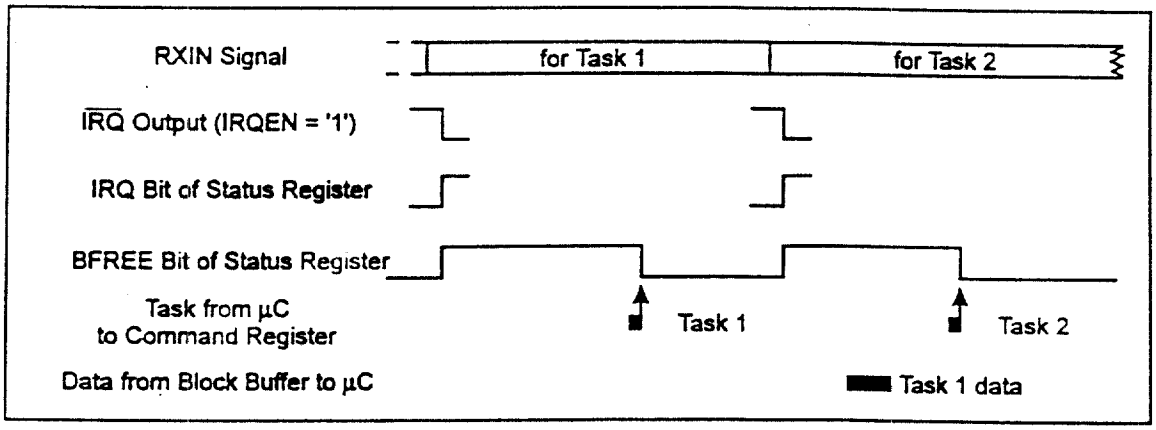


Figure 10: Receive Task Overlapping

Note: Detailed timings for the various tasks are provided in Figure 11 and Figure 12.

MX929A Modem Tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFP	Search for Frame Preamble	T24S	Transmit 24 symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 symbols	T4S	Transmit 4 symbols
1	1	0	RSID	Read Station ID	TSID	Transmit Station ID
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.5.2.6 NULL: No effect

This task is provided so that a AQSC or AQLEV command can be initiated without loading a new task.

4.5.2.7 SFP: Search for Frame Preamble

This task causes the modem to search the received signal for a valid Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID data which has a correct CRC0 checksum.

The task continues until a valid Frame Preamble has been found.

The search consists of four stages:

First of all the modem will attempt to match the incoming symbols against the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Control Register.

Once a match has been found, the modem will read in the following 'S' symbol, place it in the SVAL bits of the Status Register then set the SRDY bit to '1'. (The IRQ bit of the Status Register will also be set to '1' at this time if the SSIEN bit of the Mode Register is '1').

The modem will then read the next 22 symbols as station ID data. They will be decoded and the CRC0 checked. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.

If the received CRC0 is correct, the following 'S' symbol will be read into the SVAL bits of the Status Register and the SRDY, BFREE and IRQ bits set to '1', the CRCERR bit cleared to '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

On detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the 3 Station ID bytes from the Data Block Buffer then write the next task to the modem's Command Register.

4.5.2.8 RHB: Read Header Block

This task causes the modem to read the next 69 symbols as a 'Header' Block. It will strip out the 'S' symbols then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC1 checksum bytes.

As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received, the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

4.5.2.9 RILB: Read 'Intermediate' or 'Last' Block

This task causes the modem to read the next 69 symbols as an 'Intermediate' or 'Last' block (the µC can tell from the 'Header' block how many blocks are in the frame, and when to expect the 'Last' block).

In each case, it will strip out the 3 'S' symbols, de-interleave and decode the remaining 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum

As each of the 3 'S' symbols of the block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received, the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

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4.5.2.10 SFS: Search for Frame Sync

This task - which is intended for special test and channel monitoring purposes - performs the first two parts only of a SFP task. It causes the modem to search the received signal for a 24-symbol sequence which matches the required Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will read in the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to '1' and update the SVAL bits. The µC may then write the next task to the Command Register.

4.5.2.11 R4S: Read 4 Symbols

This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by SFS task

4.5.2.12 RSID: Read Station ID

This task causes the modem to read in and decode the following 23 symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of a SFP task except that it will not re-start if the received CRC0 is incorrect. It would normally follow a SFS task.

The 3 decoded bytes will be placed into the Data Block Buffer, and the CRCERR bit of the Status Register set to '1' if the received CRC0 was incorrect, otherwise it will be cleared to '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY and IRQ bits set to '1' to indicate that the µC may read the 3 received bytes from the Data Block Buffer and write the next task to the modem's Command Register.

4.5.2.13 T24S: Transmit 24 Symbols

This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC, FEC, interleaving or adding any 'S' symbols.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data has to be written to the Data Block Buffer to transmit the MX929A Symbol and Frame Sync sequences:

'Symbol Sync'				Values written to Data Block Buffer		
Symbols					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
-3	-3	+3	+3	Byte 5 :	01011111	5F

'Frame Sync'				Values written to Data Block Buffer		
Symbols					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

4.5.2.14 THB: Transmit Header Block

This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block , inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.15 TIB: Transmit Intermediate Block

This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block , inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.16 TLB: Transmit Last Block

This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block , inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.17 T4S: Transmit 4 Symbols

This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

4.5.2.18 TSID: Transmit Station ID

This task takes 3 ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.19 RESET: Stop any current action

This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied, to set the modem into a known state.

Note: Due to delays in the RRC filter, it will take several symbol times for any change to appear at the TXOUT pin.

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Task Timings

		Task	Time (symbol times)
t1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1' (high).	T24S TSID THB/TIB/TLB T4S	5 6 16 0
t3	Time to transmit all symbols of the task	T24S/TSID THB/TIB/TLB T4S	24 69 4
t4	Max time allowed from BFREE going to a logic '1' for next task (and data) to be written to modem	T24S TSID THB/TIB/TLB T4S	18 17 52 3
t5	Time to receive all symbols of task	SFS SFP RSID RHB/RILB R4S	25 (min) 48 (min) 23 69 4
t6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem	SFS SFP RSID RHB/RILB R4S	21 21 15 51 3
t7	Maximum time from the last bit of the task entering the de-interleave circuit to BFREE going to a logic '1'	Any	1

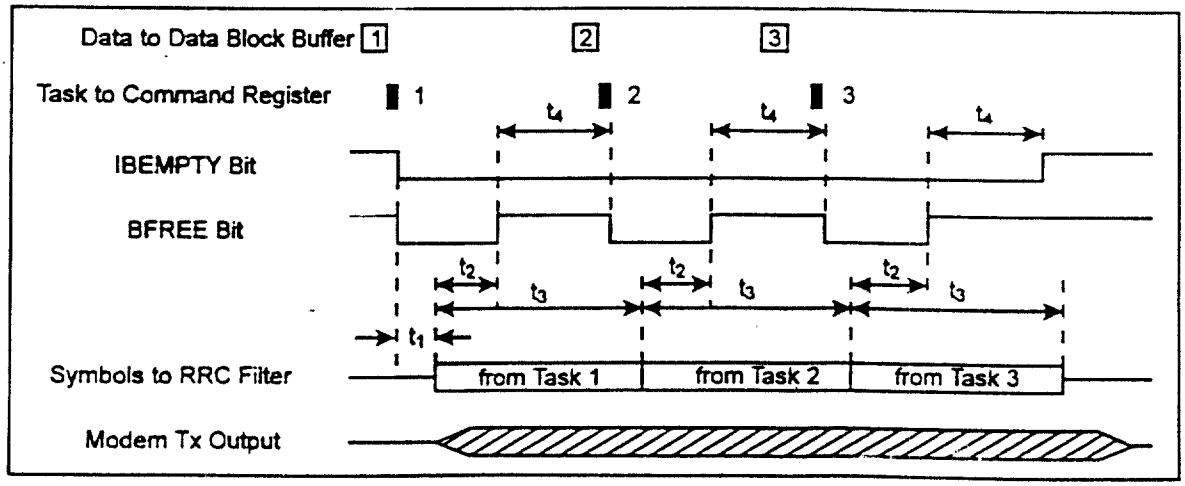


Figure 11: Transmit Task Timing Diagram

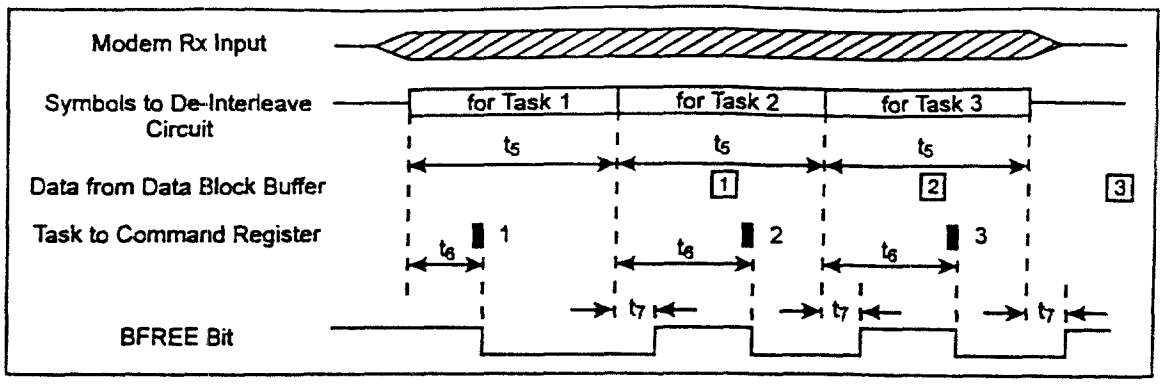


Figure 12: Receive Task Timing Diagram

RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of approximately 8 symbol times through to the RRC filter in both transmit and receive modes, as shown in Figure 13:

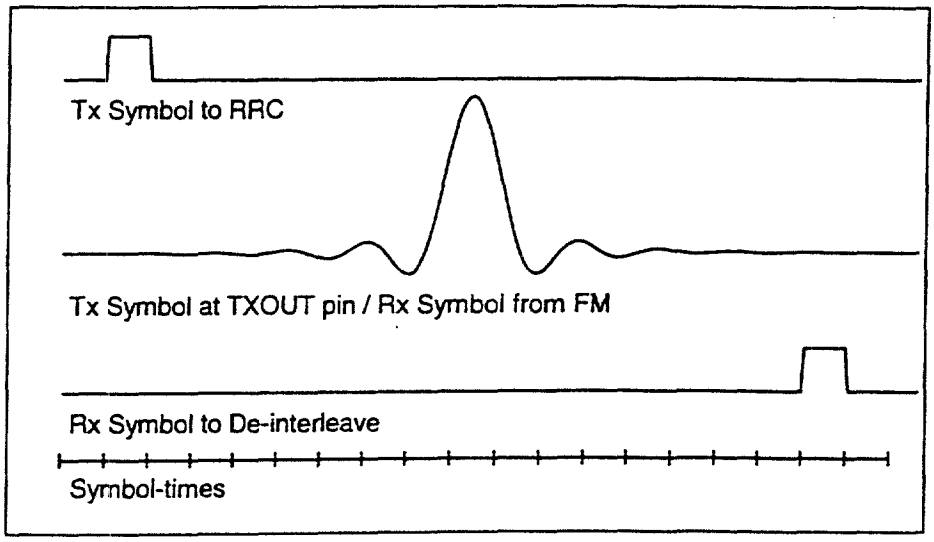
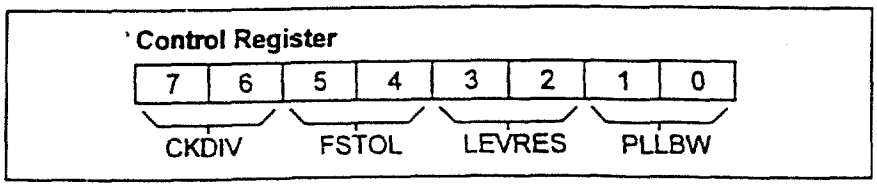


Figure 13: RRC Low Pass Filter Delay

4.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.



4.5.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the $\overline{XTAL}$ pin, thereby determining the nominal symbol rate. The table below shows how symbol rates of 2400/4800/9600 symbols/sec may be obtained from common Xtal frequencies:

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	B6	Division Ratio: Xtal Frequency/Symbol Rate	Symbol Rate (symbols/sec)		
0	0	512	4800	9600	
0	1	1024	2400	4800	9600
1	0	2048		2400	4800
1	1	4096			2400

Note: Device operation is not guaranteed below 2400 or above 9600 symbols/sec.

4.5.3.2 Control Register B5, B4: FSTOL - Frame Sync Tolerance

These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches.

4.5.3.3 Control Register B3, B2: LEVRES - Level Measurement Modes

These two bits have no effect in transmit mode. In receive mode they set the 'normal' operating mode of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an ACLEV command.

B3	B2	Mode
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

For most applications these two bits should be set to 'Slow Peak Detect' mode, in which the peak positive and peak negative excursions of the received signal (after filtering) are measured to establish the amplitude and dc offset of the signal. The decay time-constant of the peak rectifier circuits used in this mode is approximately 750 symbol times.

The 'Hold' setting freezes the stored values of the current amplitude and offset measurements and may therefore be used to improve performance during short fades or while the radio is switched from receive mode for the transmission of a short acknowledgment. It should be noted, however, that the measured amplitude and offset values are stored on the external capacitors C7 and C8 and will decay gradually when the 'Hold' setting is chosen, the discharge time-constant being approximately 750 symbol times.

The 'Lossy Peak Detect' setting is similar to 'Slow Peak Detect' except that the decay time-constant of the peak detectors are reduced to approximately 25 symbol times to give a faster response to signal changes at the expense of a reduction in BER performance. This mode is used by the automatic Level Measurement acquisition sequence but may also be useful in non-standard systems.

The 'Clamp' setting is primarily intended for use by the automatic Level Measurement acquisition sequence as described in section 5.3, but may also be useful in non-standard systems. In this mode the DOC1 and DOC2 pins are connected directly to the output of the circuit that normally drives the peak detectors.

4.5.3.4 Control Register B1, B0: PLLBW - Phase-Locked Loop Modes

These two bits have no effect in transmit mode In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQSC command.

B1	B0	PLL Mode	Working Bandwidth (±ppm)
0	0	Hold	-
0	1	Narrow Bandwidth	20
1	0	Medium Bandwidth	100
1	1	Wide Bandwidth	650

The minimum bandwidth consistent with the transmit and receive modem symbol rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracy's of within ± 50ppm, then the PLLBW bits should be set to '10' ('Medium Bandwidth'). However, to allow the PLL to settle quickly it is recommended that when very close tolerance Xtals are used, then the PLLBW bits should be set to 'Medium' whenever an AQSC is triggered, and only changed to 'Narrow' about 200 symbol times later.

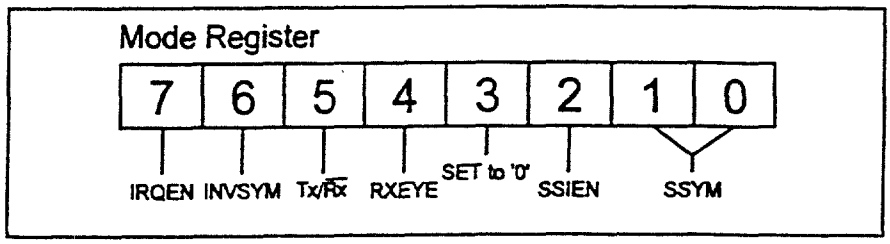
The 'Wide Bandwidth' setting is intended for message acquisition in systems where the µC cannot detect the start of a received message, as it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate Vs Signal to Noise performance.

The 'Hold' setting disables the PLL feedback loop, and may be used during signal fades.

Note: 'Working Bandwidths' are the maximum difference between the actual received symbol rate and the nominal rate determined by the tolerance of the modem's Xtal frequency, to give minimal degradation of a reasonably random received signal.

4.5.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.5.4.1 Mode Register B7: IRQEN - $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (to V_{SS}) when the IRQ bit of the Status Register is a '1'.

4.5.4.2 Mode Register B6: INVSYM - Invert Symbols

This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOUT	Signal at RXAMPOUT
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

4.5.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode.

Note: Changing between receive and transmit modes will cancel any current task.

4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye

This bit should normally be set to '0'.

Setting it to '1' when the modem is in receive mode configures the modem into a special test mode, in which the input of the Tx output buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TXOUT pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator.

The resulting eye diagram (for reasonably random data) should ideally be as shown in Figure 14, with 4 'crisp' and equally spaced crossing points.

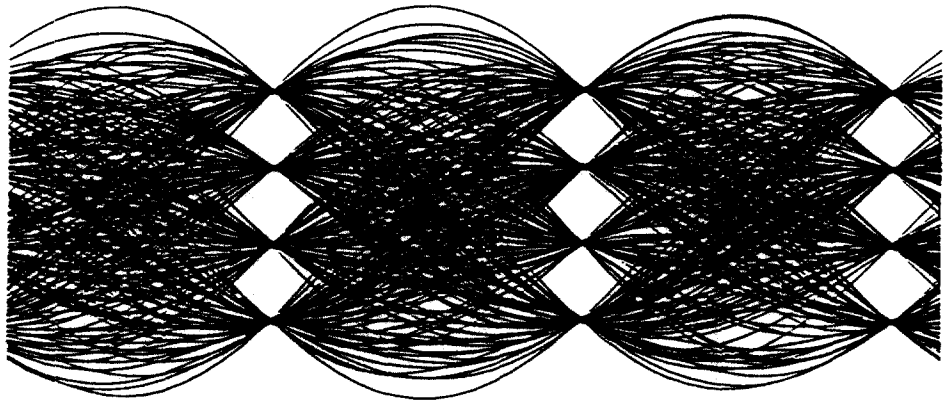


Figure 14: Ideal 'RXEYE' Signal

4.5.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in 'powersave mode' in which the internal filters, the RX Symbol and Clock extraction circuits, and the Tx output buffer will be disabled. The TXOUT pin will be connected to V_{BIAS} through a high value resistance. The XTAL/CLOCK oscillator, Rx input amplifier, and the µC interface logic will continue to operate.

4.5.4.6 Mode Register B2: SSIEN - 'S' Symbol IRQ Enable

In receive mode, setting this bit to '1' causes the IRQ bit of the status register to be set to '1' whenever a new 'S' symbol has been received. (The SRDY bit of the Status Register will also be set to '1' at the same time, and the SVAL bits updated to reflect the received 'S' symbol.)

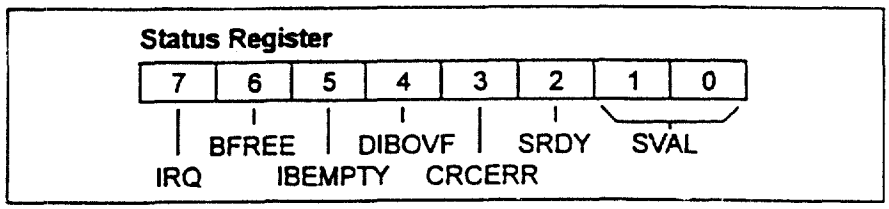
In transmit mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a 'S' symbol has been transmitted. (The SRDY bit of the Status Register will also be set to '1' at the same time.)

4.5.4.7 Mode Register B1, 0: SSYM - 'S' Symbol To Be Transmitted

In transmit mode these two bits define the next 'S' symbol to be transmitted. These bits have no effect in receive mode.

4.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.5.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register TX/$\overline{RX}$ bit.

Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register TX/$\overline{RX}$ bit.

Status Register DIBOVF bit going from '0' to '1'.

Status Register SRDY bit being set to '1' (due to a 'S' symbol being received or transmitted) if the Mode Register SSIEN bit is '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (to V_{SS}) whenever the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

4.5.5.2 Status Register B6: BFREE - Data Block Buffer Free

This bit reflects the availability of the Data Block Buffer and is cleared to '0' whenever a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register TX/$\overline{RX}$ bit is changed.

4.5.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TX/$\overline{RX}$ bit, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid level (half-way between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

4.5.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB, RSID or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the TX/$\overline{RX}$ bit of the Mode Register.

In transmit mode this bit is '0'.

4.5.5.5 Status Register B3: CRCERR - CRC Checksum Error

In receive mode this bit will be updated at the end of a SFP, RHB, RILB or RSID task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error. In transmit mode this bit will be '0'.

Note: This bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task, or by changing the TX/$\overline{RX}$ bit of the Mode Register.

4.5.5.6 Status Register B2: SRDY - 'S' Symbol Ready

In receive mode, this bit is set to '1' whenever an 'S' symbol has been received. The µC may then read the value of the symbol from the SVAL field of the Status Register. In transmit mode, this bit is set to '1' whenever an 'S' symbol has been transmitted.

The bit is cleared to '0' immediately after a read of the Status Register, by a RESET task or by changing the TX/$\overline{RX}$ bit of the Mode Register.

4.5.5.7 Status Register B1, B0: SVAL - Received 'S' Symbol Value

In receive mode, these two bits reflect the value of the latest received 'S' symbol. In transmit mode, these two bits will be '0'.

4.5.6 Data Quality Register

In transmit mode and for 64 symbol times after enabling receive mode or after starting an AQSC or AQLEV sequence the value in the Data Quality Register will be invalid.

In receive mode, the MX929A continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal'.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 15 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

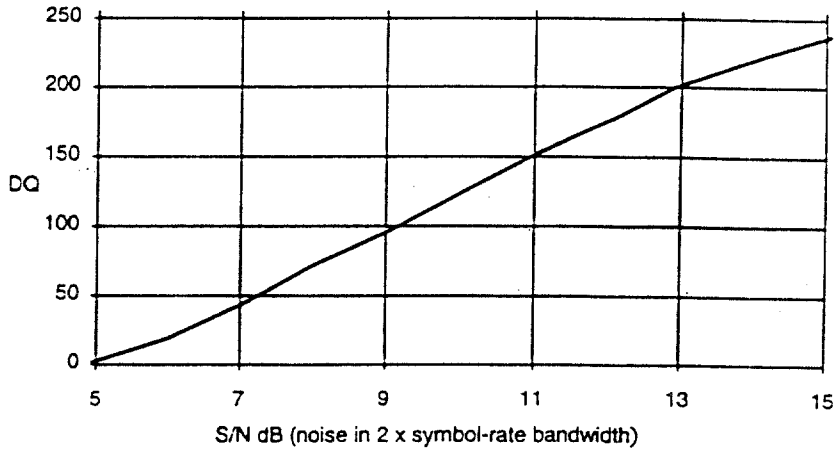


Figure 15: Typical Data Quality Reading vs S/N

4.6 CRC, FEC and Interleaving

4.6.1 Cyclic Redundancy Codes

4.6.1.1 CRC0

This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24 bits of the block (Bytes 0,1 & 2) as follows:

The 24 bits are considered as the coefficients of a polynomial M(x) of degree 23, such that the msb bit (7) of byte 0 is the coefficient of x^{23}, and bit 0 of byte 2 is the coefficient of x^0.

The polynomial F(x) of degree 5 is calculated as being the remainder of the modulo-2 division

$$x^6 M(x) / (x^6 + x^4 + x^3 + 1)$$

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to F(x)

The coefficients of F(x) are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the msb of CRC0.

4.6.1.2 CRC1

This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

4.6.1.3 CRC2

This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$

Note: In receive mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB or TLB.

4.6.2 Forward Error Correction

In transmit mode, the MX929A uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate' or 'Last' Block or the 30 bits of a Station ID Block into a 66 or 22-symbol sequence which includes FEC information.

In receive mode, the MX929A decodes the received 22 or 66 symbols of a block into 30 or 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

4.6.3 Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission (and before the 'S' symbols are added) to give protection against the effects of noise bursts and short fades. The 22 symbols of a 'Station ID' Block are not interleaved.

In receive mode, the MX929A de-interleaves the received symbols after stripping out the 'S' symbols and prior to decoding.

5. Application Notes

5.1 Transmit Frame Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, Station ID block, and one each Header, Intermediate and Last blocks are shown below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQEN and TX/$\overline{RX}$ bits of the Mode Register are '1', the RXEYE, PSAVE and SSIEN bits are '0' and the INVSYM bit is set appropriately.
2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes to the Data Block Buffer and a T24S task to the Command Register.
3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
4. Write 6 Frame Sync bytes to the Data Block Buffer and a T24S task to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
6. Write 3 Station ID bytes to the Data Block Buffer and a TSID task to the Command Register.
7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
8. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.
9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
10. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
12. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.
13. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
14. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Note: The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.

The SSYM bits of the Mode Register may be altered at any time to change the transmitted 'S' symbols. If a timing reference is required, setting the Mode Register SSIEN bit to '1' will cause a µC interrupt after every 'S' symbol transmitted - in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.

Figure 16 and Figure 17 illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Station ID Block, a Header Block, any number of Intermediate Blocks and one Last Block. It is assumed that the Tx Interrupt Service routine (Figure 17) is called when the MX929A's $\overline{IRQ}$ outline goes low.

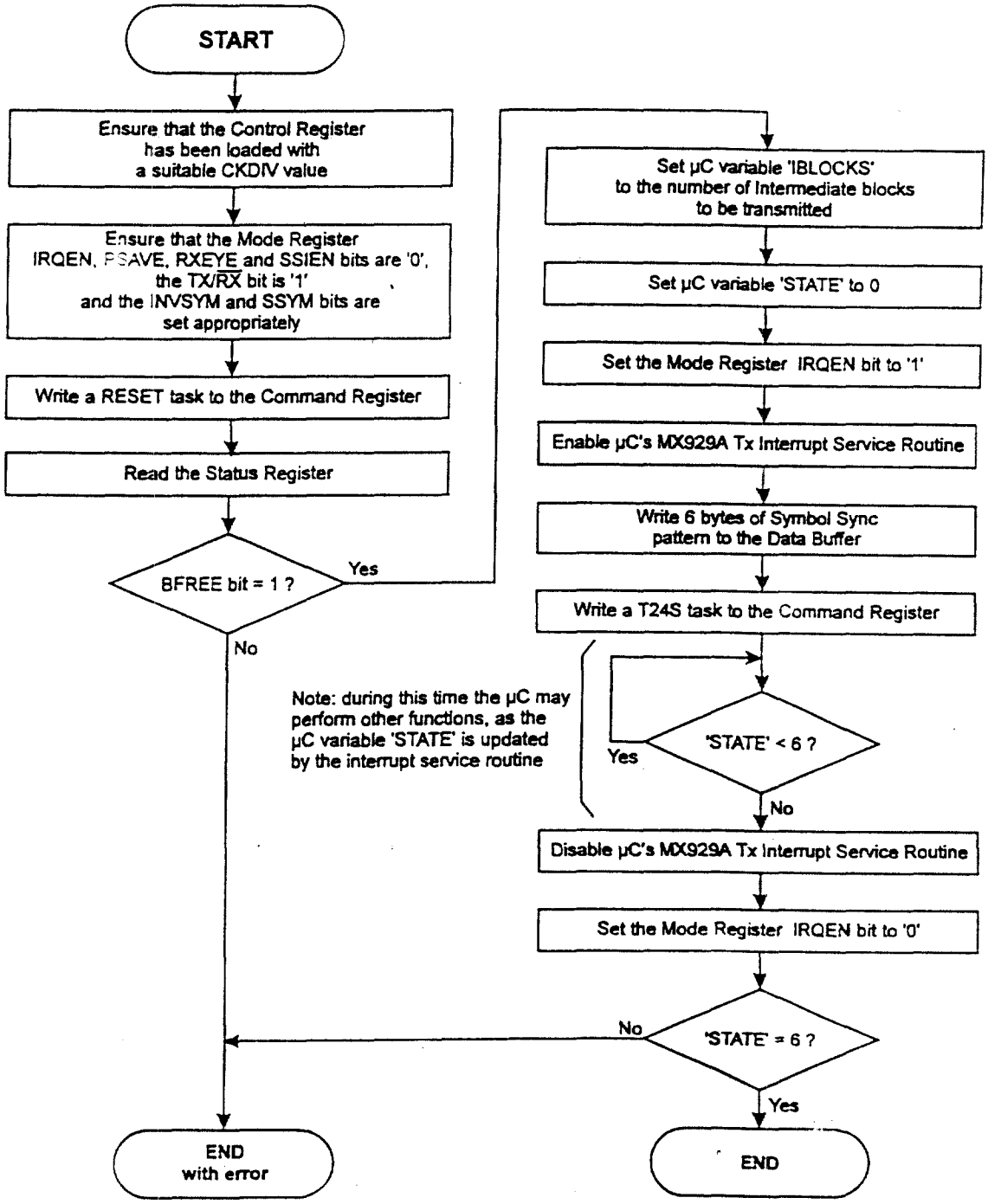


Figure 16: Transmit Frame Example Flowchart , Main Program

Note: The RESET command in Figure 16 and the practice of disabling the MX929A's $\overline{IRQ}$ output when not needed are essential, but can eliminate problems during debugging and if errors occur in operation. The CRC bit should be set appropriately when a byte is written to the Command Register.

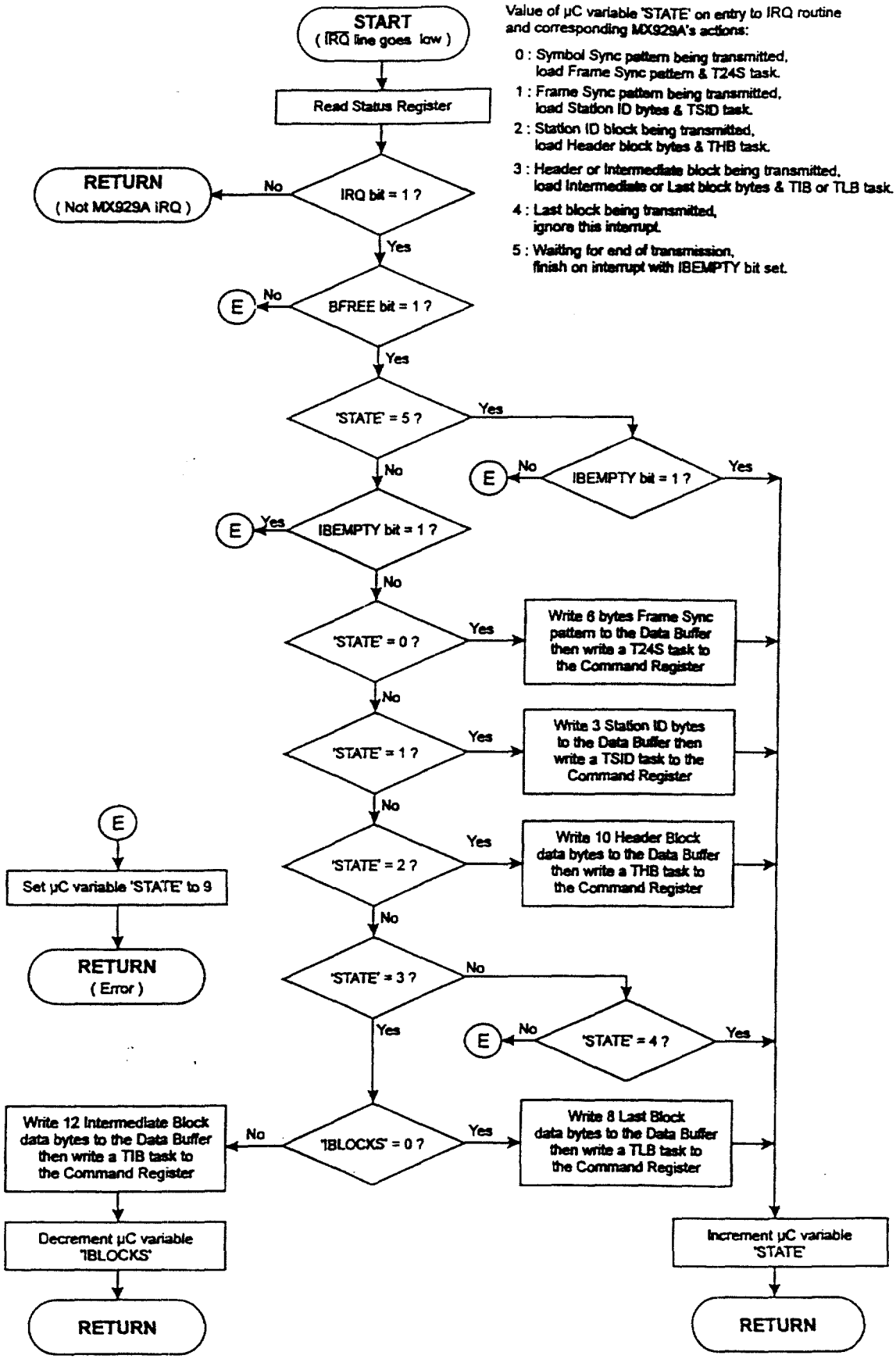


Figure 17: Transmit Interrupt Service Routine

5.2 Receive Frame Example

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences, Station ID block and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQEN bit of the Mode Register is '1', the TX/$\overline{RX}$, RXEYE PSAVE, and SSIEN bits are '0', and the INVSYM bit is set appropriately.
2. Wait until the received carrier has been present for at least 8 symbol times (see section 5.3).
3. Read the Status Register to ensure that the BFREE bit is '1'.
4. Write a byte containing a SFP task with the AQSC and AQLEV bits set to '1' to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.
6. Read 3 Station ID bytes from the Data Block Buffer.
7. Write a RHB task to the Command Register.
8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
9. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.
10 Write a RILB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
12. Read 12 Intermediate Block bytes from the Data Block Buffer.
13. Write a RILB task to the Command Register.
14. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
15. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from Data Buffer.

Note: The value of the latest 'S' symbol received will be contained in the SVAL bits each time that the Status Register is read. If desired, the Mode Register SSIEN bit may be set to '1', which will cause a µC interrupt after every 'S' symbol is received - in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.

Figure 18 and Figure 19 illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Station ID Block, a Header Block, any number of Intermediate Blocks and one Last Block.

It is assumed that the Rx Interrupt service routine (Figure 19) is called when the MX929A's $\overline{IRQ}$ output line goes low.

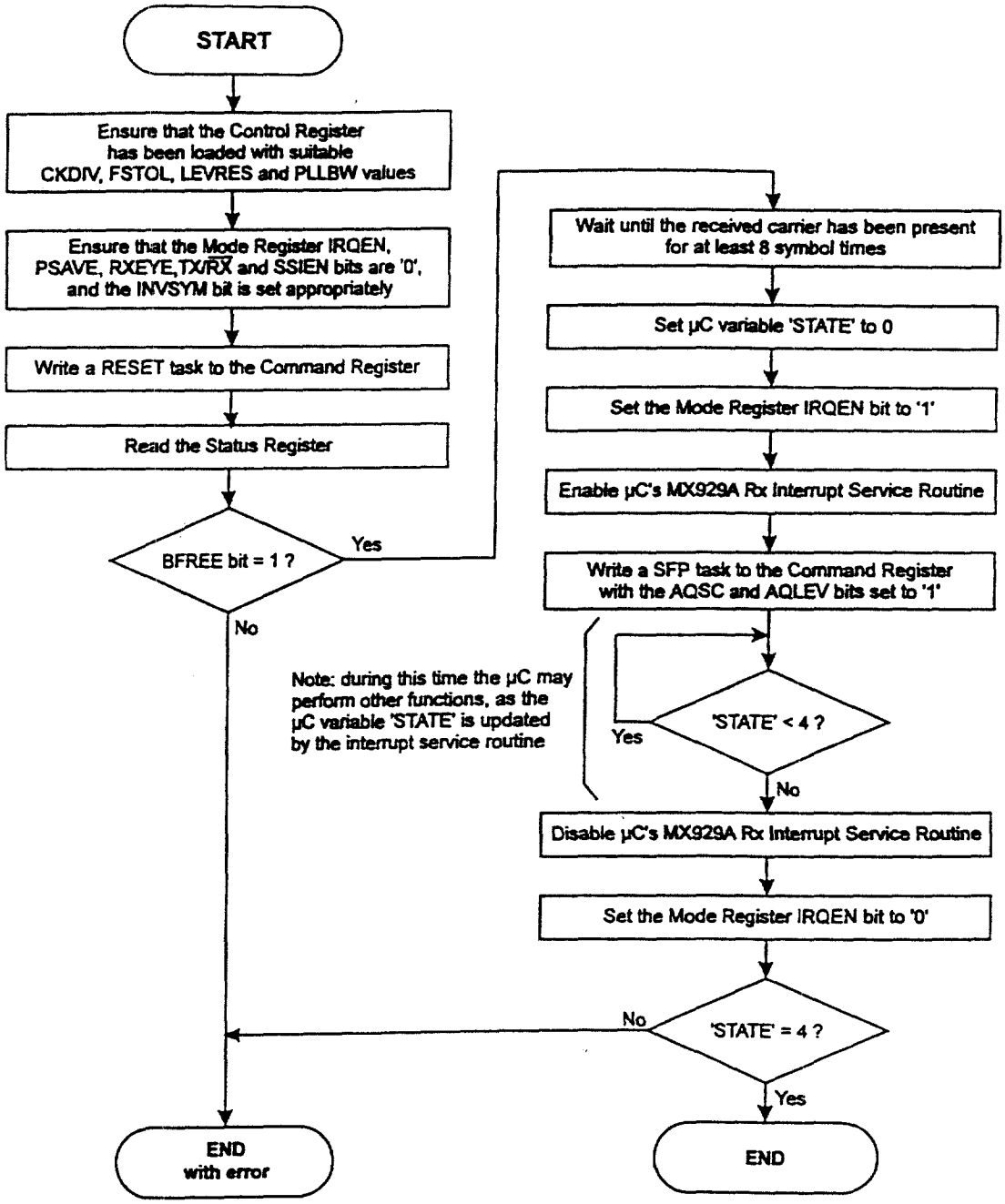


Figure 18: Receive Frame Example Flowchart, Main Program

Note: The RESET command in Figure 18 and the practice of disabling the MX929A's $\overline{IRQ}$ output when not needed are not essential, but can eliminate problems during debugging and if errors occur in operation. The CRC bit should be set appropriately when a byte is written to the Command Register.

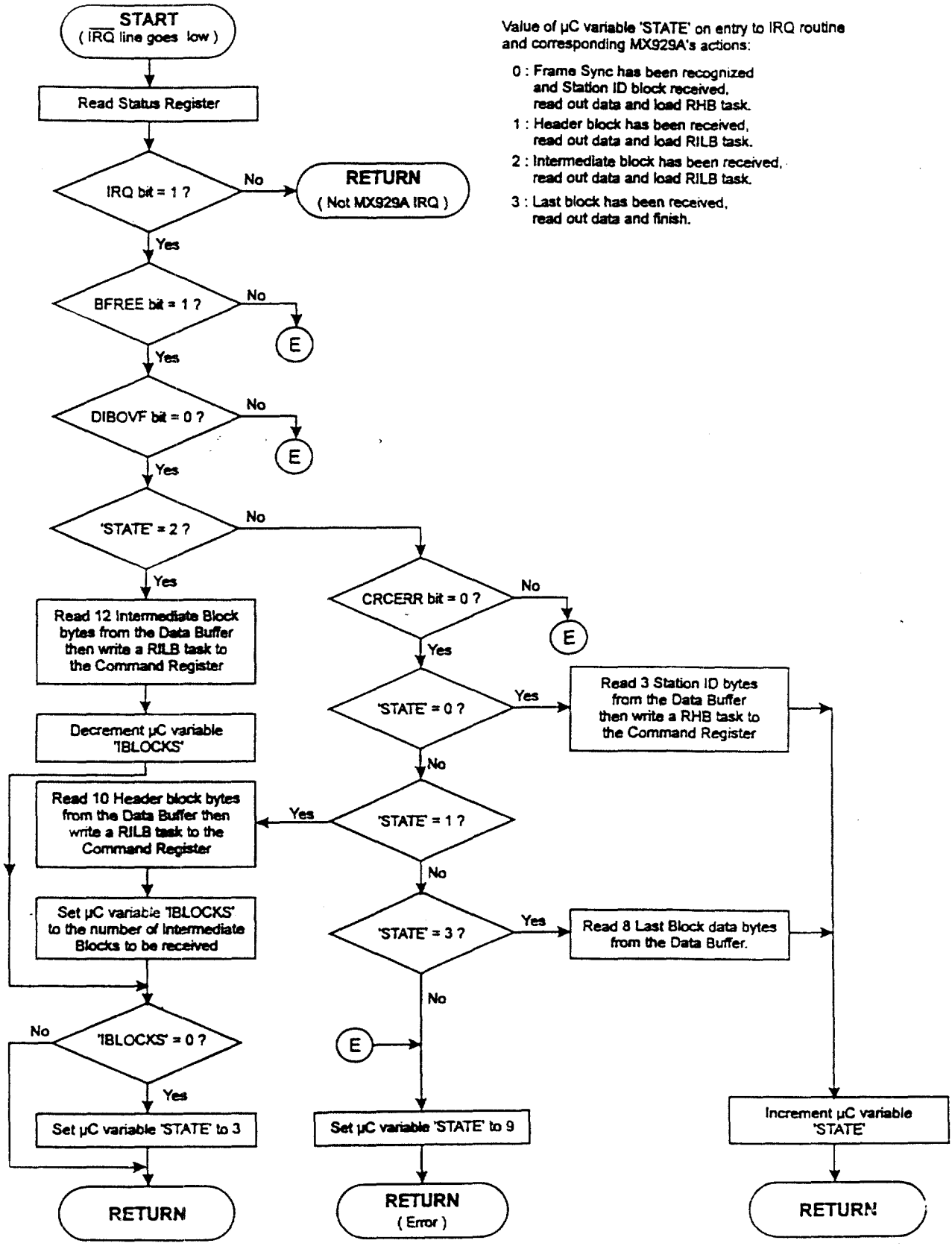


Figure 19: Receive Interrupt Service Routine

Note: This routine assumes that the number of Intermediate Blocks in the Frame are contained within the header Block

5.3 Clock Extraction and Level Measurement Systems

The MX929A is intended for use in systems where the Symbol Sync pattern is transmitted immediately on start-up of the transmitter.

When the carrier is detected by the receiver or when the receiver is switched to another channel, the controlling µC should wait approximately 8 symbol times for the received signal to propagate through the modem's RRC filter then issue a SFS or SFP task with the AQSC and AQLEV bits set to '1'. The 8-symbol delay can usefully be included in the carrier detect circuitry.

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude and dc offset as quickly as possible during the Symbol Sync period before switching to more accurate - but slower - measurement modes for the remainder of the received message.

Note: If the acquisition sequences are triggered after the Symbol Sync period - as can happen when the receiver is switched to another channel - they will still function correctly, but will take much longer to acquire accurate level and timing information.

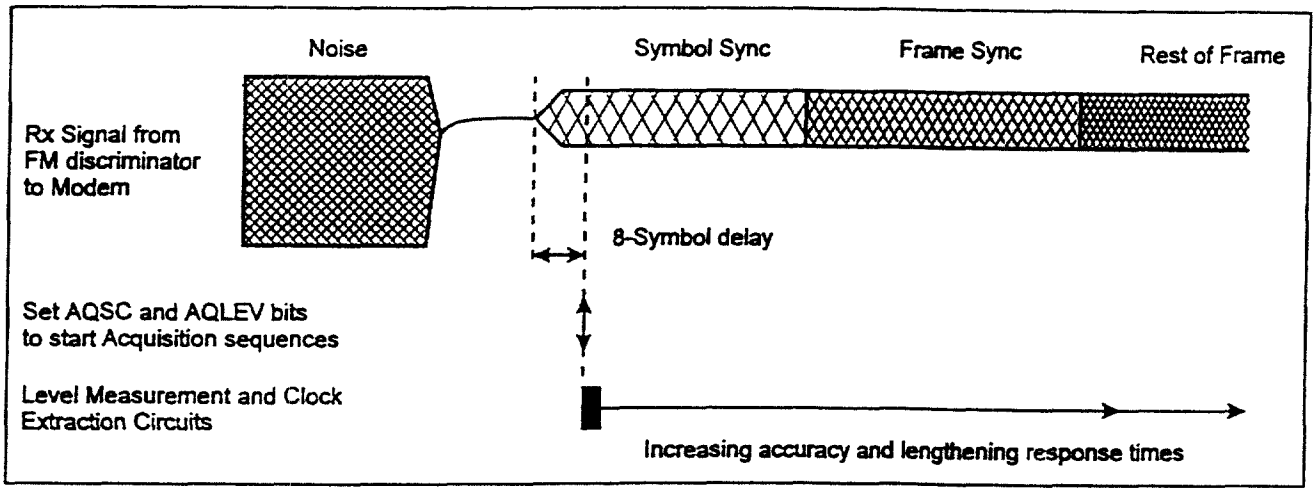


Figure 20: Acquisition sequence Timing

The operation of the Level Acquisition Sequence depends on the settings of the Control Register LEVRES bits:

LEVRES setting:	B3	B2	Details of Level Acquisition Sequence
'Hold'	0	0	1 symbol time of 'Clamp' mode then 15 symbol times of 'Lossy Peak Detect' mode before reverting to 'Hold' mode.
'Slow Peak Detect'	0	1	1 symbol time of 'Clamp' mode then 15 symbol times of 'Lossy Peak Detect' mode before reverting to 'Slow Peak Detect' mode.
'Lossy Peak Detect'	1	0	1 symbol time of 'Clamp' mode before reverting to 'Lossy Peak Detect' mode
'Clamp'	1	1	Remain in 'Clamp' mode.

The 1-symbol 'Clamp' time at the start of these sequences is used to make an initial measurement of the dc offset present on the received signal, after which the 'Lossy Peak Detect' period is used to estimate the signal amplitude.

The operation of the Symbol Clock Acquisition Sequence depends on the settings of the Control Register PLLBW bits:

PLLBW setting:	B1	B0	Details of Symbol Clock Acquisition Sequence
'Hold'	0	0	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' mode before reverting to 'Hold' mode.
'Narrow' BW	0	1	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' mode before reverting to 'Narrow BW' mode.
'Medium BW'	1	0	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' before reverting to 'Medium BW' mode.
'Wide BW'	1	1	16 symbol times of 'Extra-wide BW' mode before reverting to 'Wide BW' mode.

Note: The 'Extra-wide BW' PLL mode is designed to synchronize rapidly to the '+3 +3 -3 -3 ...' Symbol Sync pattern and is available only as part of an automatic acquisition sequence.

Although not recommended, it is possible to use the modem in a non-standard system where there is an indeterminate delay between the transmitter start-up and the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC. In these cases the Symbol Sync pattern should be extended to about 100 symbols, and the Control Register LEVRES bits should be set to 'Lossy Peak Detect' and the PLLBW bits to 'Wide BW' before initiating a 'SFS + AQSC + AQLEV' task. Once the Frame Sync pattern has been detected, the Control Register settings may be changed to 'Slow Peak Detect' and 'Medium' or 'Narrow' PLL bandwidth for the remainder of the received message.

5.4 AC Coupling

For a practical circuit, ac coupling from the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem, may be desired. However, there are two problems:

1. AC Coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of ac coupling:

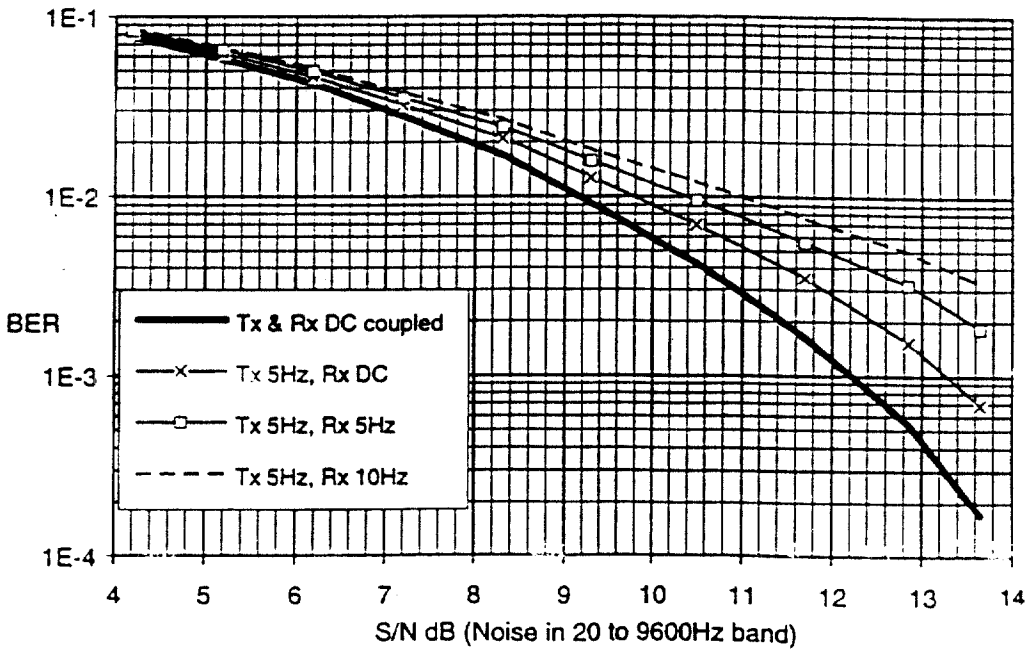


Figure 21: Effect of AC Coupling on BER

2. AC Coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 22, the time for this step to decay to 37% of its original value is 'RC' where:

   RC = 1/(2 x π x the 3dB cut-off frequency of the RC network)

   which is 32 msec, or 153 symbol times at 4800 symbols/sec, for a 5Hz network.

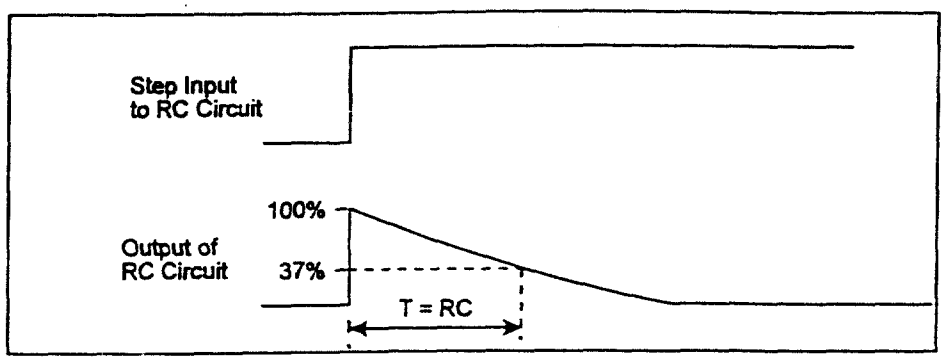


Figure 22: Decay Time - AC Coupling

In general, it is best to dc couple the receiver discriminator to the modem, and to ensure that any AC Coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800 symbols/sec).

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using these modems depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved, subject to local regulatory requirements, over a system with 12.5kHz channel spacing, if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive '+3 +3 -3 -3 ....' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio. Particular attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye - using the Mode Register RXEYE function - gives a good indication of the overall transmitter/receiver performance.

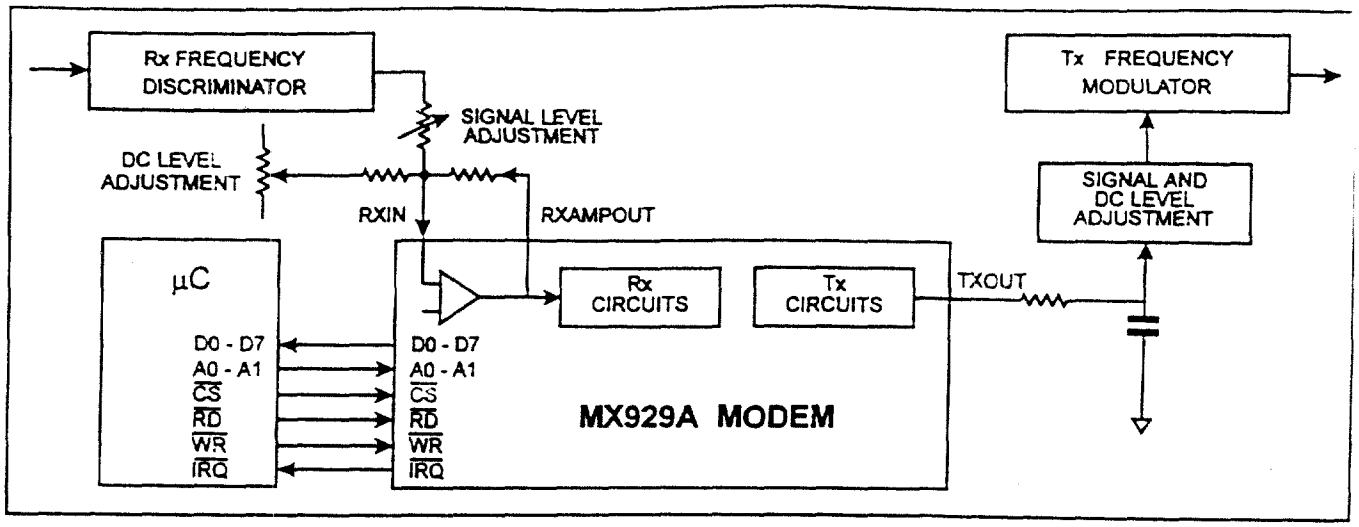


Figure 23: Typical connections Between Radio and MX929A

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Symbol Rate		2400	9600	Symbols/sec
Xtal Frequency		1.0	10.0	MHz

Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152mhz, Symbol Rate = 4800 symbols/sec,
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 3.3V to 5.0V, T_{AMB} = - 40°C to 85°C.

	Notes	Min.	Typ.	Max.	Units
DC PARAMETERS					
I_{DD} (V_{DD} = 5.0V)	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode, V_{DD} = 5.0V)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.6		mA
AC PARAMETERS					
Tx Output					
TXOUT Impedance	2		1.0	2.5	kΩ
Signal Level	3	0.8	1.0	1.2	V_{P-P}
Output DC Offset wrt V_{DD}/2	4	-0.25		0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
DC Offset wrt V_{DD}/2	5	-0.5		0.5	V
Xtal/Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	-5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10	µA

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics Notes:

1. At 25°C. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance, at V_{DD} = 5.0V and T_{AMB} = 25°C.
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence, at V_{DD} = 5.0V and T_{AMB} = 25°C (output level is proportional to V_{DD}).
4. Measured at the TXOUT pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXAMPOUT pin, for a "...+3 +3 -3 -3..." symbol sequence, at V_{DD} = 5.0V and T_{AMB} = 25°C. Optimum level is proportional to V_{DD}.
6. Timing for an external input to the CLOCK/XTAL pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

Timing

µC Parallel Interface Timings (ref. Figure 24)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

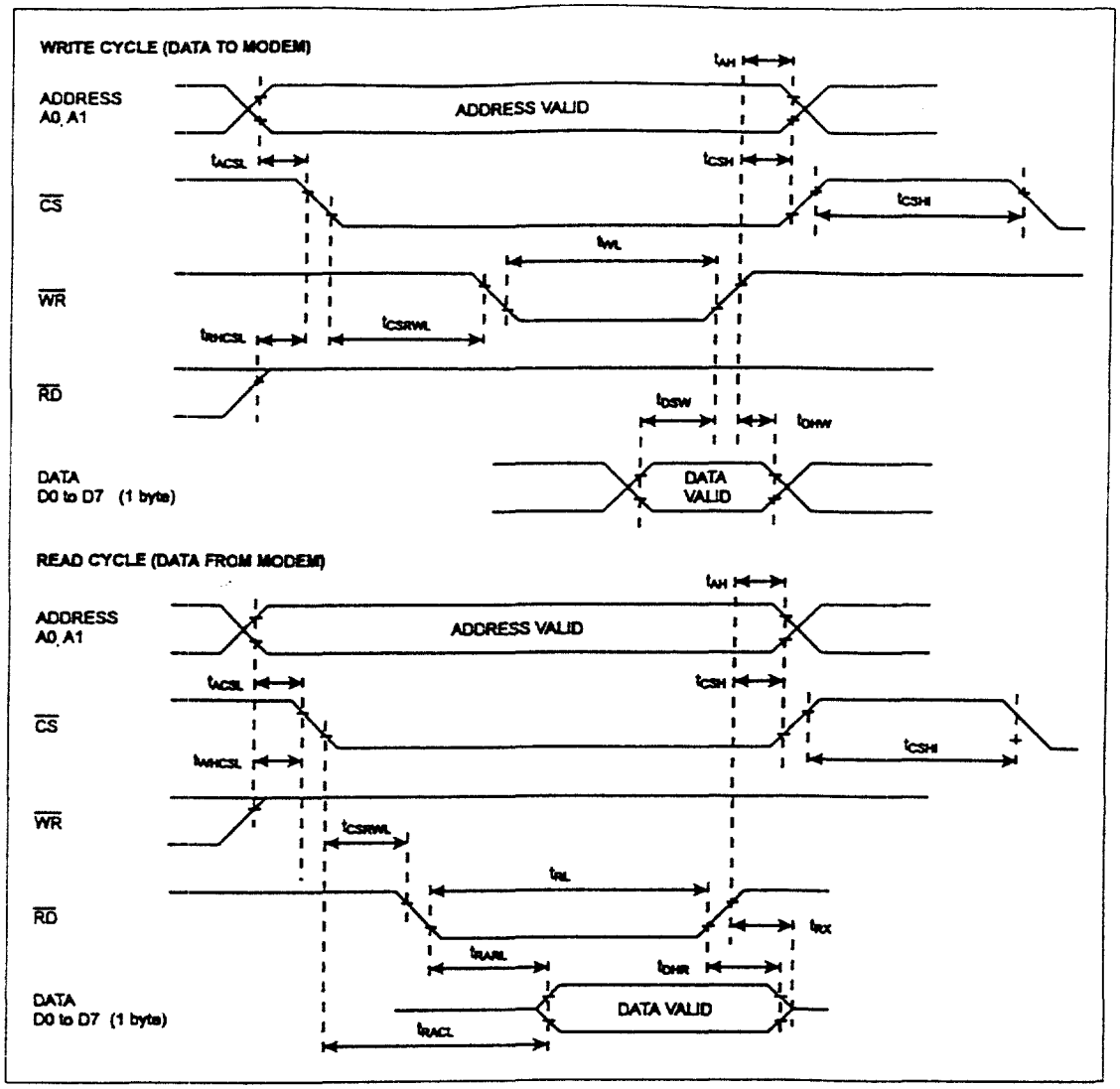


Figure 24: µC Parallel Interface Timings

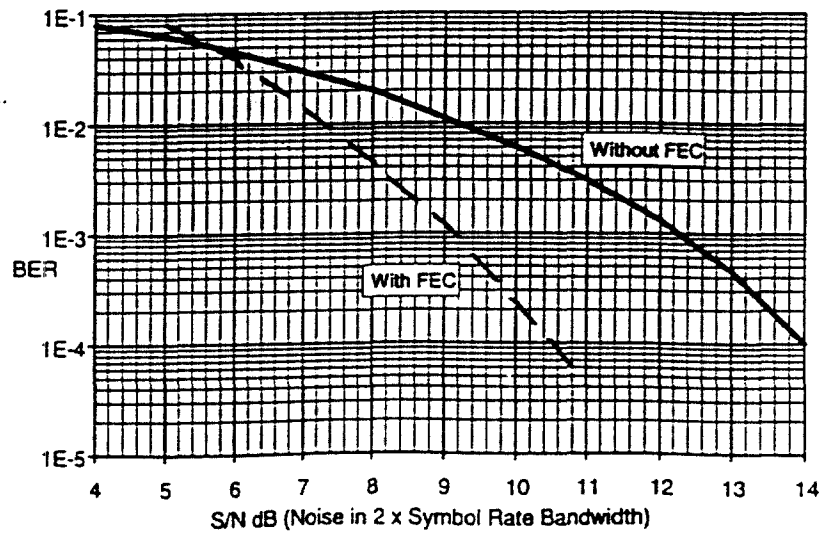
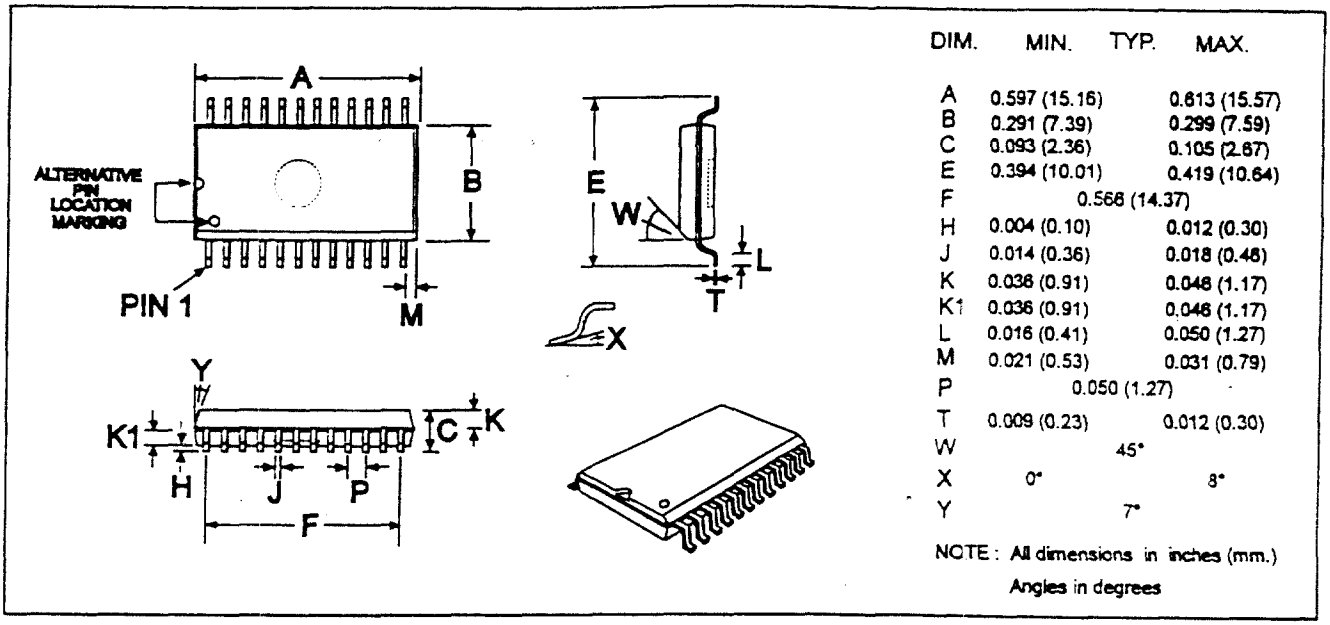


Figure 25: Typical Bit Error Rate With and Without FEC

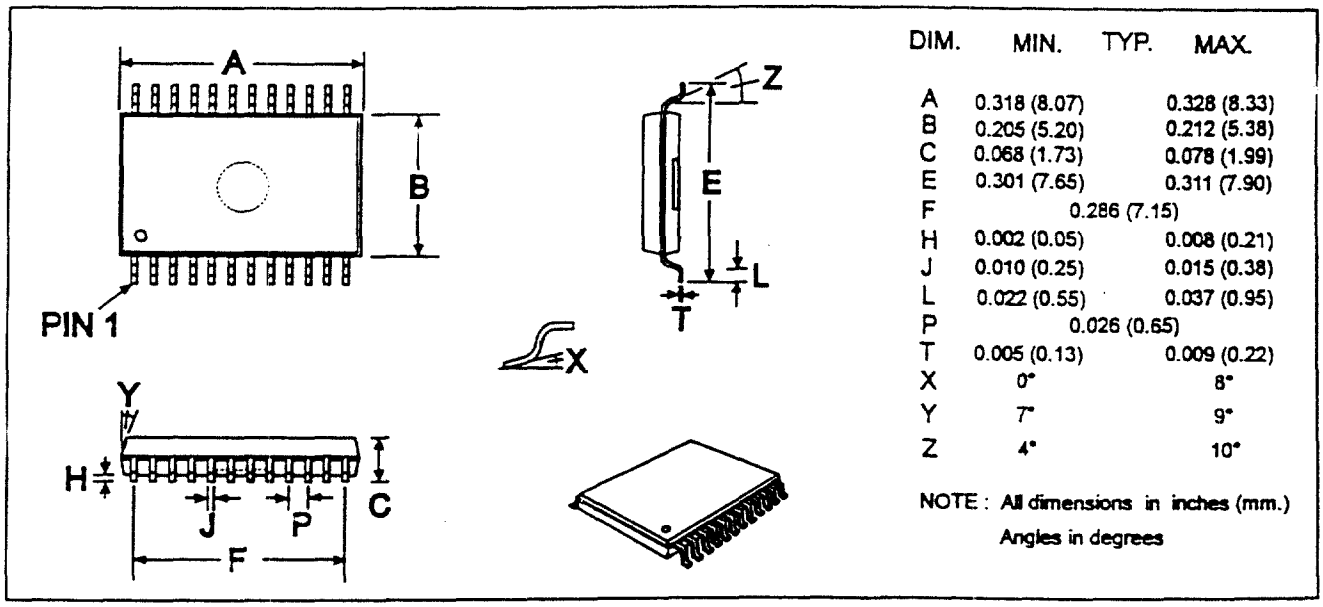
6.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

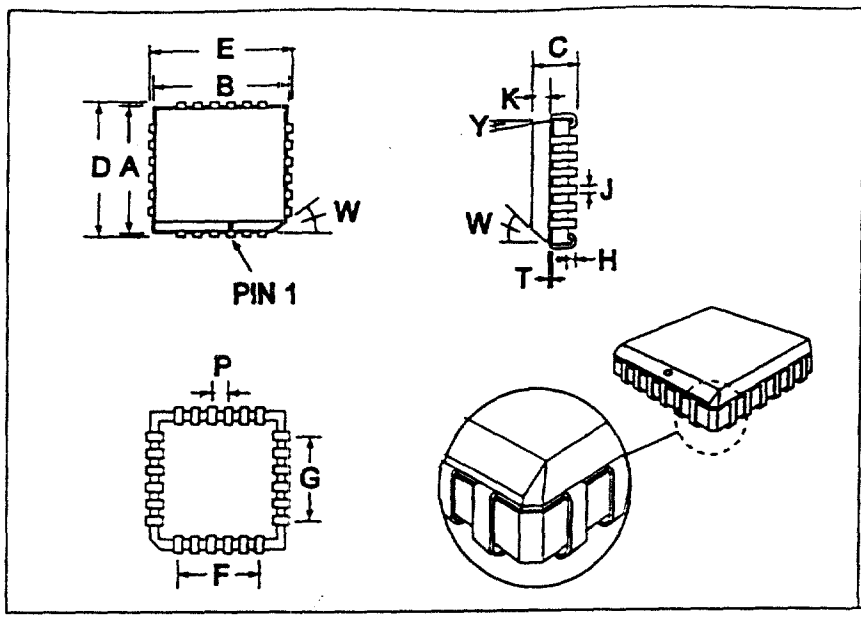
Figure 26: 24-pin SOIC Mechanical Outline : *Order as part no. MX929ADW*



DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 27: 24-pin SSOP Mechanical Outline : *Order as part no. MX929ADS*

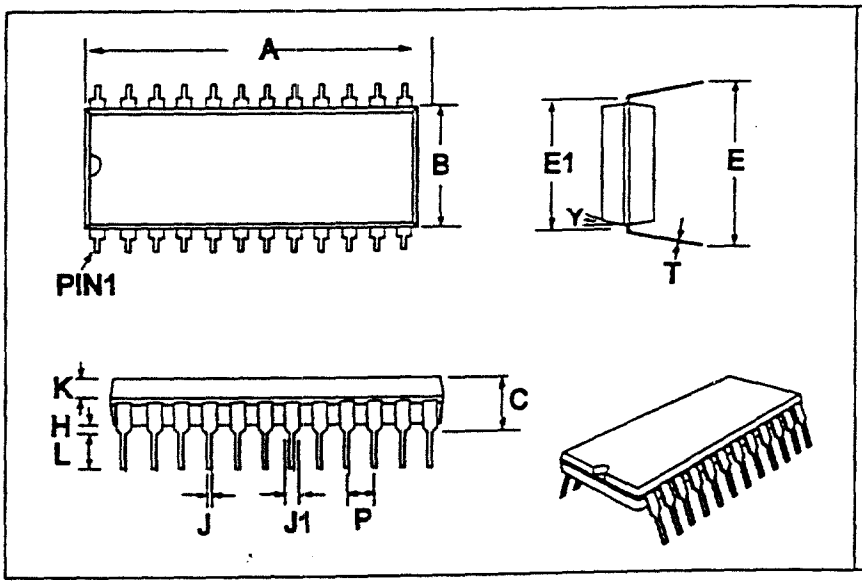


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.148 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 28: 24-pin PLCC Mechanical Outline : *Order as part no. MX929ALH*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 29: 24-pin PDIP Mechanical Outline : *Order as part no. MX929AP*

7. Errata

Coincident transitions of the $\overline{WR}$ signal and an internal clock can cause a newly written task to be ignored. In typical applications 1 out of 100,000 tasks may be ignored. Many users may never notice such an infrequent event, but to ensure that each task is loaded correctly, the software must check to see if the BFREE bit is low '0' immediately after every task set. Below is a recommended method for writing tasks.

- Procedure for writing RESET tasks:
  - Write the RESET task twice
- Procedure for writing NULL tasks with either of the Acquire bits set:
  - Write the NULL task twice
- Procedure for writing other tasks:
  - The µC should wait until the BFREE (Buffer Free) bit of the Status Register is '1' before writing the desired task to the Command Register.
  - Immediately after the task is written, the controlling device should check the value of the BFREE bit in the Status Register:
    - If BFREE = '0' then the task has been accepted.
    - If BFREE = '0' then the task needs to be rewritten to the Command Register

Note:

1. In Tx, the Data Buffer contents do not have to be rewritten if the task is not accepted.
2. In Rx, if either of the Acquire bits need to be set, then they will also have to be set in the repeated task.
3. Future revisions of this part will ensure that all newly written tasks will be accepted without requiring any task writes to be repeated.