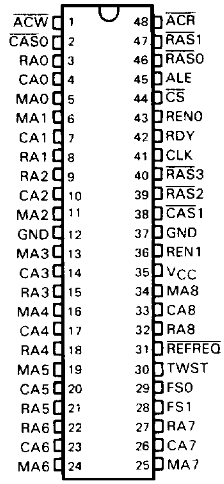
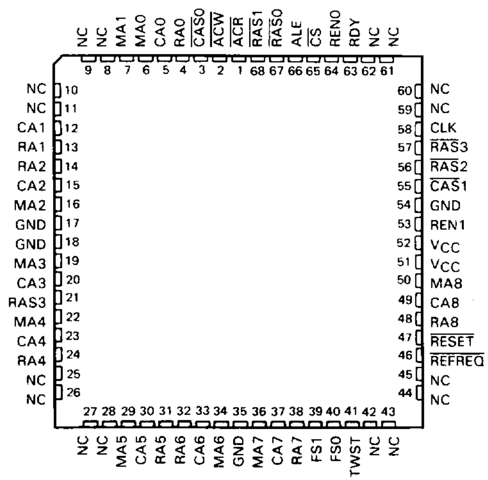
D2905, OCTOBER 1985

- Inputs are TTL- and CMOS-Voltage Compatible
- Controls Operation of 64K and 256K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 2 Megabytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
  - Asynchronous RESET Function Provided in FK and FN Packages
- High-Performance Si-Gate CMOS Technology
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- 3-State Outputs Allow Multiport Memory Configuration
- Performance Range: 125 ns ALE low to CAS low
- Compatible with TMS4500A/B and with VTI VL4500A and VL4502
- Available in Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

THCT4502 . . . JD OR N PACKAGE
(TOP VIEW)



THCT4502 . . . FK OR FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

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description

The THCT4502 is a monolithic DRAM system controller providing address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

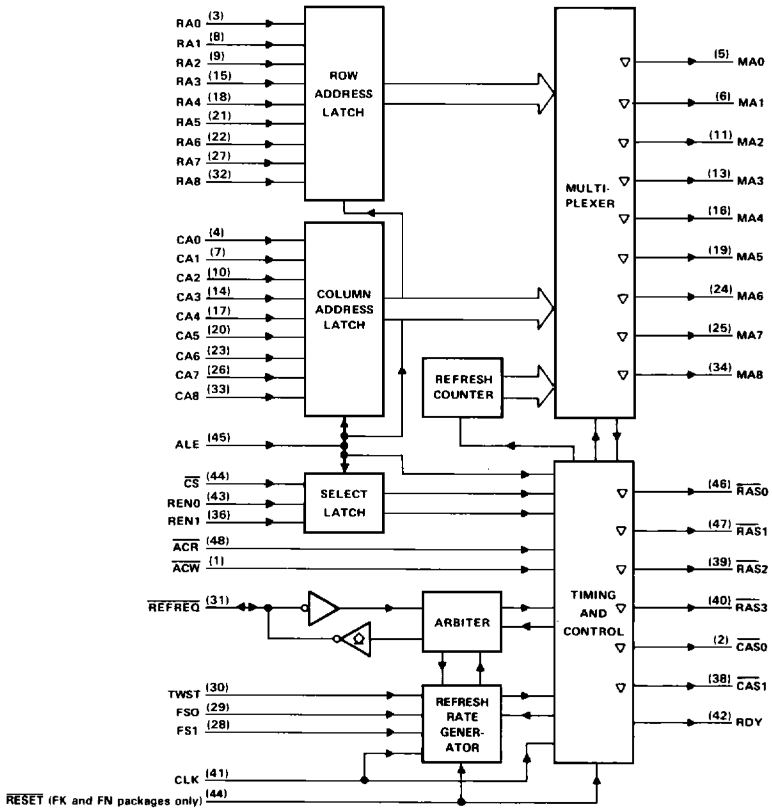
The controller contains an 18-bit multiplexer that generates the address lines for the memory device from the 18 system address bits and provides the strobe signals required by the memory to decode the address. A 9-bit refresh counter generates up to 512 row addresses required to refresh.

A refresh timer is provided to generate the necessary timing to refresh the dynamic memories and ensure data retention.

The THCT4502 also contains refresh/access arbitration circuitry to resolve conflicts between access requests and memory-refresh cycles.

The THCT4502 is characterized for operation from 0°C to 70°C.

functional block diagram



Pin numbers shown are for JD and N packages.

pin descriptions

RA0-RA8	Input	Row Address — These address inputs are used to generate the row address for the multiplexer.
CA0-CA8	Input	Column Address — These address inputs are used to generate the column address for the multiplexer.
MA0-MA8	Output	Memory Address — These three-state outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable — This input is used to latch the 18 address inputs, $\overline{CS}$, REN0, and REN1. This also initiates an access cycle if $\overline{CS}$ is low. The rising edge (low level to high level) of ALE returns all $\overline{RAS}$ outputs to the high level.
$\overline{CS}$	Input	Chip Select — A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
REN0, REN1	Inputs	$\overline{RAS}$ Enable 0 and 1 — These inputs are used to select one of four banks of RAM when $\overline{CS}$ is low. When REN1 is low, the lower banks are enabled via $\overline{CAS0}$, $\overline{RAS0}$, and $\overline{RAS1}$. When REN1 is high, the higher banks are enabled via $\overline{CAS1}$, $\overline{RAS2}$ and $\overline{RAS3}$. REN0 selects $\overline{RAS0}$ and $\overline{RAS2}$ when low, or $\overline{RAS1}$ and $\overline{RAS3}$ when high. (see Table 2).
$\overline{ACR}$, $\overline{ACW}$	Input	Access Control, Read; Access Control, Write — A low on either of these inputs causes the column address to appear on MA0-MA8 and a low-going pulse from $\overline{CAS}$. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by forcing $\overline{RAS}$ and $\overline{CAS}$ high. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0-MA8, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, $\overline{RAS3}$, $\overline{CAS0}$ and $\overline{CAS1}$ go into a high-impedance (floating) state.
CLK	Input	System Clock — This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, and FS0 inputs.
$\overline{REFREQ}$	Input	Refresh Request — This input should be driven by an open-collector or open-drain output. On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle is in progress and the current refresh address is present on MA0-MA8. (Note: $\overline{REFREQ}$ contains an internal active pullup with a nominal resistance of 10 kΩ, which is disabled when $\overline{REFREQ}$ is low).
$\overline{RAS0}$, $\overline{RAS1}$ $\overline{RAS2}$, $\overline{RAS3}$	Output	Row Address Strobe — These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN0 and REN1. On refresh, all $\overline{RAS}$ signals are active.
$\overline{CAS0}$, $\overline{CAS1}$	Output	Column Address Strobe — These three-state outputs are used to latch the column address into the DRAM array.
RDY	Output	Ready — This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.

pin descriptions (continued)

TWST	Input	Timing/Wait Strap — A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing or initialize the controller.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 — These are strap inputs to select Mode and Frequency of operation as shown in Table 1.
$\overline{RESET}$†	Input	$\overline{RESET}$ — Active-low input to initialize the controller asynchronously. Refresh Address is set to IFF_{16}, internal refresh requests, synchronizer, and frequency divider are cleared. (Note: $\overline{RESET}$ contains an internal pullup resistor with a nominal resistance of 100 kΩ, which allows this pin to be left open.)

†This function is available only in the FK and FN packages.

TABLE 1. STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLOCK FREQUENCY (MHz)	REFRESH FREQUENCY (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	–	REFREQ	4
L	L	H	0	EXTERNAL	–	REFREQ	3
L	H	L	0	CLK ÷ 61	3.904	64-95‡	3
L	H	H	0	CLK ÷ 91	5.824	64-88§	4
H	L	L	1	CLK ÷ 61	3.904	64-95‡	3
H	L	H	1	CLK ÷ 91	5.824	64-75‡	4
H	H	L	1	CLK ÷ 106	6.784	64-73‡	4
H	H	H	1	CLK ÷ 121	7.744	64-83¶	4

† This strap configuration resets the Refresh Timer Circuitry.
‡ Upper figure in refresh frequency is the frequency that is produced if the minimum clock frequency of the next select state is used.
§ Refresh frequency if clock frequency is 8 MHz.
¶ Refresh frequency if clock frequency is 10 MHz.

TABLE 2. OUTPUT STROBE SELECTION

CONTROL INPUT		SELECTED OUTPUT					
REN1	REN0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$	$\overline{CAS1}$
L	L	X				X	
L	H		X			X	
H	L			X			X
H	H				X		X

NOTE: Changing the logic value of REN1 after a low-to-high transition of ALE and before $\overline{ACX}$ rises causes the other $\overline{CAS}$ to fall. Both $\overline{CAS}$ signals remain low until $\overline{ACX}$ rises.

functional description

The THCT4502 consists of six basic blocks: address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

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address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0-MA8 follows the inputs RA0-RA8.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1, and FS0 are low. The configuration straps allow the matching of memories to the system access time. Upon power-up it is necessary to provide a reset signal by driving all three straps to the controller (or $\overline{\text{RESET}}$ for devices in the FK and FN packages only) low. A systems power-on reset ($\overline{\text{RESET}}$) can be used to do this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. A low-to-high transition on TWST sets the refresh counter to $1FF_{16}$ (511_{10}).

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 18 multiplexed addresses on nine lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (See Note 1)	−1.5 V to 7 V
Input diode current, I_{IK} ($V_I < 0$, $V_I > V_{CC}$)	±20 mA
Output diode current, I_{OK} ($V_O < 0$, $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: FK or JD package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FN or N package	260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+0.5$	V
V_{IL}	Low-level input voltage	−0.5†		0.8	V
V_O	Output voltage	−0.5		$V_{CC}+0.5$	V
t_t	Input transition (rise and fall) time	0		500	ns
T_A	Operating free-air temperature	0		70	°C

† The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	TYP	MAX	MIN	MAX	UNIT
V_{OH} High-level output voltage	MA0–MA8, $\overline{\text{RAS0}}$–$\overline{\text{RAS3}}$, $\overline{\text{CAS0}}$–$\overline{\text{CAS1}}$	I_{OH} = −20 µA	4.5 V	4.4			4.4		V
		I_{OH} = −6 mA	4.5 V	3.86			3.76		
	RDY	I_{OH} = −20 µA	4.5 V	4.4			4.4		
		I_{OH} = −4 mA	4.5 V	3.86			3.76		
	$\overline{\text{REFREQ}}$	I_{OH} = −20 µA	4.5 V	4			3.8		
V_{OL} Low-level output voltage	RDY, $\overline{\text{REFREQ}}$	I_{OL} = 20 µA	4.5 V			0.1		0.1	V
		I_{OL} = 4 mA	4.5 V			0.32		0.37	
	MA0–MA8, $\overline{\text{RAS0}}$–$\overline{\text{RAS3}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$	I_{OL} = 20 µA	4.5 V			0.1		0.1	
		I_{OL} = 6 mA	4.5 V			0.32		0.37	
I_{IH} High-level input current except $\overline{\text{REFREQ}}$		V_I = 5.5 V	5.5 V			0.1		1	µA
I_{IL} Low-level input current	$\overline{\text{REFREQ}}$	V_I = 0	5.5 V			−5		−50	µA
	$\overline{\text{RESET}}$					−100		−250	
	All others					−0.1		−1	
I_{OZ}‡ Off-state output current (3-state outputs only)		V_O = 0 to 5.5 V	5.5 V			±5		±50	µA
I_{CC} Supply current		$V_I = V_{CC}$ or 0, I_O = 0	5.5 V			5		15	mA
ΔI_{CC}§ Supply current change		One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3	mA
C_i Input capacitance		V_I = 0, f = 1 MHz	5.5 V		5	10		10	pF

‡ This parameter, I_{OZ}, the high impedance-state output current, applies only for three-state outputs and transceiver I/O pins.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		THCT4502-125		UNIT
		MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		ns
$t_{w(CH)}$	CLK high pulse duration	45		ns
$t_{w(CL)}$	CLK low pulse duration	45		ns
$t_{AEL\text{-}CL}$	Time delay, ALE low to CLK starting low (see Note 1)	25		ns
$t_{CL\text{-}AEL}$	Time delay, CLK low to ALE starting low (see Note 1)	15		ns
$t_{CL\text{-}AEH}$	Time delay, CLK low to ALE	15		ns
$t_{w(AEH)}$	Pulse width ALE high	45		ns
$t_{AV\text{-}AEL}$	Time delay, address REN1, $\overline{CS}$ valid to ALE low	10		ns
$t_{AEL\text{-}AX}$	Time delay, ALE low to address not valid	15		ns
$t_{AEL\text{-}ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 3, 4, 5, and 6)	$t_{h(RA)}+30$		ns
$t_{ACH\text{-}CL}$	Time delay, $\overline{ACX}$ high to CLK low (see Notes 3 and 7)	30		ns
$t_{ACL\text{-}CH}$	Time delay, $\overline{ACX}$ low to CLK starting high (to remove RDY)	30		ns
$t_{RQL\text{-}CL}$	Time delay, $\overline{REFREQ}$ low to CLK starting low (see Note 8)	35		ns
$t_{w(RQL)}$	Pulse width $\overline{REFREQ}$ low	30		ns
$t_{w(ACL)}$	$\overline{ACX}$ low width (see Note 9)	120		ns
t_{reset}	Power-up reset	$4t_{cCLK}$		ns

NOTES:
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided as the refresh/access occurs on the trailing CLK edge.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after $t_{CL\text{-}AEH}$ will output the refresh address to MA0-MA7 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE, then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE, then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL\text{-}CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL\text{-}MAX}$ minimum.
7. The minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge, $t_{ACH\text{-}CL}$ also affects precharge time such that the minimum $t_{ACH\text{-}CL}$ should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for a cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).
9. The specification $t_{w(ACL)}$ is designed to allow a $\overline{CAS}$ pulse. This assures normal operation of the device in testing and system operation.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	THCT4502-125 MIN	THCT4502-125 MAX	UNIT
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	C_L = 180 pF		45	ns
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid	C_L = 360 pF		50	ns
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address	C_L = 360 pF		90	ns
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	C_L = 40 pF		40	ns
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low (see Note 10)	C_L = 360 pF	50	125	ns
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high	C_L = 180 pF		50	ns
$t_{ACL-MAX}$	Row address valid after $\overline{ACX}$	C_L = 360 pF	15		ns
$t_{MAV-CEL}$	Time delay, memory address valid to $\overline{CAS}$ starting low	C_L = 360 pF	0		ns
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (see Note 10)	C_L = 360 pF	40	100	ns
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high	C_L = 180 pF		55	ns
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high	C_L = 360 pF	5	45	ns
$t_{ACH-MAX}$	Column address valid after $\overline{ACX}$ high	C_L = 360 pF	10		ns
t_{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{ACX}$ low) (see Note 11)	C_L = 40 pF		60	ns
$t_{RFL-RFL}$	Time delay, $\overline{REFREQ}$ external till supported by $\overline{REFREQ}$ internal	C_L = 40 pF		35	ns
t_{CH-RFL}	Time delay, CLK high till $\overline{REFREQ}$ internal starting low	C_L = 40 pF		50	ns
t_{CL-MAV}	Time delay, CLK low till refrefresh address valid	C_L = 360 pF		100	ns
t_{CH-RRL}	Time delay, CLK high till refresh $\overline{RAS}$ starting low	C_L = 180 pF	10	60	ns
$t_{MAV-RRL}$	Time delay, refresh address valid till refresh $\overline{RAS}$ low	C_L = 180 pF	5		ns
t_{CL-RFH}	Time delay, CLK low to $\overline{REFREQ}$ starting high (3 cycle refresh)	C_L = 40 pF		70	ns
t_{CH-RFH}	Time delay, CLK high to $\overline{REFREQ}$ starting high (4 cycle refresh)	C_L = 40 pF		70	ns
t_{CH-RRH}	Time delay, CLK high to refresh $\overline{RAS}$ starting high	C_L = 160 pF	5	60	ns
t_{CH-MAX}	Refresh address valid after CLK high	C_L = 360 pF	10		ns

NOTES: 10. The falling edge of $\overline{CAS}$ occurs when both ALE low to $\overline{CAS}$ low time delay ($t_{AEL-CEL}$) and $\overline{ACX}$ low to $\overline{CAS}$ low time delay ($t_{ACL-CEL}$) have elapsed, i.e., if $\overline{ACX}$ goes low prior to ($t_{AEL-CEL} - t_{ACL-CEL}$) after the falling edge of ALE, the falling edge of $\overline{CAS}$ is measured from the falling edge of ALE ($t_{AEL-CEL}$). Otherwise, the access time increases and the falling edge of $\overline{CAS}$ is measured from the falling edge of $\overline{ACX}$ ($t_{ACL-CEL}$).

11. RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access $\overline{RAS}$ low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{ACX}$ goes low on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ low on access grant cycles (assuming $\overline{ACX}$ low).

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switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1) (continued)

PARAMETER		TEST CONDITIONS	THCT4502-125		UNIT
			MIN	MAX	
t_{CH-REL}	Time delay, CLK high till access $\overline{RAS}$ starting low	C_L = 180 pF		60	ns
t_{CL-CEL}	Time delay, CLK low to access $\overline{CAS}$ starting low (see Note 12)	C_L = 360 pF		100	ns
t_{CL-MAX}	Row address valid after CLK low	C_L = 360 pF	25		ns
$t_{REL-MAX}$	Row address valid after $\overline{RAS}$ low	C_L = 360 pF	25		ns
$t_{AEH-MAX}$	Column address valid after ALE high	C_L = 360 pF	10		ns
t_{dis}	Output disable time (3-state outputs)	C_L = 360 pF		125	ns
t_{en}	Output enable time (3-state outputs)	C_L = 360 pF		75	ns
$t_{CAV-CEL}$	Time delay, column address valid to $\overline{CAS}$ starting low after refresh (see Note 12)	C_L = 360 pF	0		ns
t_{CH-CEL}	Time delay, CLK high to access $\overline{CAS}$ starting low (see Note 13)	C_L = 360 pF		180	ns
$t_{t(CEL)}$	$\overline{CAS}$ fall time	C_L = 360 pF		20	ns
$t_{t(CEH)}$	$\overline{CAS}$ rise time	C_L = 360 pF		50	ns
$t_{t(REL)}$	$\overline{RAS}$ fall time	C_L = 180 pF		30	ns
$t_{t(REH)}$	$\overline{RAS}$ rise time	C_L = 180 pF		40	ns
$t_{t(MAV)}$	Address transition time	C_L = 180 pF		40	ns
$t_{t(RYL)}$	RDY fall time	C_L = 40 pF		20	ns
$t_{t(RYH)}$	RDY rise time	C_L = 40 pF		50	ns

NOTES: 12. The occurrence of $\overline{CAS}$ low is guaranteed not to occur until the column address is valid on MAX.

13. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low. (See Refresh Cycle Timing Diagram)

PARAMETER MEASUREMENT INFORMATION

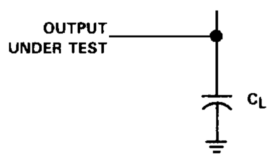
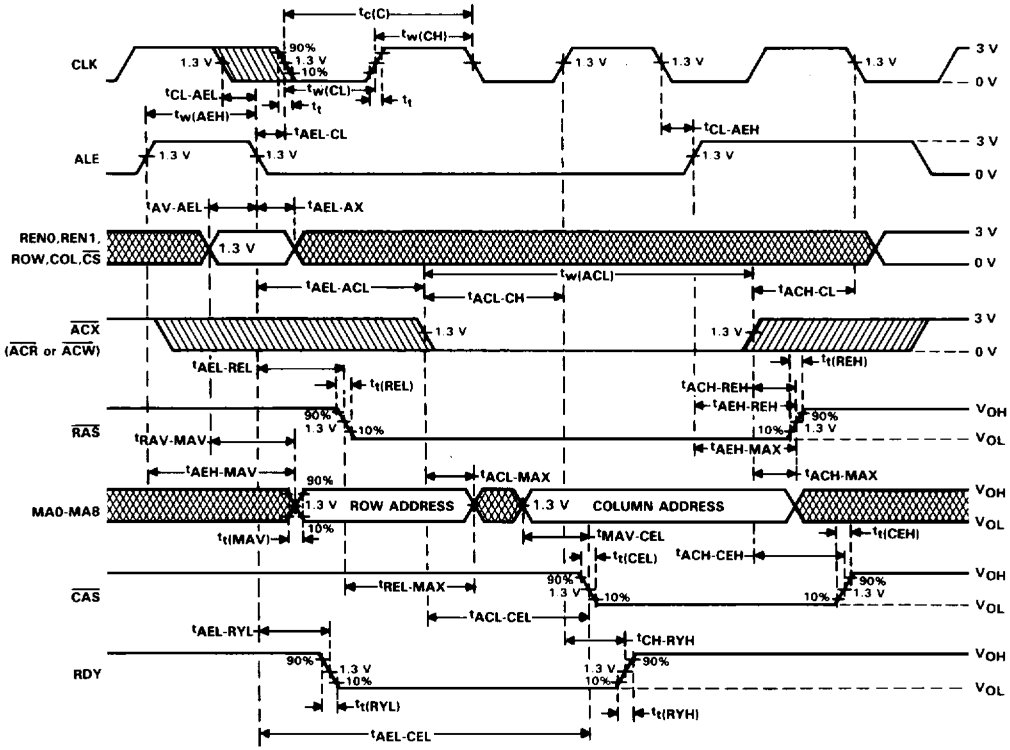


FIGURE 1. LOAD CIRCUIT



NOTE 14: All transition times (t_t) are measured between 10% and 90% points.

FIGURE 2. ACCESS CYCLE TIMING

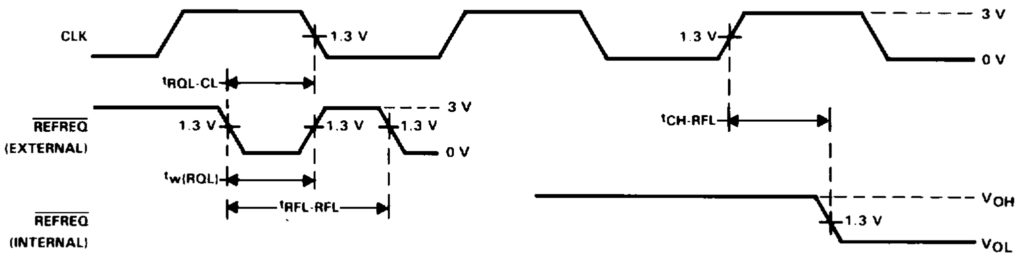


FIGURE 3. REFRESH REQUEST TIMING

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

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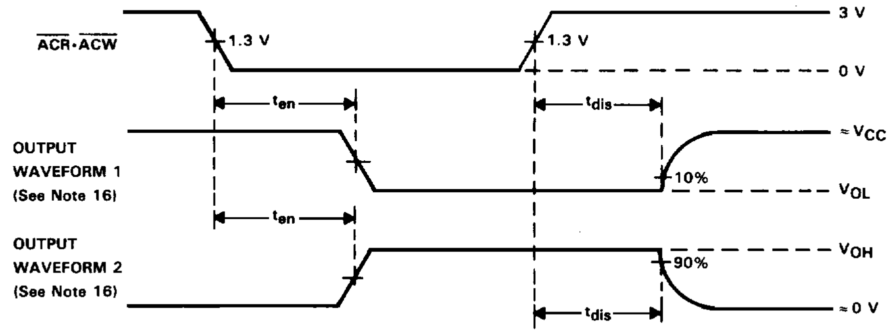
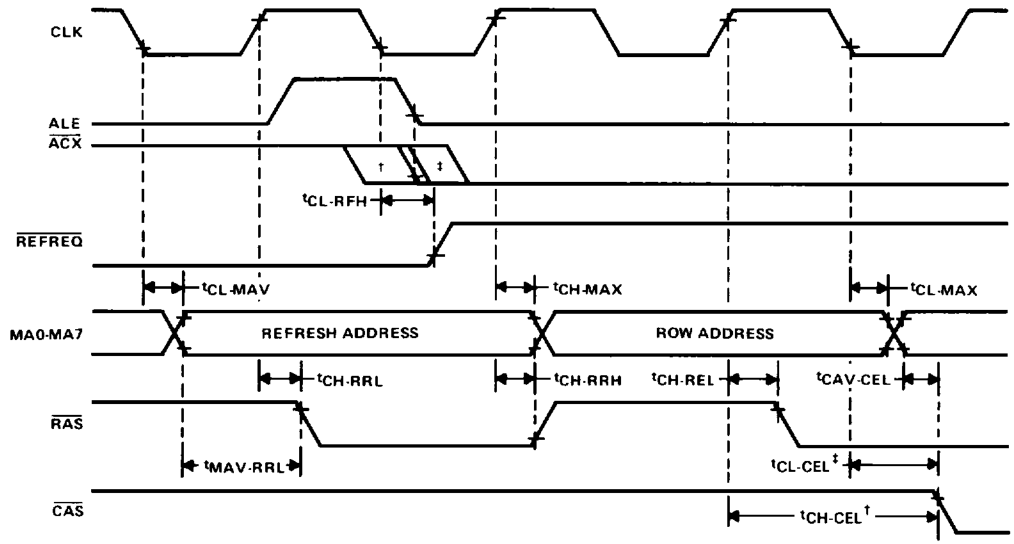


VOLTAGE WAVEFORMS

NOTE 16: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the access controls. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the access controls.

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

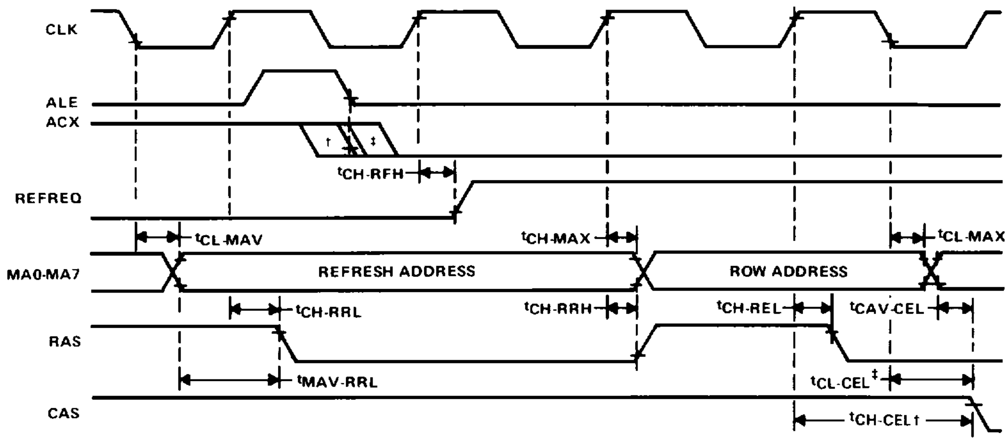


† On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK high transition ($t_{CH\text{-}CEL}$) if $\overline{ACX}$ low occurs prior to or coincident with the falling edge of ALE.

‡ On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK low transition ($t_{CL\text{-}CEL}$) if $\overline{ACX}$ low occurs 20 ns or more after the falling edge of ALE.

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 5. REFRESH CYCLE TIMING (THREE CYCLE)



† On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK high transition ($t_{CH\text{-}CEL}$) if $\overline{ACX}$ low occurs prior to or coincident with the falling edge of ALE.

‡ On access grant cycle following refresh, $\overline{CAS}$ low and address multiplexing are timed from CLK low transition ($t_{CL\text{-}CEL}$) if $\overline{ACX}$ low occurs 20 ns or more after the falling edge of ALE.

NOTE 15: All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50 Ω, t_r = 6 ns, t_f = 6 ns.

FIGURE 6. REFRESH CYCLE TIMING (FOUR CYCLE)

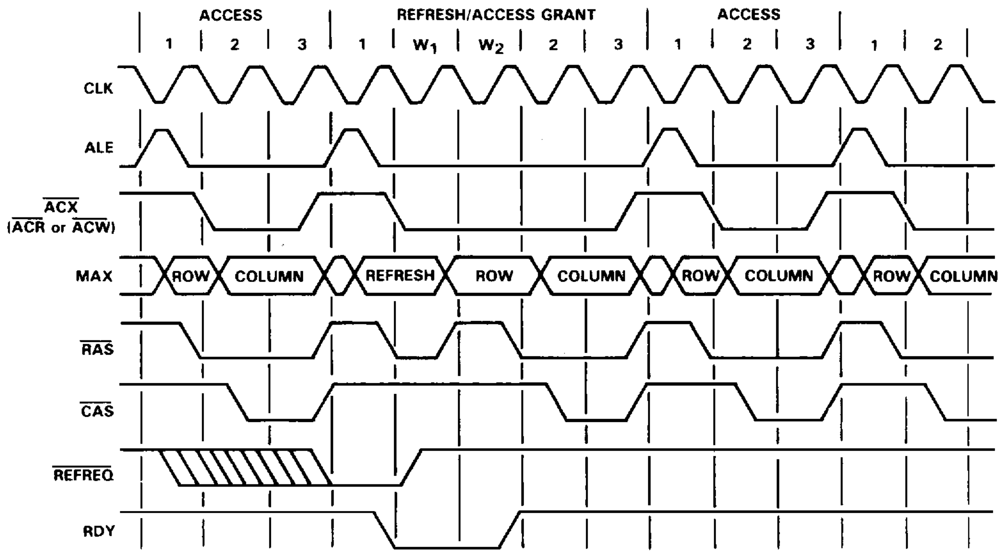


FIGURE 7. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS LOW)

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LSI Devices

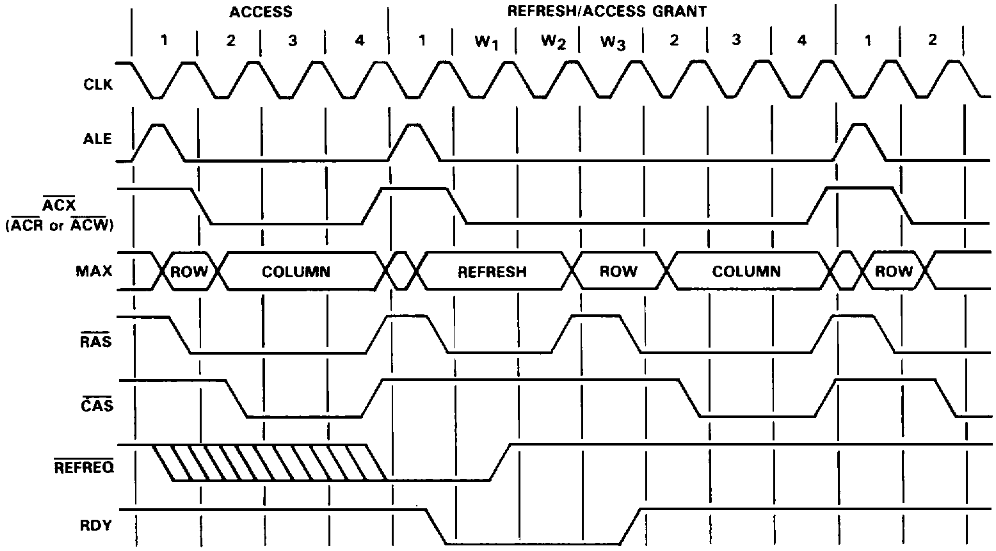


FIGURE 8. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS LOW)

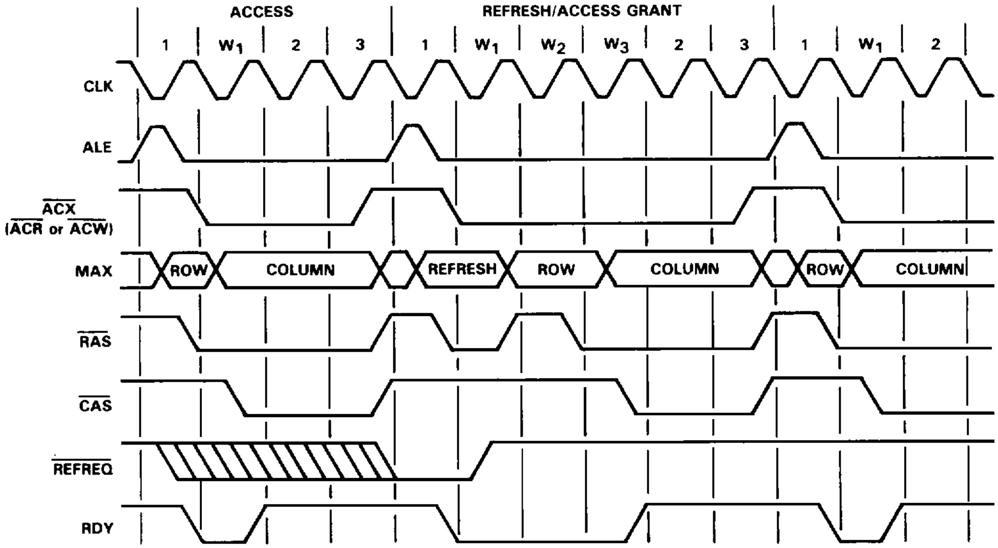


FIGURE 9. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (THREE-CYCLE, TWST IS HIGH)

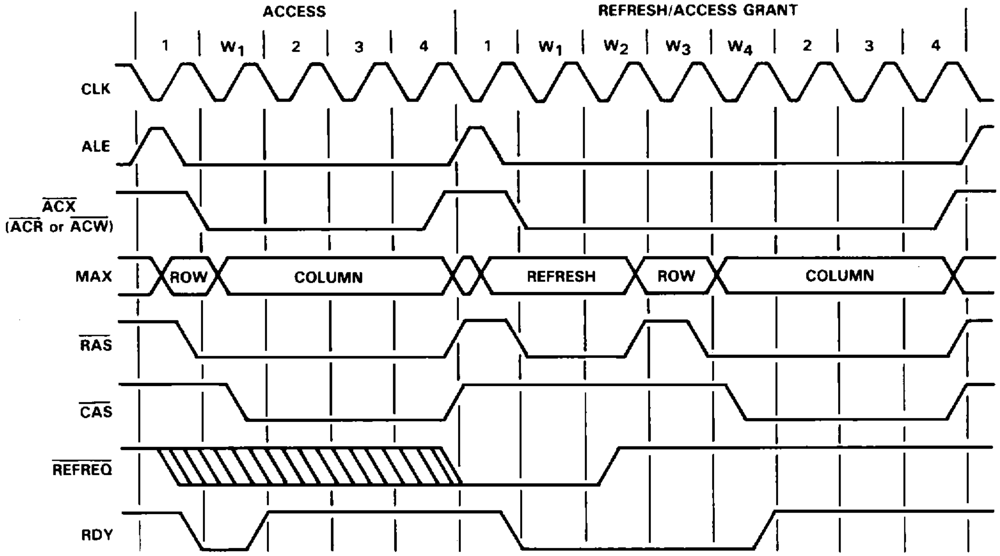
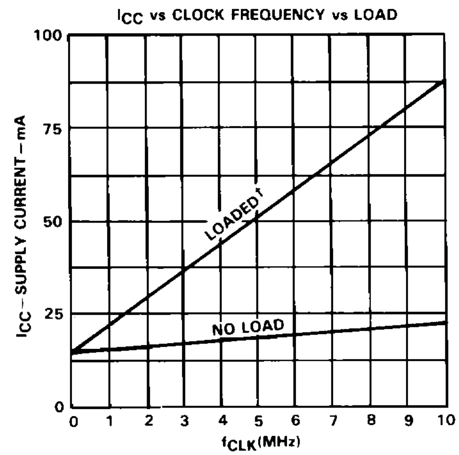


FIGURE 10. TYPICAL ACCESS/REFRESH/ACCESS CYCLE (FOUR-CYCLE, TWST IS HIGH)



†Load is 360 pF for $\overline{CAS}$ and MA outputs, 180 pF for all $\overline{RAS}$ outputs.

FIGURE 11.

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ORDERING INSTRUCTIONS

THCT 4502 — 125 JD

Prefix → THCT

Circuit Designator → 4502

Speed Selection → 125

−125 . . . 125 ns, ALE to $\overline{CAS}$ low

Package → JD

N, JD (Dual in-line packages)
FK, FN (Chip carrier packages)