FEATURES

- **Adaptive Equalizer with Line Compensation Loop Control**
- **Complies with ATM Forum STS-3 Twisted Pair Specifications**
- **Transmitter output disable option for quiet line**
- **Supports up to 100 meters of Shielded Twisted Pair or Category 5 Unshielded Twisted Pair Cable**
- **32-pin surface mount package (PLCC or TQFP)**
- **Pin-for-pin compatible with the Micro Linear ML6672**

APPLICATIONS

- **ATM over copper (TP-PMD)**

DESCRIPTION

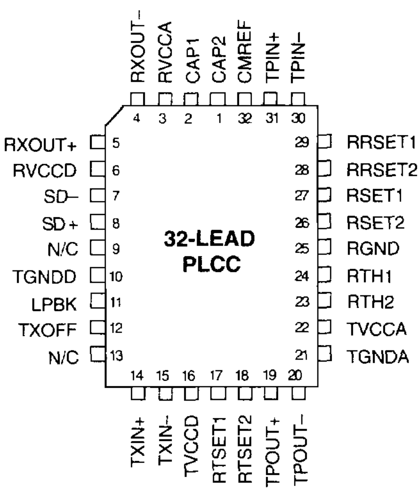
Synergy's SY67672 is a transceiver with an adaptive equalizer for 155 MBaud NRZ/NRZI encoded data present in ATM applications. Supporting category 5 shielded and Unshielded Twisted Pair cable, the SY67672 will compensate line losses for up to 100 meters of UTP in compliance with ATM Forum 155 Mbps Twisted Pair Specifications.

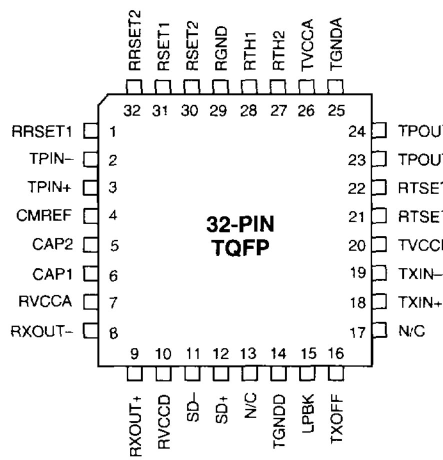
The SY67672 is manufactured in Synergy's high-performance, highly reliable ASSET technology and is pin compatible with the Micro Linear ML6672. The receive section contains an adaptive equalizer with line compensation feedback control incorporating a filter and control signal detection block. An ECL compatible buffer is employed in the final stage for direct interface (100K ECL) to various Synergy Clock Recovering Transceiver PHY standard products such as the SY69743 or SY69952.

The transmit section of the SY67672 is also100K ECL compatible and the transmit output level is externally controlled by a single RTSET resistor, and directly drives the line transformer.

Additional functions include a common-mode reference to set the input DC level for the equalizer and near-end transformer winding. The transmitter output driver can be disabled for true quiet line performance.

PIN CONFIGURATION





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BLOCK DIAGRAM

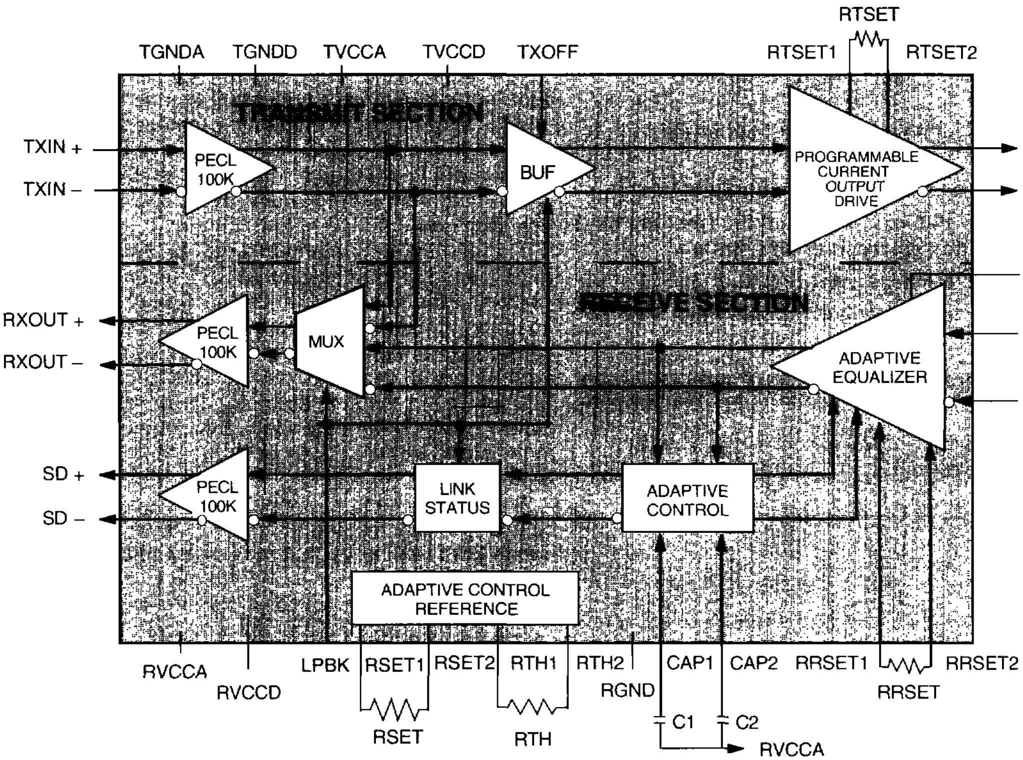

Figure 1. ATM UTP Transceiver Block Diagram

PIN NAMES

TXIN+, TXIN–

These differential ECL100K compatible inputs receive NRZ data from the PHY for transmission.

TPOUT+, TPOUT–

Outputs from NRZ buffer drive these differential current outputs. The transmitter filter/transformer module connects the media to these pins.

$\overline{\text{LPBK}}$

This TTL input enables transmitter-receiver loopback internally when asserted low.

$\overline{\text{TXOFF}}$

This TTL input forces the NRZ buffer to a quiet state when asserted low.

RTSET1, RTSET2

An external 1% resistor connected between these pins controls the transmitter output current amplitude.
$I_{OUT} = 64 \times 1.25V/RTSET$

TVCCA, TVCCD

Separate analog and digital transmitter power supply pins help to isolate sensitive circuitry from noise generating digital functions. Both supplies are nominally +5 volts.

TGNDA, TGNDD

Analog and digital transmitter grounds provide separate return paths for clean and noisy signals.

SD+, SD–

These differential ECL 100K compatible outputs indicate the presence of a data signal with an amplitude exceeding a preset threshold.

TPIN+, TPIN–

NRZ encoded data from the receiver filter/transformer module enters the receiver through these pins.

RXOUT+, RXOUT–

Differential ECL 100K compatible outputs provide NRZ encoded data to the PHY.

CAP1, CAP2

Two external capacitors connected to these pins sets the time constant for the adaptation in the equalizer loop as well as for signal detect response.

RRSET1, RRSET2

Internal time constants controlling the equalizer's transfer function are set by an external resistor connected across these pins.

CMREF

This pin provide a DC common mode reference point for the receiver inputs.

RVCCA, RVCCD

Analog and digital supply pins are separated to isolate clean and noisy circuit functions. Both supplies are nominally +5 volts.

RGND

Receiver ground.

RSET1, RSET2

An external 5KΩ resistor across these pins sets up an internal reference current.

RTH1, RTH2

An external resistor connected across these pins sets the internal levels for equalization as well as signal detect. This resistor allows compensation for transmit and magnetics variations. RTH should be set to match the peak-to-peak transmit amplitude. $V_{AMP} = 16 \times 1.25V \times RTH/RSET$ where V_{AMP} is the peak-to-peak amplitude of the transmit output with zero length cable.

OTHER

N/C No Connect

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply Voltage Range	-0.3V to 6V	V
V_I	Input Voltage Range Digital Inputs	-0.3V to V_{CC}	V
I_{OUT}	Output Current TPOUT±, SD±, RXOUT± All other outputs	50 10	mA
T_{store}	Storage Temperature Range	-65°C to 150	°C

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
V_{CC}	Power Supply Voltage Range	5 ±5%	V
T_A	Operating Temperature Range	0 to 70	°C
RTSET RRSET RSET RTH	External Resistor Value External Resistor Value External Resistor Value External Resistor Value	4 ±1% 8 ±1% 5 ±1% 250 ±1%	kΩ kΩ kΩ Ω
CAP1 CAP2	External Capacitor Value	0.33 ±5%	µF

2

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = 5V ±5%, RTSET = 4.0KΩ, RTH = 250Ω

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current						
I_{CCRD}	Receiver Supply Current (digital)	—	67	—	mA	
I_{CCRA}	Receiver Supply Current (analog)	—	52	—	mA	
I_{CCTD}	Transmitter Supply Current (digital)	—	25	—	mA	
I_{CCTA}	Transmitter Supply Current (analog)	—	6	—	mA	
I_{CCtot}	Transceiver Supply Current (total)	—	—	170	mA	
TTL Inputs ($\overline{TXOFF}$, $\overline{LPBK}$)						
V_{ILT}	Input LOW Voltage	—	—	0.8	V	
V_{IHT}	Input HIGH Voltage	2.0	—	—	V	
Differential Inputs (TPIN±, TXIN±)						
V_{ICM}	TPIN+, TPIN– Common Mode Input Voltage	2.2	—	V_{CC}	V	
V_{ID}	TPIN+, TPIN– Differential Input Voltage	—	—	1.5	V	
R_{ID}	TPIN+, TPIN– Differential Input Resistance	10.0K	—	—	Ω	
I_{ICM}	TPIN+, TPIN– Common Mode Input Current	—	—	+10	µA	
V_{IHE}	TXIN+, TXIN– Input Voltage HIGH	V_{CC} – 1.165	—	V_{CC} – 0.88	V	
V_{ILE}	TXIN+, TXIN– Input Voltage LOW	V_{CC} – 1.810	—	V_{CC} – 1.475	V	
I_{ILE}	TXIN+, TXIN– Input Current LOW	0.5	—	—	µA	
I_{IHE}	TXIN+, TXIN– Input Current HIGH	—	—	50	µA	
Differential Outputs (SD±, RXOUT±, TPOUT±)						
V_{OHE}	SD+, SD–, RXOUT+, RXOUT– Output Voltage HIGH(5)	V_{CC} – 1.025	—	V_{CC} – 0.88	V	
V_{OLE}	SD+, SD–, RXOUT+, RXOUT– Output Voltage LOW(5)	V_{CC} – 1.810	—	V_{CC} – 1.62	V	
I_{OH}	TPOUT+, TPOUT– Output Current HIGH(4)	19.0	—	21.0	mA	$V_{OUT} = V_{CC}$ ±0.5V
I_{OL}	TPOUT+, TPOUT– Output Current LOW(4)	—	—	0.5	mA	$V_{OUT} = V_{CC}$ ±0.5V
I_{Ooff}	TPOUT+, TPOUT– Output Current Offset(3)	—	—	0.5	mA	
I_{OAE}	TPOUT+, TPOUT– Output Amplitude Error(3),(4)	–5.0	—	+5.0	%	$V_{OUT} = V_{CC}$
I_{OVC}	TPOUT+, TPOUT– Output Voltage Compliance	–2.0	—	+2.0	%	$V_{OUT} = V_{CC}$ ±1.1V

NOTES:

1. Absolute maximum ratings are limited beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
3. Low duty cycle pulse testing is performed at T_A.
4. Output current amplitude is determined by I_{OUT} = 64 x 1.25V/RTSET.
5. Output voltage levels are specified when terminated by 50Ω to V_{CC} –2V or equivalent load.

AC ELECTRICAL CHARACTERISTICS

Transmitter Characteristics(2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$t_{TXr/f}$	TPOUT Rise/Fall Time (10% – 90%)	—	2.0	—	ns	Figure 2
t_{TXpd}	Propagation Delay TXIN to TPOUT	—	2.1	—	ns	Figure 2
t_{TXon}	TXOFF disabled to TPOUT	—	3.2	—	ns	Figure 3
t_{TXoff}	TXOFF enabled to TPOUT	—	3.4	—	ns	Figure 3
t_{TXj}	TPOUT pk Total Jitter(7)	—	0.8	—	ns	
DCD_{TX}	Duty Cycle Distortion(8) Transmitter Output	—	0.1	—	ns	

Receiver Characteristics(2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$t_{RXr/f}$	RXOUT Rise/Fall Time (20% – 80%)	—	1.0	5.0	ns	Figure 4
t_{RXpd}	Propagation Delay TPIN to RXOUT(6)	—	3.0	—	ns	Figure 4
t_{SDon}	Signal detect turn on time TPIN to SD(9)	—	100	—	ns	Figure 5
t_{SDoff}	Signal detect turn off time TPIN to SD(9)	—	1000	—	ns	Figure 5
t_{RXj}	RXOUT pk Total Jitter(10)	—	2.0	—	ns	
DCD_{RX}	Duty Cycle Distortion(8) Receiver Output	—	0.1	—	ns	

Loopback Characteristics(2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{LBpd}	Propagation Delay TXIN to RXOUT	—	3.4	—	ns	Loopback enabled; Figure 6
t_{LBonRX}	LPBK enabled to RXOUT	—	3.6	—	ns	TPIN not switching; Figure 7
$t_{LBoffRX}$	LPBK disabled to RXOUT	—	3.6	—	ns	TPIN not switching; Figure 7
t_{LBonTX}	LPBK disabled to TPOUT	—	4.5	—	ns	Figure 7
$t_{LBoffTX}$	LPBK enabled to TPOUT	—	5.2	—	ns	Figure 7
t_{LBonSD}	LPBK enabled to SD	—	3.2	—	ns	TPIN not switching; Figure 7
$t_{LBoffSD}$	LPBK disabled to SD	—	3.2	—	ns	TPIN not switching; Figure 7

NOTES:

1. Absolute maximum ratings are limited beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.
2. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
3. Low duty cycle pulse testing is performed at T_A.
4. Output current amplitude is determined by I_{OUT} = 64 x 1.25V/RTSET.
5. Output voltage levels are specified when terminated by 50Ω to V_{CC} –2V or equivalent load.
6. tRXpd is measured by applying a 1V p-p 62.5MHz square wave to the TPIN± inputs.
7. TX Jitter measurements are made differentially at the TPOUT± current outputs using PRBS 2^{23} pattern. All measurements are referenced to the original transmit clock.
8. Duty cycle distortion is measured as the time difference from an ideal signal with 16ns pulse width.
9. Signal Detect turn on and turn off times are measured using 1V p-p 2^{23} pseudo random bit stream over a length of Category 5 UTP cable ≤ 100 meters.
10. RX Jitter measurements are made differentially at the RXOUT± PECL outputs using PRBS 2^{23} pattern. This test includes data transmission over a 100m Category 5 UTP cable. All measurements are referenced to the original transmit clock.

AC ELECTRICAL CHARACTERISTICS (continued)

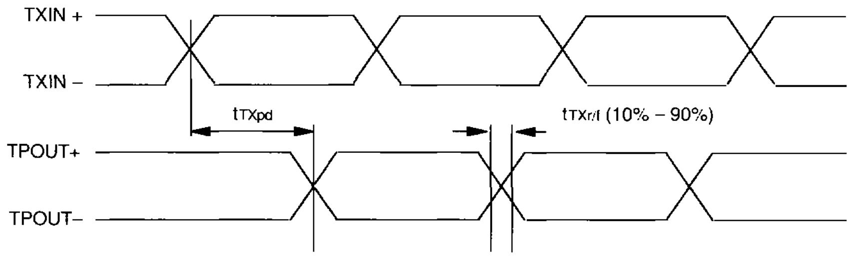

Figure 2. TX – Timing

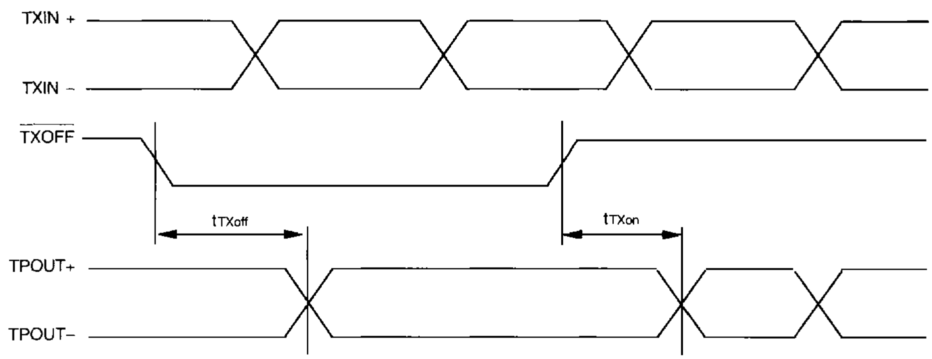

Figure 3. TXOFF – Timing

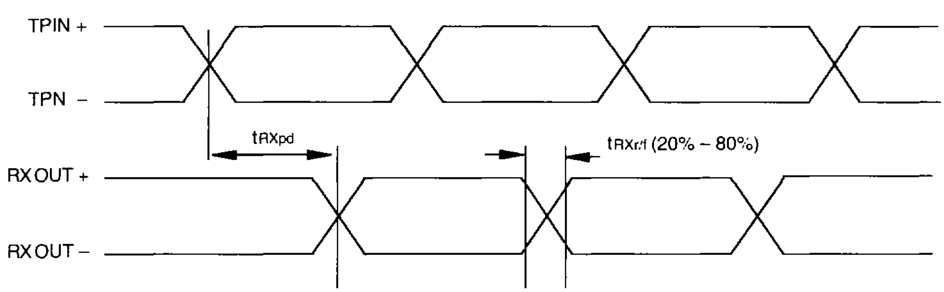

Figure 4. RX – Timing

AC ELECTRICAL CHARACTERISTICS (continued)

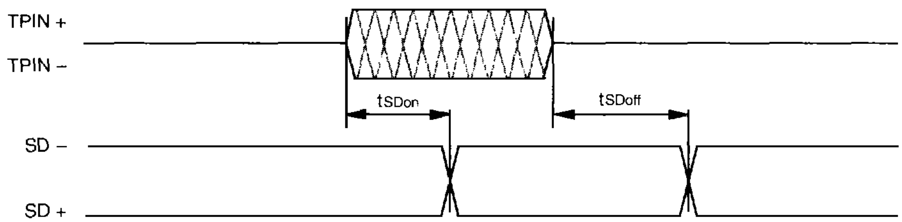

Figure 5. Signal Detect Timing

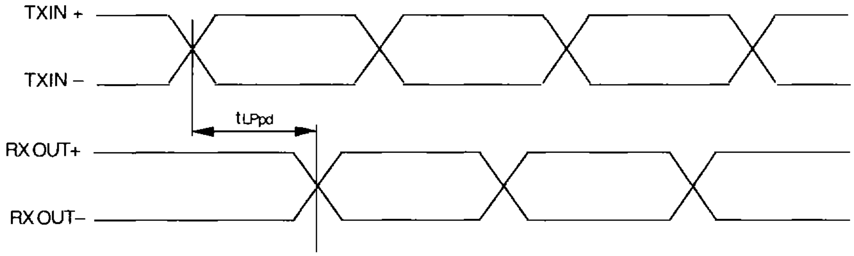

Figure 6. RX – Timing (Loopback)

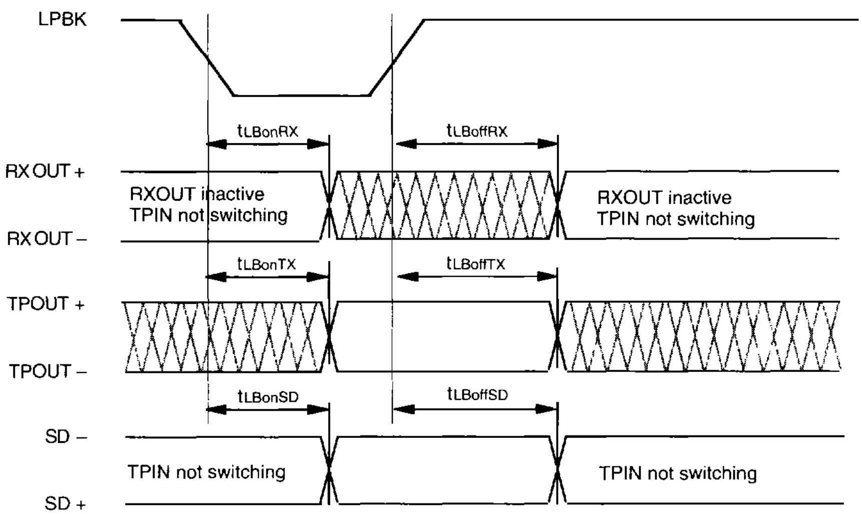

Figure 7. Loopback Timing

FUNCTIONAL DESCRIPTION

The SY67672 transceiver is a physical media dependent transceiver that allows the transmission and reception of 155Mbps data up to 100 meters over shielded twisted pair cable or category 5 unshielded twisted pair cable.

The transmit section accepts NRZ data, sending the information on a two pin current driven transmitter. The transmitted output passes through an external low pass filter and transformer before entering the connectors to the STP or UTP cable. The output amplitude of the transmitted signal is programmable through the external RTSET resistor.

The receive section accepts NRZ coded data after it passes through an isolation transformer and band limiting filter. The adaptive equalizer is used to compensate for the amplitude and phase distortion incurred from the cable. The adaptive control section determines the cable length and adjusts the equalizer accordingly. As the input signal amplitude diminishes, the amount of equalization increases until it reaches its maximum of an equivalent 100 meters of category 5 cable.

The adaptive control block governs both the equalization level as well as the link detection status. The link detection threshold has a fixed relationship to the overall equalization level which is currently 25% of the transmitted amplitude. For the link status to be true, a minimum level signal must be received. When the input signal is small, the equalization will be at its maximum.

After the signal has been equalized, it is fed through the loopback multiplexer onto the RXOUT± pins.

Figure 8 shows a typical gain vs frequency plot of the adaptive equalizer for 0, 25, 50, 75 and 100 meter category 5 cable lengths.

Typical Equalizer Transfer Function

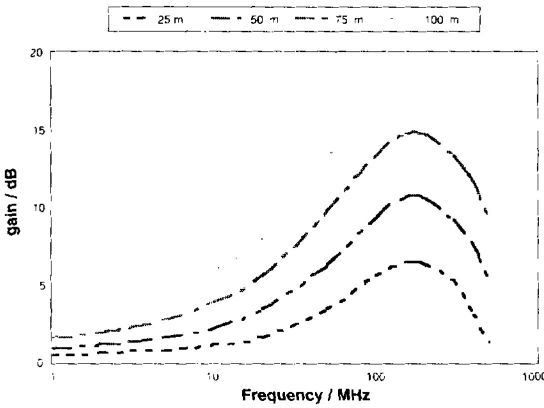

Figure 8. Equalization Range

TRANSMISSION

TRANSMISSION

PECL level scrambled NRZ data is received by the SY67672 and the current driven transmitter then sends the data to the filter/transformer module. The transmit amplitude is controlled by one external resistor, RTSET.

$$\text{IOUT} = \frac{64 \times 1.25\text{V}}{\text{RTSET}}$$

For ATM UTP applications the transmit amplitude is 1V peak to peak. The termination at the transmitter output is 50Ω. Therefore, the transmit current IOUT = 1/50 = 20mA.

Therefore, RTSET = 64 x 1.25/20KΩ = 4KΩ

The transmitter may be disabled via the TXOFF pin.

ADAPTIVE EQUALIZATION

During transmission of data over UTP (unshielded twisted pair), distortion and ISI are caused by dispersion in the cable. Equalization is used to overcome this signal corruption. However, the distortion is frequency dependent and loop length dependent.

Therefore, in most practical cases, the TP port characteristic is unknown and it is impractical to tune the equalizer specifically to each individual port. Hence, adaptive equalization is used in the TP-PMD to ensure proper compensation of the received signal.

By using adaptive equalization, the receiver automatically compensates different lengths of cable without over equalizing or under equalizing the line. The SY67672 monitors the energy of the received signal to determine the cable length and adjust the equalizer accordingly. The input signal level is inversely proportional to the cable length. Therefore, as the signal level decreases, the amount of equalization is increased to compensate for the line loss.

RECEIVED CIRCUIT

After the data is received and equalized, it is then sent to the clock recovery circuit via the RXOUT pins. A resistor RTH is used to control the internal level of equalization.

$$V_{AMP} = \frac{16 \times 1.25\text{V} \times \text{RTH}}{\text{RSET}}$$

VAMP is the transmit voltage amplitude and is equal to 1V and RSET = 5KΩ. Therefore, RTH = 1 x 5/(16 x 1.25) KΩ = 250Ω.

CAP1 and CAP2 are capacitors used to set the time constant for adaptation of the equalizer loop and should be 0.33μF.

APPLICATION EXAMPLE

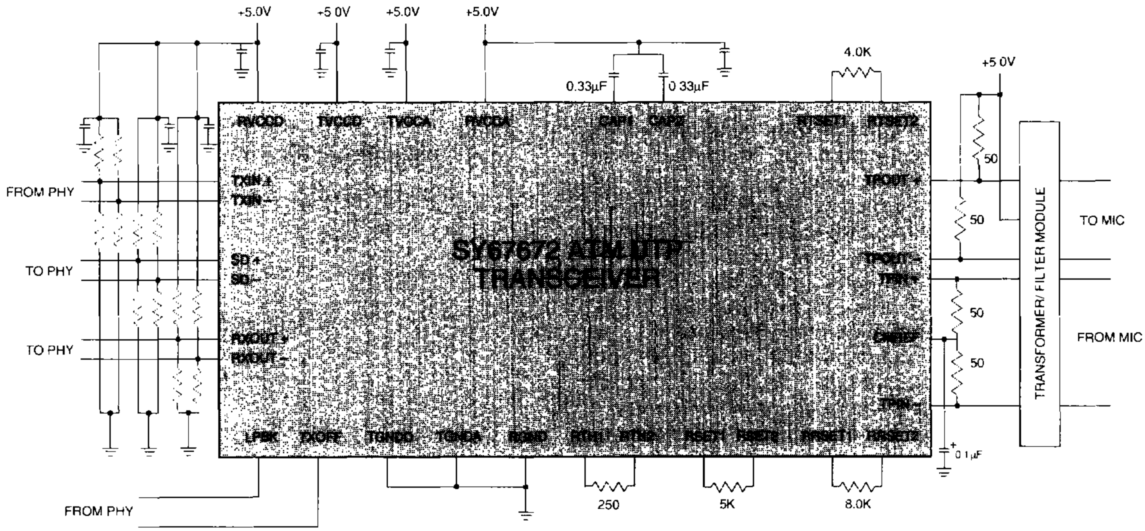

Figure 9. Application Example of SY67672
Configured for 1.0Vp.p Transmit Amplitude on C5 UTP.

NOTES:

1. Split 100K ECL terminations are 82Ω and 130Ω to Vcc and GND respectively.
2. Recommended power supply bypass capacitors are 0.1µF with optional 10µF tantalum in parallel.
3. Transformer turns ratio is 1:1.
4. LPBK and TXOFF inputs are active LOW.
5. Resistors 250Ω, 4.0K, 5.0K and 8.0K are ±1%.
6. Capacitors 0.33µF are ±5%.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY67672JC	J32-1	Commercial
SY67672TC	T32-1	Commercial