ANALOG DEVICES

Address Generator

ADSP-1410

FEATURES

16-Bit Addresses with Higher Precision Options
Look-Ahead™ Pipeline
80ns Cycle Time
20ns Clock-to-Address Delay
Versatile Addressing Hardware:
- **30 16-Bit Registers**
- **16-Bit ALU with Left/Right Shift & Carry I/O**
- **Comparator**
- **Bit Reverser**

Dual Ports
Powerful Single-Cycle Looping Instructions
Low-Power TTL-Compatible 1.5 Micron CMOS Technology
175mW Max Power Dissipation
48-Pin DIP (Ceramic or Low-Cost Plastic)

GENERAL DESCRIPTION

The ADSP-1410 is a fast, flexible address generator optimized for digital signal processors and general purpose computers. This low-power CMOS device rapidly generates the data memory addresses required by routines such as digital filters, FFTs, matrix operations, and DMAs.

The ADSP-1410's 10-bit microcode instructions include commands for looping, register read/writes, internal data transfers, and logical/shift operations. An internal Alternate Instruction Register (AIR) can also provide the instruction under external control, allowing microcode to be conserved in many applications.

In a single instruction cycle, the ADSP-1410 can:

- output a 16-bit memory address
- modify this memory address
- conditionally reinitialize the address based on a comparison with a preset value.

Consequently, circular buffers and modulo addressing of data memories can be implemented without overhead.

The ADSP-1410's architecture features a 16-bit ALU, a comparator, and 30 16-bit registers. The registers are organized into four files: sixteen address registers, six offset registers, four compare registers, and four initialization registers.

The ADSP-1410 has a 16-bit address (Y) port for outputting addresses and a 16-bit data (D) port for I/O between internal and external registers. A value provided by the data port may serve as an input to the 1410's ALU or may be directly output over the address port.

ORDERING INFORMATION

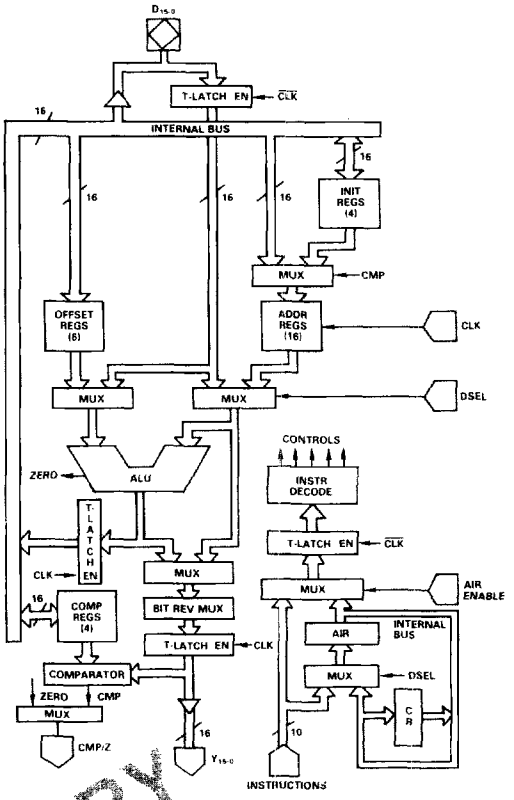
ADSP-1410TD/883B — Processing
— Package
— Performance, Temp. Range
— Part Number
Analog Devices Digital Signal Processing

Package
D – Ceramic DIP
N – Plastic DIP

Processing
Blank – Standard
+ – High Reliability
883B – MIL-STD-883

Performance/ Temperature
J – Standard, 0 to + 70°C
K – High Speed, 0 to + 70°C
S – Standard, – 55°C to + 125°C
T – High Speed, – 55°C to + 125°C

ADSP-1410 ADDRESS GENERATOR



The ADSP-1410's Look-Ahead pipeline eliminates the need for an external microcode pipeline register by internally latching instructions and addresses. A complementary latching arrangement allows a new instruction to be decoded (in preparation for the following cycle) while the data memory address for the current cycle is held constant.

Double-precision (30-bit), single-cycle addressing can be performed by cascading two ADSP-1410's. Alternatively, a single ADSP-1410 can provide one double-precision address every two clock cycles.

The ADSP-1410 is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Packaging options include a 48-pin ceramic DIP and a low cost 48-pin plastic DIP.

Look-Ahead is a trademark of Analog Devices, Inc.