Signetics

FAST 74F166
Shift Register

FAST Products

8-Bit Bidirectional Universal Shift Register
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F166	175MHz	50mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **Expandable to 16 bits in 8-bit increments**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F166N
16-Pin Plastic SO	N74F166D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

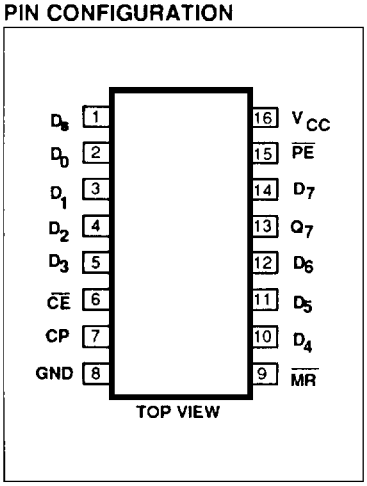
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_7	Parallel data inputs	1.0/0.033	20μA/20μA
D_S	Serial data input (Shift Right)	2.0/0.066	40μA/40μA
CP	Clock input (Active rising edge)	1.0/0.033	20μA/20μA
$\overline{CE}$	Clock Enable input (Active Low)	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel Enable input (Active Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (Active Low)	2.0/0.066	40μA/40μA
Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

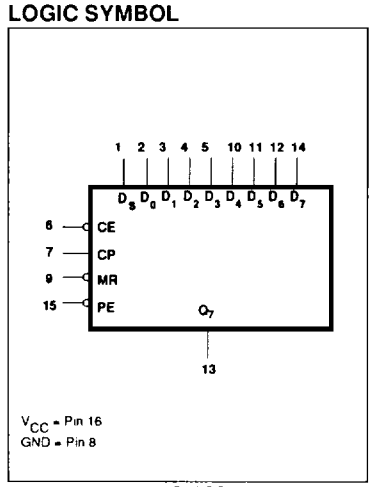
DESCRIPTION

The 74F166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active Low Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is Low one setup time before the Low-to-High clock transition, parallel data is entered into the register. When $\overline{PE}$ is High, data is entered into internal bit position Q_0 from serial data input (D_s), and the remaining bits are shifted one place to the right (Q_0-Q_1-Q_2, etc.) with each positive going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_s input of the succeeding stage. The clock input is gated OR structure which allows one input to be used as an active-Low Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The Low-to-High transition of $\overline{CE}$ input should only take place while the CP is High for predictable operation. A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a Low state.

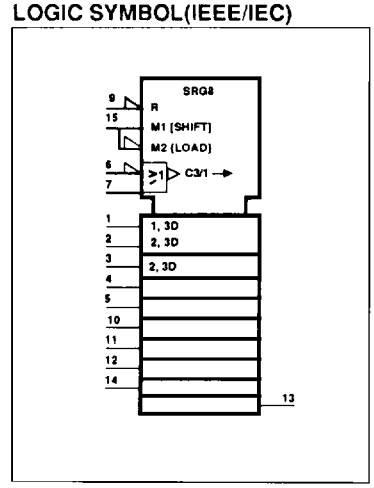
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

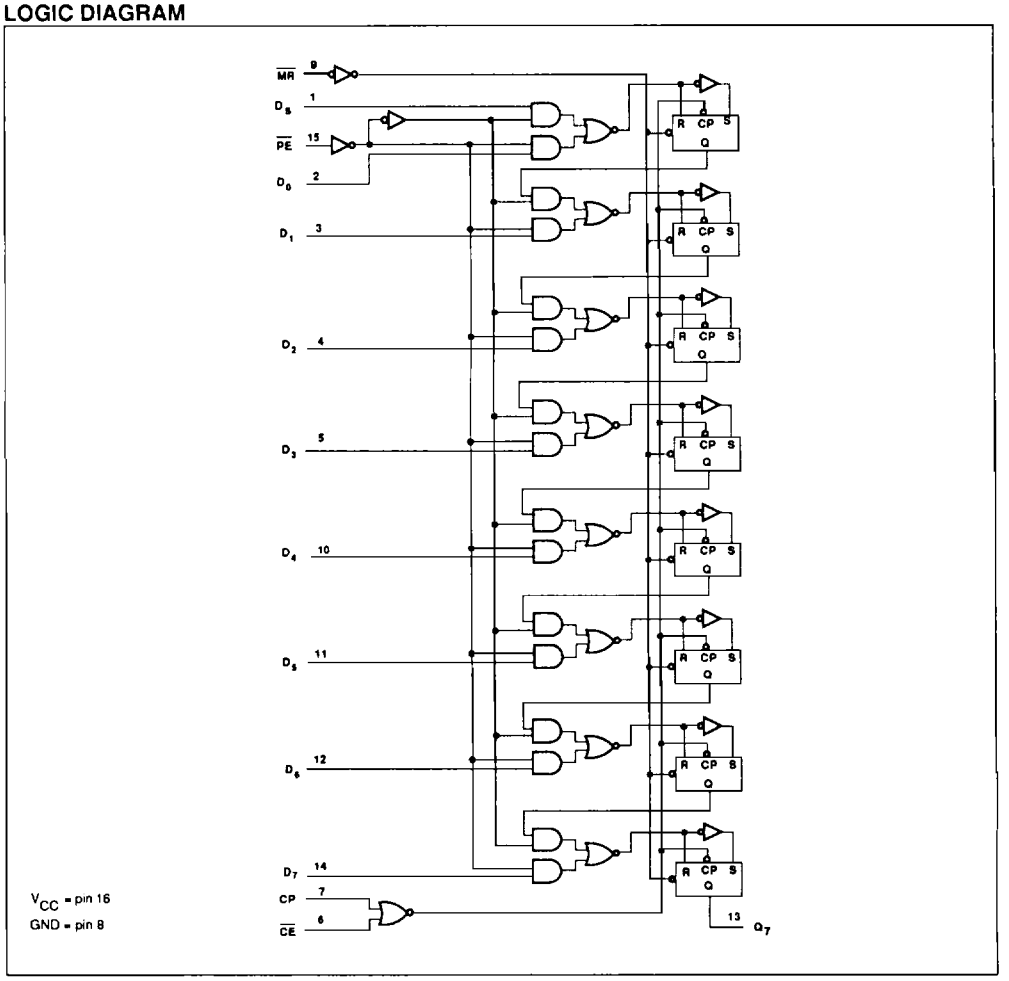


FUNCTION TABLE

INPUTS					Q_n REGISTER		OUTPUT	OPERATING MODE
$\overline{PE}$	$\overline{CE}$	CP	D_s	D_0 - D_7	Q_0	Q_1 - Q_6	Q_7	
l	l	↑	X	l - l	L	L - L	L	Parallel load
l	l	↑	X	h - h	H	H - H	H	
h	l	↑	l	X - X	L	q_0 - q_5	q_6	Serial shift
h	l	↑	h	X - X	H	q_0 - q_5	q_6	
X	h	X	X	X - X	q_0	q_1 - q_6	q_7	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		$\overline{CE}$, CP[3]						
I_{IH}	High-level input current	others	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{MR}$, D_s					40	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V				-20	µA
		$\overline{MR}$, D_s					-40	µA
I_{OS}	Short circuit output current[4]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{PE}$= $\overline{CE}$=D_n=GND, $\overline{MR}$=D_S=4.5V, CP=↑			50	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. When testing CP, $\overline{CE}$ must remain in High state, whereas CP must remain in High state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

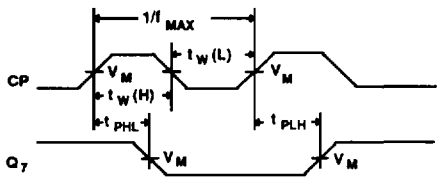
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	135	175		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	4.0	6.5	8.5	4.0	9.5	ns

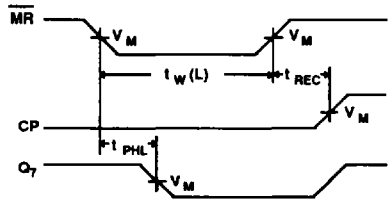
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n, D_s to CP, $\overline{CE}$	Waveform 3	3.0 2.5			4.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n ,D_s to CP	Waveform 3	0 0			1.0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_s to $\overline{CE}$	Waveform 3	1.5 0			2.0 0		ns
t_sL)	Setup time, Low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		ns
$t_h(H)$	Hold time, High $\overline{CE}$ to CP	Waveform 3	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.5			3.5 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

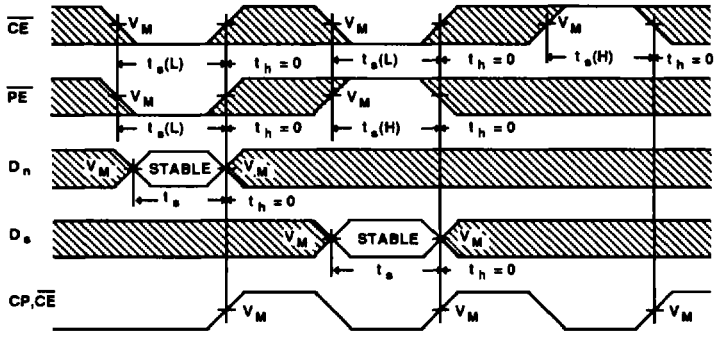
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



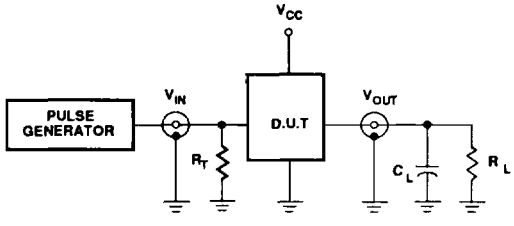
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



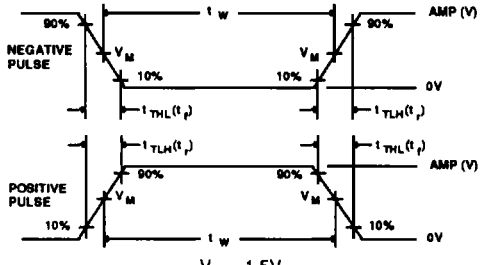
Waveform 3. Setup Time and Hold Time

NOTES: 1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.
3. $\overline{CE}$ may change only from High to Low while CP is Low

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns