

**PRIORITY**

**QRT™**

**WAC-487-A**

# ATM Quad Routing Table

\*\*\*U.S. Patents 5,557,607, 5,570,348, and 5,583,861\*\*\*

## DESCRIPTION

The WAC-487-A ATM Quad Routing Table (QRT™) is an advanced communications device capable of supporting very large, high-performance ATM switching systems. The rich feature set of the QRT enables systems to offer many sophisticated network services. The QRT provides 675 Mbps UTOPIA (Level 1 or Level 2) access to switch fabrics composed of either IgT WAC-188 ATM Switch Elements (SEs) or IgT WAC-488 ATM Quad Switch Elements (QSEs). Together, these devices can be used to build architectures with capacities from 675 Mbps to 10 Terabits per second (Tbps). The QRT can also act as a stand-alone 675 Mbps switch.

The QRT/QSE architecture virtually eliminates head-of-line blocking by means of the QRT's per-Virtual Channel (VC) receive queues and congestion feedback from the QSE™ switch fabric. The distributed architecture acts as an output-buffered switch by incorporating Evil Twin Switching™ (a congestion-reducing routing algorithm in the switch fabric) and a speed-up factor in the switch fabric (running the fabric faster than the line rate).

The QRT uses per-VC receive queues, 64 receive Service Classes (SCs), and 16 transmit SCs per each of the 31 Virtual Outputs (VOs) to enable flexible multi-priority scheduling algorithms. The scheduler can be used to ensure Quality-of-Service (QoS) guarantees for Constant Bit Rate (CBR), Variable Bit Rate (VBR), Available Bit Rate (ABR), and Unspecified Bit Rate (UBR) VCs. The QRT also provides five separate congestion thresholds, each with hysteresis, that selectively control AALS Early Packet Discard (EPD) and/or Cell Loss Priority (CLP)-based cell dropping for UBR support. Additional highlights of the QRT include full Virtual Path Indicator (VPI)/Virtual Channel Indicator (VCI) header translation, separate input and output cell buffers (up to 64K each), Virtual Path (VP)/VC switching, and support for up to 16K VCs on both the receive and transmit sides.

IgT also offers the QRT Device Control Package (WAC-487-DCP), which is a software package that harnesses the QRT's rich feature set and shortens system development times.

## FEATURES

### Queuing Algorithms

#### Receive

- Maintains 64 weighted, bandwidth-controlled SCs with per-VC queues.
- Provides round-robin servicing of queues within each SC.
- Provides per-channel (VP or VC), per-SC, and per-direction congested and maximum queue depth limits.
- Provides up to 64K cell buffers.

#### Transmit

- Provides 31 VOs.
- Maintains 16 SCs for each VO with per-VC accounting.
- Provides per-channel (VP or VC), per-SC Queue (SCQ), per-SC, per-VO, and per-direction congested and maximum queue depth limits.
- Provides up to 64K cell buffers.

### Congestion Management Algorithms

- Supports EPD and Partial Packet Discard (PPD) for UBR traffic, and as a backup for ABR traffic.
- Supports CLP-based cell discard and Explicit Forward Congestion Indicator (EFCI) cell marking.
- Supports three congestion limits (as well as EPD, CLP, and EFCI, and/or backpressure) for logical multicast on the transmit side.

### Switching

- Supports VC and VP switching.
- Supports up to 16K VCs.

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## Address Mapping

- Supports all 12 VP and 16 VC bits through use of a double, indirect lookup table.
- Performs header translation at both the input (receive) and output (transmit) directions. Input header translation is used to pass the output queue channel number through the switch.

## Multicast

- Supports logical multicast with a superior queue-clearing algorithm.

## Diagnostic/Robustness Features

- Checks the header parity.
- Counts tagged cells.
- Runs error checks continually on all fabric lines.
- Checks liveness of control signal lines at both switch fabric and UTOPIA interfaces, working around partial fabric failures.
- Checks Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) parity.

## Statistics Features

- In the receive direction, counts cells transmitted and dropped.
- In the transmit direction, counts cells transmitted and dropped on a per-VC basis.

## I/O Features

- Provides four switch element interfaces with phase aligners. The phase aligners allow for external serialization of the data stream enabling systems to be built that support device separation of up to 10 meters.
- Provides a UTOPIA Level 2 Multi-PHY (MPHY) 16-bit, 50 MHz interface.
- Provides a 2-level priority servicing algorithm for high and low bandwidth UTOPIA PHY layer devices.
- Provides a multiplexed address/data CPU interface.
- Provides two 100 MHz, 32-bit, synchronous DRAM cell buffer interfaces.
- Provides three 100 MHz, synchronous SRAM control interfaces.
- Provides a JTAG boundary scan interface.

## Compatibility Features

- Compatible with the ATM Forum 3.0, 3.1, and 4.0 specifications.
- Compatible with the ATM Forum UTOPIA Level 1 and Level 2 specifications.
- Compatible with the IgT WAC-188 ATM Switch Element.
- Compatible with the IgT WAC-187 ATM Routing Table.
- Compatible with the IgT WAC-488 ATM QSE.

## Physical Characteristics

- 3.3 V supply voltage.
- 5 V tolerant inputs on the microprocessor and UTOPIA interfaces.
- Available in a 503-pin Enhanced Plastic Ball Grid Array (EPBGA) package.

Figure 1 shows a QRT system block diagram.

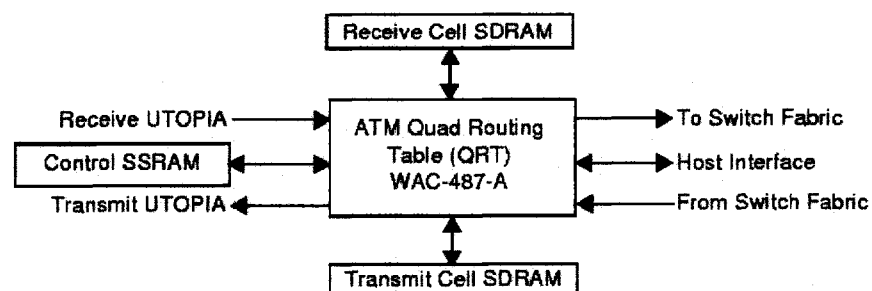


Figure 1. QRT System Block Diagram

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