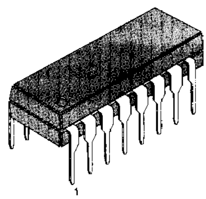
## 8-BIT D/A CONVERTERS

The KDA0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The KDA0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 $V_{p\text{-}p}$ with simple resistor loads. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications, while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the KDA0800 series will accept TTL levels with the logic threshold pin, $V_{LC}$, potentially allowing for direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33mW with ±5V supplies and is independent of the logic input states.

16 DIP



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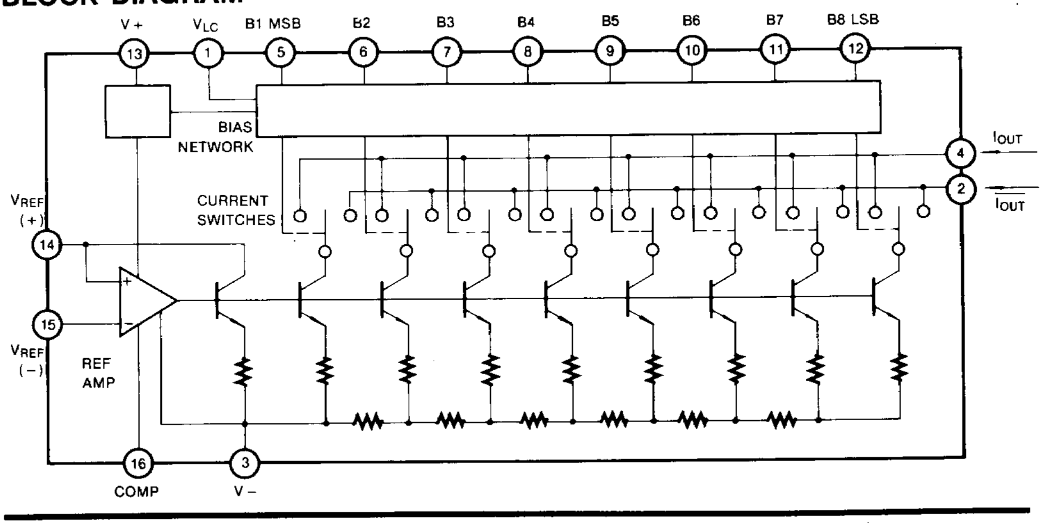
## FEATURES

- Fast settling output time: 100ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2-quadrant widerange multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33mW at ±5V
- Low cost
- Standard 16 DIP package

## ORDERING INFORMATION

| Device | Package | Temperature Range | Nonlinearity |
|---|---|---|---|
| KDA0800CN | 16 DIP | 0 ~ +70°C | ±0.19%FS |
| KDA0801CN | 16 DIP | 0 ~ +70°C | ±0.39%FS |
| KDA0802CN | 16 DIP | 0 ~ +70°C | ±0.1%FS |

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | ±18 or 36 | V |
| Power Dissipation | $P_D$ | 500 | mW |
| Reference Input Differential Voltage (V14 to V15) | $V_{IN}$ | $V^- \sim V^+$ | V |
| Reference Input Common Mode Range (V14, V15) | $V_{IN}$ | $V^- \sim V^+$ | V |
| Reference Input Current | $I_{ref}$ | 5 | mA |
| Logic Inputs | $V_{IN}$ | $V^- \sim V^- +36$ | V |
| Operating Temperature Range | $T_{opr}$ | $0 \sim +70$ | °C |
| Storage Temperature Range | $T_{stg}$ | $-65 \sim +150$ | °C |

## ELECTRICAL CHARACTERISTICS

($V_S = \pm 15V$, $I_{ref} = 2mA$, $T_{min} \leq Ta \leq T_{max}$ unless otherwise specified. Output characteristics refer to both $I_{OUT}$ and $\overline{I_{OUT}}$.)

| Characteristic | Symbol | Test Conditions | KDA0800 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Resolution | | | 8 | 8 | 8 | Bits |
| Monotonicity | | | 8 | 8 | 8 | Bits |
| Nonlinearity | | KDA0802<br>KDA0800<br>KDA0801 | | | ±0.1<br>±0.19<br>±0.39 | %FS |
| Settling Time | $t_S$ | To ±1/2 LSB, all bits switched "ON" or "OFF", Ta = 25°C | | 100 | 150 | ns |
| Propagation Delay<br>Each Bit<br>All Bits Switched | $t_{PLH}$, $t_{PHL}$ | Ta = 25°C | | 35<br>35 | 60<br>60 | ns<br>ns |
| Full-scale Tempco | $TCI_{FS}$ | | | ±10 | ±50 | ppm/°C |
| Output Voltage Compliance | $V_{OC}$ | Full scale current change < 1/2 LSB, $R_{OUT}$ > 20MΩ Typ | −10 | | 18 | V |
| Full-scale Current | $I_{FS4}$ | $V_{ref}$ = 10V, R14 = 5KΩ<br>R15 = 5KΩ, Ta = 25°C | 1.94 | 1.99 | 2.04 | mA |
| Full-scale Symmetry | $I_{FSS}$ | $I_{FS4} - I_{FS2}$ | | ±1 | ±8.0 | μA |
| Zero-scale Current | $I_{ZS}$ | | | 0.2 | 2.0 | μA |
| Output Current Range | $I_{FSR}$ | V− = −5V<br>V− = −8V to −18V | 0<br>0 | 2.0<br>2.0 | 2.1<br>4.2 | mA<br>mA |
| Logic Input Levels<br>Logic "0"<br>Logic "1" | <br>$V_{IL}$<br>$V_{IH}$ | $V_{LC}$ = 0V | 2.0 | | 0.8 | V<br>V |
| Logic Input Current<br>Logic "0"<br>Logic "1" | <br>$I_{IL}$<br>$I_{IH}$ | $V_{LC}$ = 0V<br>$-10V \leq V_{IN} \leq +0.8V$<br>$2V \leq V_{IN} \leq +18V$ | | <br>−2.0<br>0.002 | <br>−10<br>10 | <br>μA<br>μA |
| Logic Input Swing | $V_{IS}$ | V− = −15V | −10 | | 18 | V |
| Logic Threshold Range | $V_{THR}$ | $V_S$ = ±15V | −10 | | 13.5 | V |
| Reference Bias Current | $I_{15}$ | | | −1.0 | −3.0 | μA |
| Reference Input Slew Rate | dI/dt | | 4.0 | 8.0 | | mA/μs |
| Power Supply Sensitivity | $PSSI_{FS+}$ | $4.5V \leq V+ \leq 18V$ | | 0.0001 | 0.01 | %/% |

## ELECTRICAL CHARACTERISTICS (Continued)

| Characteristic | Symbol | Test Conditions | KDA0800 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | $PSSI_{FS-}$ | $-4.5V \leq V- \leq 18V$<br>$I_{ref} = 1mA$ | — | 0.0001 | 0.01 | %/% |
| Power Supply Current | I+<br>I− | $V_S = \pm 5V$, $I_{ref} = 1mA$ | —<br>— | 2.3<br>−4.3 | 3.8<br>−5.8 | mA<br>mA |
| | I+<br>I− | $V_S = 5V, -15V$, $I_{ref} = 2mA$ | —<br>— | 2.4<br>−6.4 | 3.8<br>−7.8 | mA<br>mA |
| | I+<br>I− | $V_S = \pm 15V$, $I_{ref} = 2mA$ | —<br>— | 2.5<br>−6.5 | 3.8<br>−7.8 | mA<br>mA |
| Power Dissipation | $P_D$ | $\pm 5V$, $I_{ref} = 1mA$<br>$5V, -15V$, $I_{ref} = 2mA$<br>$\pm 15V$, $I_{ref} = 2mA$ | —<br>—<br>— | 33<br>108<br>135 | 48<br>136<br>174 | mW<br>mW<br>mW |

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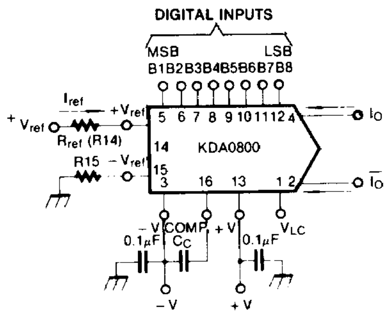
## TYPICAL APPLICATIONS




$$I_{FS} \cong \frac{+V_{ref}}{R_{ref}} \times \frac{255}{256}$$

$I_O + \bar{I}_O = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{ref} = 10V$

$R_{ref} = 5K\Omega$

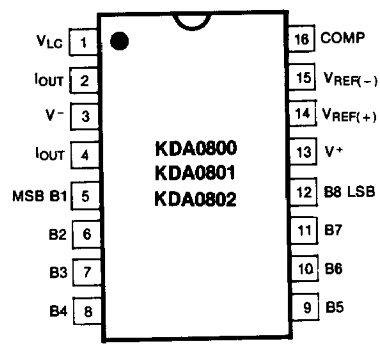
$R15 \cong R_{ref}$

$C_C = 0.01\mu F$

$V_{LC} = 0V$ (Ground)

**Fig. 1 Basic Positive Reference Operation**

## PIN CONFIGURATION




Top View

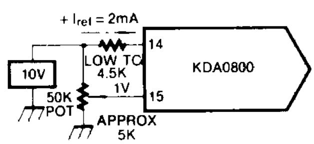
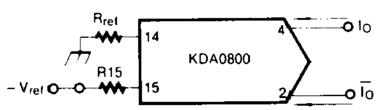



**Fig. 2 Recommended Full Scale Adjustment Circuit**

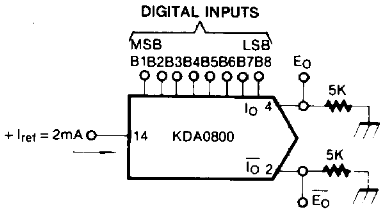



$$I_{FS} \cong \frac{-V_{ref}}{R_{ref}} \times \frac{255}{256}$$

Note: $R_{ref}$ sets $I_{FS}$; R15 is for bias current cancellation

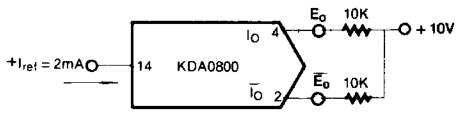
**Fig. 3 Basic Negative Reference Operation**

## TYPICAL APPLICATIONS (Continued)



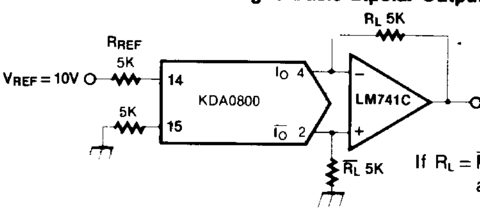

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $I_o$ mA | $\overline{I_o}$ mA | $E_o$ | $\overline{E_o}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Full-scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1.992 | 0.000 | −9.960 | 0.000 |
| Full-scale − LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1.984 | 0.008 | −9.920 | −0.040 |
| Half-scale + LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1.008 | 0.984 | −5.040 | −4.920 |
| Half-scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.000 | 0.992 | −5.000 | −4.960 |
| Half-scale − LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.992 | 1.000 | −4.960 | −5.000 |
| Zero-scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.008 | 1.984 | −0.040 | −9.920 |
| Zero-scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | 1.992 | 0.000 | −9.960 |

**Fig. 4 Basic Unipolar Negative Operation**




| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $E_o$ | $\overline{E_o}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Pos. Full-scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −9.920 | +10.000 |
| Pos. Full-scale − LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | −9.840 | +9.920 |
| Zero-scale + LSB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −0.080 | +0.160 |
| Zero-scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0.000 | +0.080 |
| Zero-scale − LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +0.080 | 0.000 |
| Neg. Full-scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +9.920 | −9.840 |
| Neg. Full-scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +10.000 | −9.920 |

**Fig. 5 Basic Bipolar Output Operation**




$E_O = V_{REF}\left(\frac{-255}{256} + \frac{2X}{256}\right)$

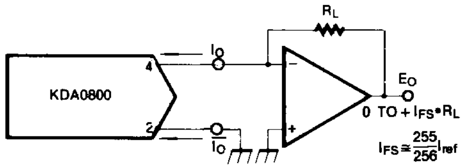
where X is the input code and
$R_L = \overline{R_L} = R_{REF}$

If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

| | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | $E_o$ |
|---|---|---|---|---|---|---|---|---|---|
| Pos. Full-scale | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +9.920 |
| Pos. Full-scale − LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | +9.840 |
| (+) Zero-scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +0.040 |
| (−) Zero-scale | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | −0.040 |
| Neg. Full-scale + LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | −9.840 |
| Neg. Full-scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | −9.920 |

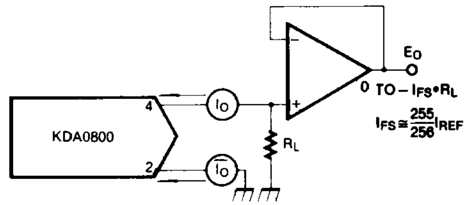
**Fig. 6 Symmetrical Offset Binary Operation**

## TYPICAL APPLICATIONS (Continued)




For complementary output
(operation as negative logic DAC), connect
inverting input of op amp to $I_O$ (Pin 2),
connect $I_O$ (Pin 4) to the ground.

**Fig. 7 Positive Low Impedance Output Operation**




For complementary output
(operation as a negative logic DAC) connect
non-inverting input of op amp to $I_O$ (Pin 2);
connect $I_O$ (Pin 4) to the ground.

**Fig. 8 Negative Low Impedance Output Operation**

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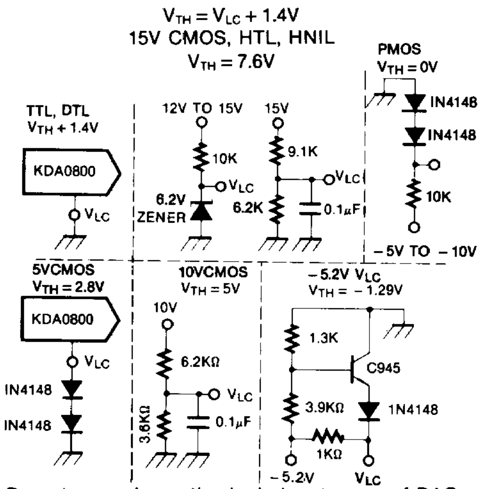
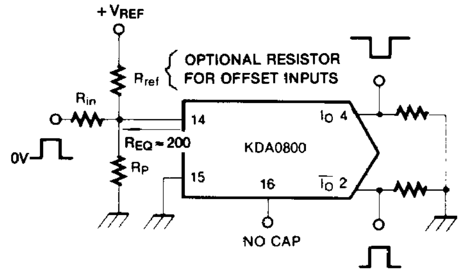



Do not exceed negative logic input range of DAC.

**Fig. 9 Interfacing with Various Logic Families**




Typical values: $R_{IN} = 5K$, $+V_{IN} = 10V$

**Fig. 10 Pulsed Reference Operation**

**(a) $I_{ref} \geq$ peak negative swing of $I_{IN}$**

**(b) $+V_{ref}$ must be above the peak positive swing of $V_{IN}$**

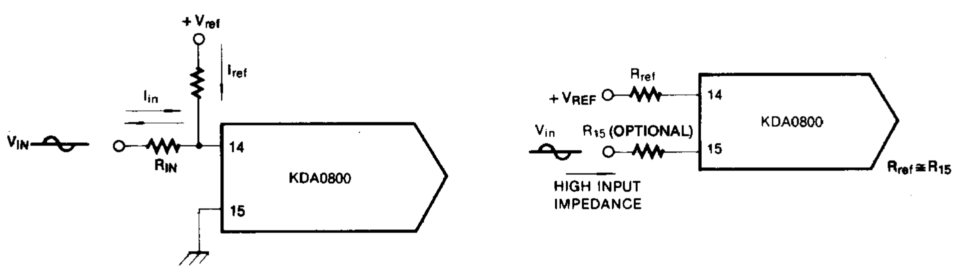



**Fig. 11. Accommodating Bipolar References**

## TYPICAL APPLICATIONS (Continued)

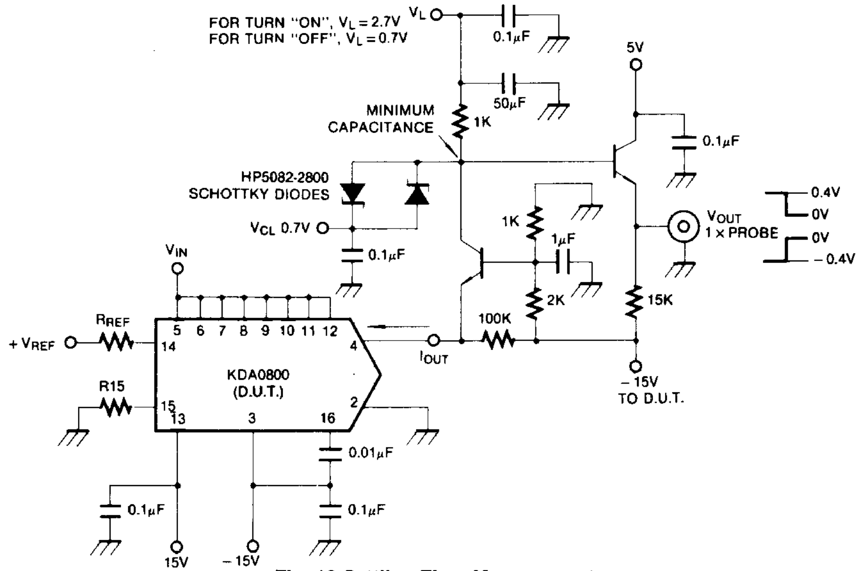
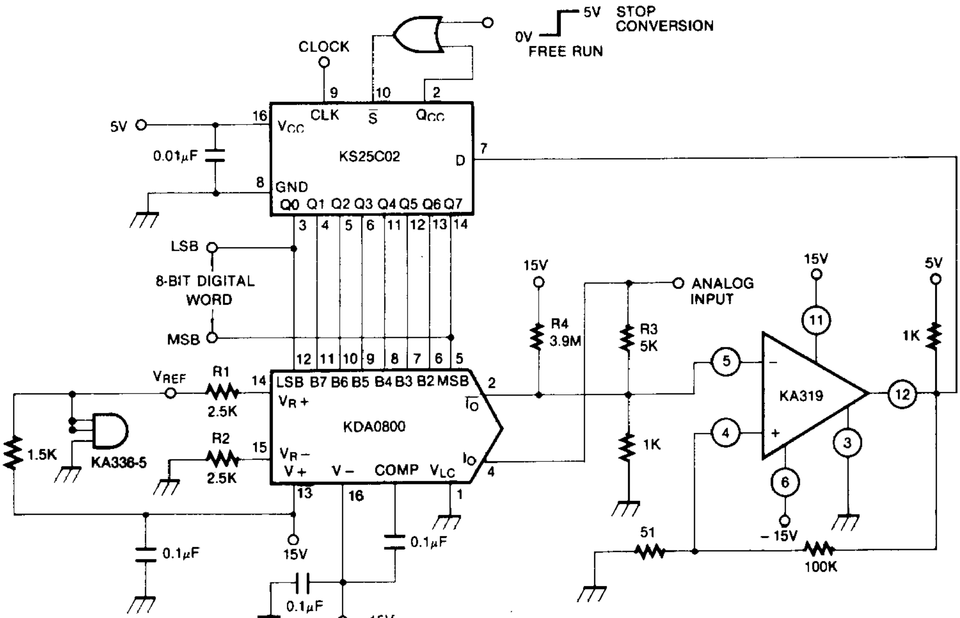



**Fig. 12 Settling Time Measurement**




Note. For a 1μs conversion time with an 8-bit resolution and a 7-bit accuracy, a KA361 comparator replaces the KA319 and the reference current is doubled by reducing R1, R2 and R3 to 1.25KΩ and R4 to 2MΩ.

**Fig. 13 A Complete 2 μs Conversion Time, 8-Bit A/D Converter**