NOT FOR NEW DESIGN
USE TS 83510

TS 83010

CMOS 10-BIT, 20 MHz FLASH A/D CONVERTER

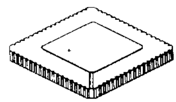
DESCRIPTION

The TS 83010 is a monolithic CMOS 10 bit parallel flash Analog-to-Digital converter designed for applications requiring high speed conversion.

The TS 83010 uses 1024 parallel comparators to digitize fast moving analog input signals. An overflow bit is incorporated.

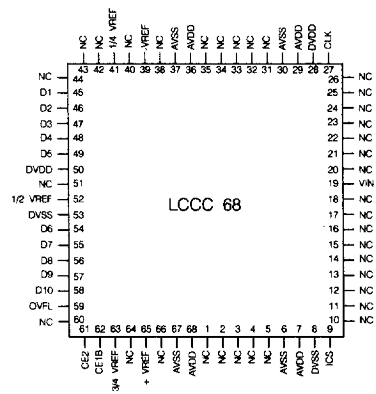
With an encode rate of 20 MHz, the TS 83010 is specified to operate from commercial to military temperature range with analog input frequency of 1 MHz, making it ideal for a variety of applications and environments. The cycling auto-zero feature which is implemented in its flash architecture allows the TS 83010 to require 0.7 W of power only.

This product is packaged in hermetic ceramic 68-pin LCCC and is available also in die form. On the latter, the coding bits are on the same side, and voltage inputs are symmetrical, facilitating the implementation.



E
LCCC 68
(Leadless ceramic chip carrier)

PIN CONNECTIONS
(Top view)



MAIN FEATURES

- 10-bit resolution.
- 20 MHz sampling rate.
- Single power supply.
- −55°C / +125°C specified.
- Guaranteed monotonicity.
- Overflow bit.
- 0.7 W power consumption.

APPLICATIONS

- Military systems.
- Radar pulse analysis.
- Video digitizing.
- Image processing.
- Medical imaging.
- High energy physics.
- X-Ray and ultrasound imaging.

ABSOLUTE MAXIMUM RATINGS (see Note 1)

Symbol	Parameter	Value	Unit
AV_{DD}, DV_{DD}	Supply voltages (see Note 2)	− 0.3 to + 7	V
$+V_{REF}$	Upper reference voltage	− 0.3 to AV_{DD}	V
$-V_{REF}$	Lower reference voltage	− 0.3 to AV_{DD}	V
1/2 I_{VREF}	Mid-point reference current	3	mA
1/4 I_{VREF}	First quarter reference current	3	mA
3/4 I_{VREF}	Third quarter reference current	3	mA
V_{IN}	Analog input voltage (see Note 2)	− 0.3 to AV_{DD}	V
CLK / ICS	Digital input voltage (see Note 2)	− 0.3 to DV_{DD}	V
CE1, CE2	Tristate command	− 0.3 to DV_{DD}	V
I_D	Digital output currents	40	mA
T_j	Junction temperature	+ 150	°C
T_{stg}	Storage temperature	− 65 to + 150	°C
T_{oper}	Operating temperature	− 55 to + 125	°C
T_{leads}	Lead temperature (soldering 10 S)	+ 260	°C

Note 1 : Absolute maximum ratings are admissible limits for each parameter while all other parameters are within the specified operating conditions. Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to $AV_{SS} = DV_{SS}$.

SET UP TIME

Due to cyclic auto-zero, it is necessary to wait for a given time, before getting valid data : $T_{set\ up} = 4 \times 1024 \times T_{CLK}$ after setting up the device (V_{DD} + CLK).

USER WARNING

The power supplies must the applied before all the other signals to prevent damage from occuring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$AV_{DD} = DV_{DD} = +5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	Tcase	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				10		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility (see Note 1)				TTL		
Clock input		IV				
• Logic «0» voltage	full		0		0.8	V
• Logic «1» voltage	full		2		5	V
Tristate command		III				
• Logic «0» voltage			0		0.8	V
• Logic «1» voltage			2		5	V
Output data		II, D				
• Logic «0» voltage (see Note 2)	full				0.5	V
• Logic «1» voltage (see Note 3)	full		2.4			V
• Tristate		III		0.1	10	μA
• Output delay (see Note 4)		IV		25	40	ns
MAX SAMPLING FREQUENCY	full	II	20			MHz
MIN SAMPLING FREQUENCY	full	I			1	MHz
	full	III			3	MHz
ANALOG INPUT						
Voltage range		V		V_{REF}		V
Input capacitance		V		100		pF
Input resistance		I, D	10			MΩ
Analog bandwidth (see Note 5)		I			1	MHz
REFERENCE INPUT						
Lower reference voltage		V		0		V
Upper reference voltage		I, D	1	2.5	$AV_{DD} - 2.5$	V
Differential reference voltage		I, D	1	2.5	$AV_{DD} - 2.5$	V
Reference ladder resistance		I, D	1.8	3	3.7	kΩ
	full	II	1	3	5	kΩ
POWER REQUIREMENTS						
Power supply		I, D	4.5	5	5.5	V
Power dissipation (see Note 6)						
• Analog supply		I, D		550	650	mW
• Digital supply		I, D		150	250	mW
THERMAL RESISTANCE (see Note 7)						
Junction-to-ambient (still air) θ_{JA}		V		45		°C/W
Junction-to-case θ_{JC}		V		5		°C/W

Note 1 : TTL : DATA OUTPUT, clock input, $\overline{CE1}$, CE2.
Note 2 : With $I_{out} = -4$ mA.
Note 3 : With $I_{out} = +0.4$ mA.
Note 4 : See timing diagram.
Note 5 : Specified frequencies are maximum with no missing codes.
Note 6 : Clock frequency : 20 MHz.
Note 7 : For leadless ceramic chip carrier package.

System performance characteristics

$AV_{DD} = DV_{DD} = +5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
ACCURACY (see Notes 1 and 2)						
Offset error	full	V		± 10		LSB
Gain error	full	V		± 10		LSB
Integral nonlinearity		I, D		± 1.5	± 2.5	LSB
	full	II		± 2		LSB
Differential nonlinearity		I, D		± 0.6	± 1	LSB
	full	II		± 0.8	± 1	LSB
Monotonicity and no missing codes	full	IV	Guaranteed in specified temperature range			
DYNAMIC CHARACTERISTICS (see Notes 2 and 3)						
Signal-to-noise ratio						
$F_S = 10\ MHz$ $F_{in} = 0.1\ MHz$ (ICS = «1»)		I, D	50	51		dB
$F_S = 20\ MHz$ $F_{in} = 1\ MHz$ (ICS = «0»)		I		45.5		dB
Total harmonic distorsion						
$F_S = 10\ MHz$ $F_{in} = 0.1\ MHz$ (ICS = «1»)		I, D	50	55		dB
$F_S = 20\ MHz$ $F_{in} = 1\ MHz$ (ICS = «0»)		I		46		dB
Number of effective bits						
$F_S = 10\ MHz$ $F_{in} = 0.1\ MHz$ (ICS = «1»)		I, D	8	8.2		Bits
$F_S = 20\ MHz$ $F_{in} = 1\ MHz$ (ICS = «0»)		I		7.3		Bits
Aperture uncertainty		V		30		pS

Note 1 : Histogram based on sampling of 100 kHz sinusoïdal analog signal with an encode rate of 10 MHz.

Note 2 : For sampling frequency below 11 MHz ICS should be set to DV_{DD}.
For sampling frequency up to 11 MHz ICS should be set to DV_{SS} or be left unconnected.

Note 3 : Dynamic measurements are performed with a $V_{p\text{-}p}$ sine wave input equal to 90 % of V_{REF}.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sampling test at specified temperature.
III	Sampling test only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at $T_{amb} = +25°C$.

SWITCHING PERFORMANCES

Symbol	Definition of terms	Min.	Typ.	Max.	Unit
$1/F_S$	Period of clock signal	50 ns			ns
TC1	High level clock pulse width	$0.4 / F_S$		$0.6 / F_S$	ns
T_D	Delay time between input and output		27		ns
t_r / t_f	Clock rise and fall time		5		ns

TIMING DIAGRAM

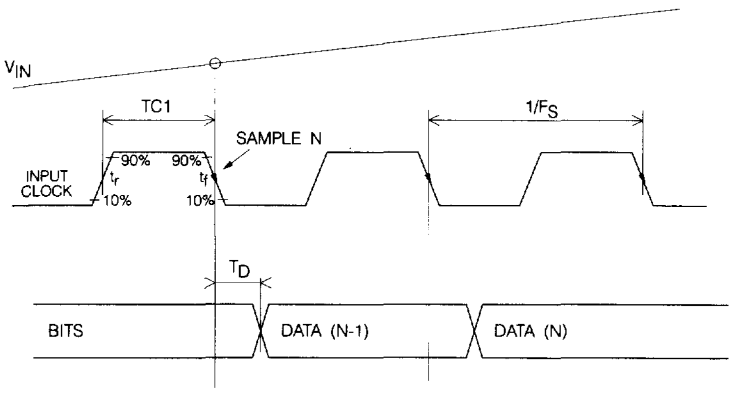


Figure 1 : Time t_r is design dependent.

PIN DESCRIPTION

Pin	Symbol	Function	Description
1, 2	NC	Not connected	
3, 4	NC	Not connected	
5	NC	Not connected	
6	AV_{SS}	Analog ground	
7	AV_{DD}	Analog supply	
8	DV_{SS}	Digital ground	
9	ICS	Digital input	Internal clock select
10	NC	Not connected	
11	NC	Not connected	
12	NC	Not connected	
13	NC	Not connected	
14	NC	Not connected	
15	NC	Not connected	
16	NC	Not connected	
17	NC	Not connected	
18	NC	Not connected	
	NC	Not connected	
19	V_{IN}	Analog input	
20	NC	Not connected	
21	NC	Not connected	
22	NC	Not connected	
23	NC	Not connected	
24	NC	Not connected	
25	NC	Not connected	
26	NC	Not connected	
27	CLK	Clock input	
28	DV_{DD}	Digital supply	
29	AV_{DD}	Analog supply	
30	AV_{SS}	Analog ground	
31	NC	Not connected	
32	NC	Not connected	
33, 34, 35	NC	Not connected	
36	AV_{DD}	Analog supply	
37	AV_{SS}	Analog ground	
38	NC	Not connected	
39	$-V_{REF}$	Lower reference	Access to the lower reference voltage. A voltage source must be applied (or ground).
40	NC	Not connected	
41	1/4 V_{REF}	1st quarter ref.	Access to the first quarter reference voltage
42	NC	Not connected	
43	NC	Not connected	
44	NC	Not connected	
45	D1	D1 output	TTL level
46	D2	D2 output	TTL level
47	D3	D3 output	TTL level
48	D4	D4 output	TTL level
49	D5	D5 output	TTL level
50	DV_{DD}	Digital supply	
51	NC	Not connected	
52	1/2 V_{REF}	Half ref.	Access to the half ref. volt.
53	DV_{SS}	Digital ground	

PIN DESCRIPTION (Continued)

Pin	Symbol	Function	Description
54	D6	D6 output	TTL level
55	D7	D7 output	
56	D8	D8 output	
57	D9	D9 output	
58	D10	D10 output	
59	OVFL	Overflow status line	This line is set to logical «1» when the input signal is higher than $+V_{REF}$ voltage. All data (D1 to D10) are set to logical «1».
60	NC	Not connected	
61	CE2	Tristate command	CE2 = «1» : overflow valid out data lines valid only if $\overline{CE1}$ = 0
62	CE1	Tristate command	CE2 = 0 : Tristate for both overflow status and data lines
63	3/4 V_{REF}	3rd quarter ref.	Access to 3 rd quarter ref.
64	NC	Not connected	
65	$+V_{REF}$	Upper reference	Access to the upper reference voltage. A voltage source must be applied.
66	NC	Not connected	
67	AV_{SS}	Analog ground	
68	AV_{DD}	Analog supply	

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FUNCTIONAL BLOCK DIAGRAM

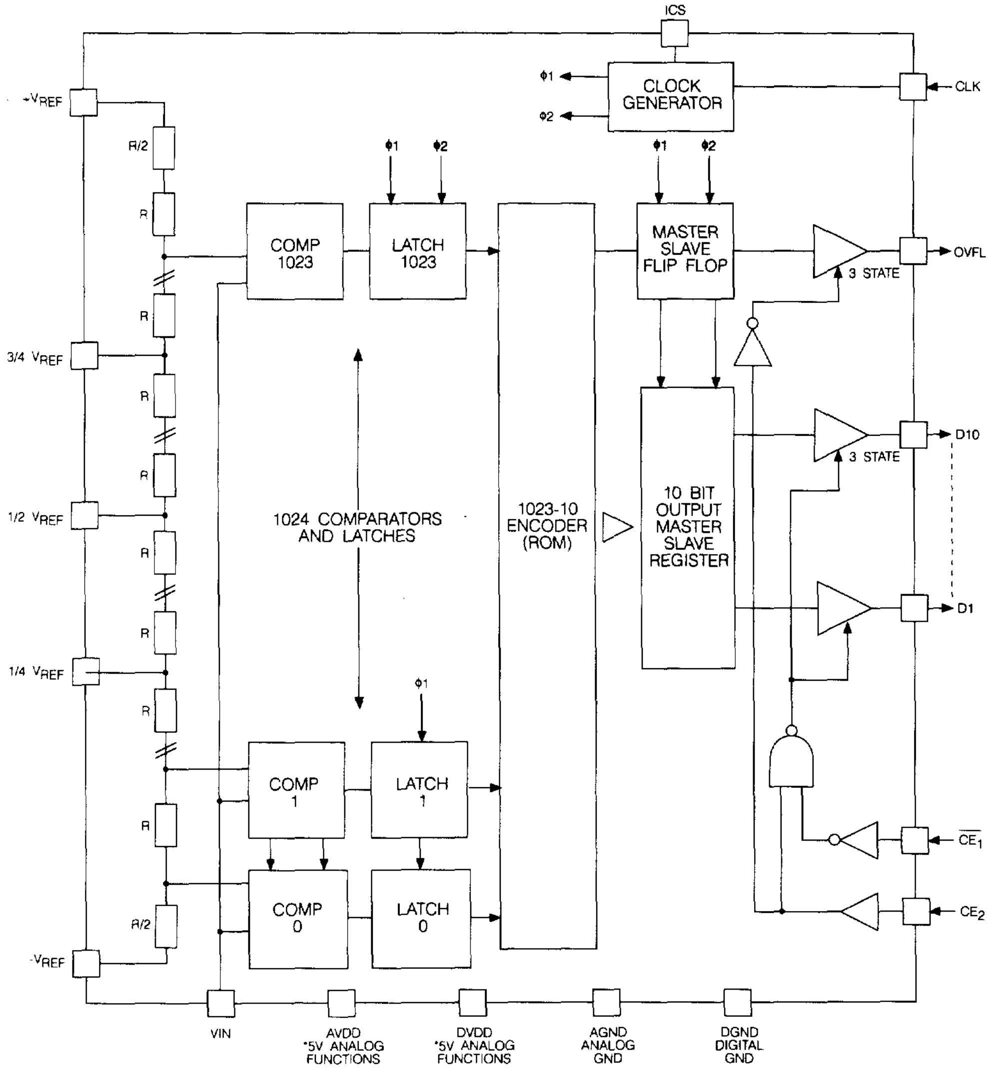

Figure 2

FUNCTIONAL DESCRIPTION

TS 83010 is based on a new architecture (cyclic auto-zero) patented by TCS, which avoids the drawbacks of conventional MOS converters (8-bit resolution).

Instead of putting all comparators in auto-zero mode at each clock cycle, only one is put in this mode, the others remain in the comparison mode. Auto-zero of the comparators is then implemented successively.

Thanks to this feature, charge pumping on reference ladder and on signal input is eliminated out, and low power and high-sampling frequency are achieved.

The TS 83010 includes :

- a sequencer generating internal clocks,
- the core ensuring conversion,
- an output circuit delivering digital data,
- the means to implement cyclic auto-zero.

The core includes :

- A linear resistor ladder delivering 1024 reference voltages distributed linearly between external reference voltages ($+V_{REF}$ and $-V_{REF}$). Access to quarter (1/4 V_{REF}), half (1/2 V_{REF}), and three quarter (3/4 V_{REF}) ladder make it possible to :
  - improve linearity by external reference voltage forcing,
  - filter disturbances going through the ladder by means of external capacitors,
  - the delinearize the bridge by means of external resistors.
- 1024 comparators and latches,
- A 1024 to 10 bits decoder.

The output stage consists of 11 identical parts (10 bits and overflow), each formed of a master-slave flip-flop and a tristate output buffer.

If the input signal is higher than the upper most reference voltage, code 1023 is written to the output and overflow bit is set to logic «1». Inputs $\overline{CE1}$ and CE2 switch the output bits to high impedance according to the following table.

$\overline{CE1}$	CE2	D1 ... D10 in high Z	OVFL in high Z
0	0	Yes	Yes
0	1	No	No
1	0	Yes	Yes
1	1	Yes	No

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

APPLICATION CONSIDERATIONS

In order to optimize dynamic performances of TS 83010, the ICS pin state (Internal Clock Select) should be chosen according to the sampling frequency :

- below 11 MHz ICS state should be set to V_{DD},
- above 11 MHz, ICS state should be set to GND or left unconnected. In that case, at 20 MHz sampling frequency, the optimal high state duration of the clock is 20 ns.

The operating conditions of TS 83010 can still be improved under a specific condition.

By setting the ICS pin to V_{DD} and the duration of the high state of the clock between 8 ns and 13 ns, an increase of 0.1 to 0.2 effective number of bits will be seen for clock frequency from 1 to 20 MHz.

One should notice that, in that case, the clock duty cycle will be less than 20 % even at 20 MHz clock input.

This condition is not given in the «timing diagram» sheet number 5.

In all cases, in order to prevent clock disturbance on the analog input it is necessary to drive this input with a low impedance generator.

TYPICAL EVALUATION CIRCUIT

The general circuit used for the flash converter in typical conditions is represented on Figure 3.

- **Voltage reference**

Flash converter requiring a positive reference voltage ($+V_{REF}$) ranging from 2 V to 2.5 V, a voltage regulator generates a reference voltage of 2.5 V from the power supply voltage (+5 V).

- V_{REF} has to be set to analog ground.

- **Resistor ladder reference voltages**

The circuit allows to access some particular points on the resistor bridge. These points correspond to 3/4, 1/2 and 1/4 of the bridge total resistance. This feature enables use of the flash converter in two ways :

- In linear operation with these 3 points grounded by decoupling capacitors in order to filter disturbances along the bridge.
- In non-linear operation with the following 2 functions.

  Improvement in flash converter integral linearity by forcing the 3 points to their corresponding voltages.
  Implementation of a non-linear conversion law (compression law for instance) in order to better observe the results of the conversion on one part only of the transfer curve.

- **Analog signal**

For better dynamic performance, the analog input signal must be driven by a wideband buffer amplifier (CLC 110) with a low output impedance.

The input signal should have an offset voltage equal to half the reference voltage ($\pm V_{REF}$) in order to be comprised between $+V_{REF}$ and $-V_{REF}$.

- **Clock signal**

Clock signals are CMOS compatible.

- **Considerations on electrical layout**

A certain number of elementary precautions should be taken in the electrical layout when using high frequencies.

The main ones are as follows :

- a ground plane for the components,
- the ground tracks corresponding to the various signals (clock, input signal, references) are separated and connected together to a single point,
- star distributed power supply (idem for ground) to avoid any possible loop,
- a maximum capacitive uncoupling as close as possible to each circuit.

- **High input frequency signal**

In order to obtain good performance for high input frequency signal (> 1 MHz) the use of a sample and hold is recommended.

Input signal must be held during the high state of CK1 internal clock corresponding to (input clock delayed by 5 to 8 ns). An example of a typical circuit is given in Figure 4a.

- **Set up time**

Due to cyclic auto zero, it is necessary to wait for a given time, before getting valid data : $T_{set\ up} = 4 \times 1024 \times T_{CLK}$ after setting up the device (V_{DD} + CLK).

TYPICAL EVALUATION CIRCUIT (SCHEMATIC)

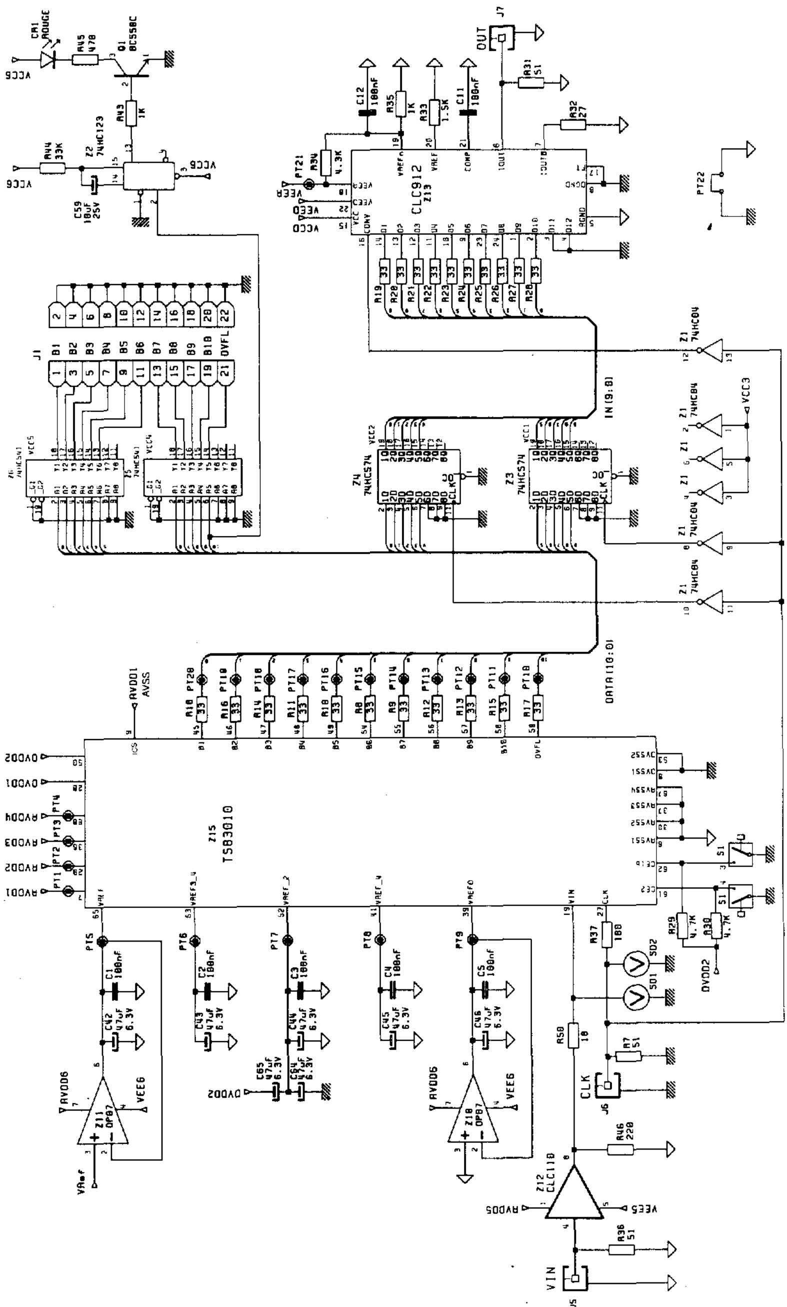

Figure 3

TYPICAL EVALUATION CIRCUIT WITH A SAMPLE AND HOLD

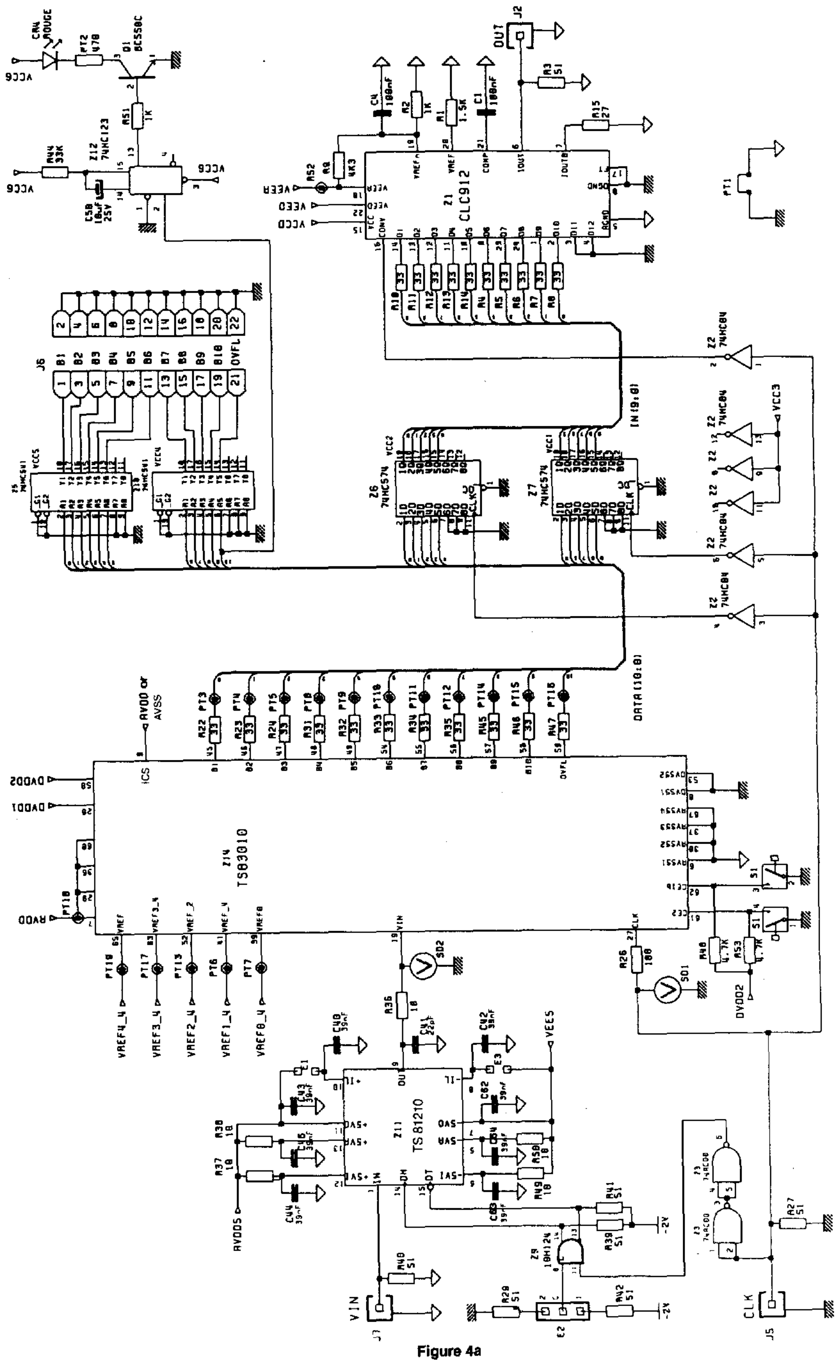

Figure 4a

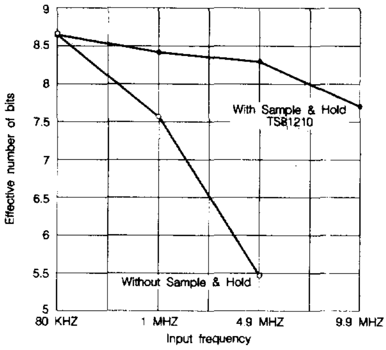

Figure 4b : Effective number of bits versus input frequency, F_S = 20 MHz.

TYPICAL PERFORMANCE CURVES

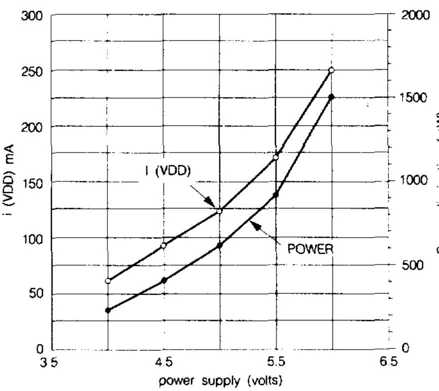

Figure 5 : Current and power supply dissipation.

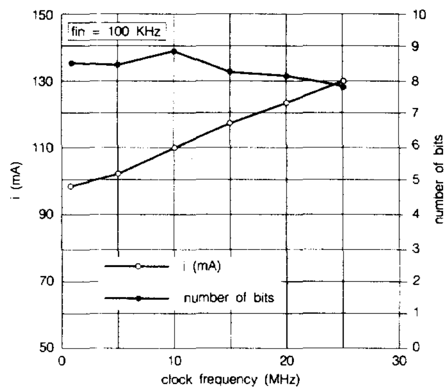

Figure 6 : Current consumption and effective number of bits vs sampling frequency.

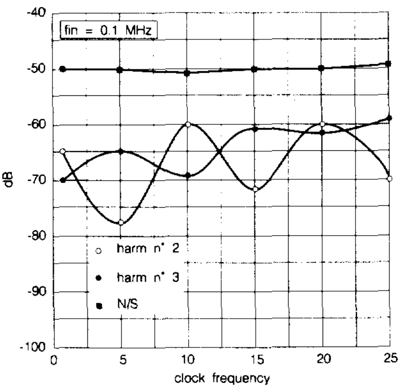

Figure 7 : Total noise to signal ratio and level of the two-first harmonics vs sampling frequency.

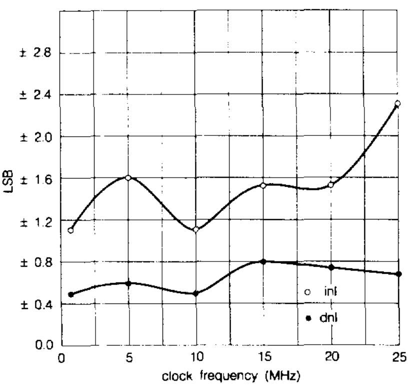

Figure 8 : Peak to peak Integral and differential non linearity vs sampling frequency.

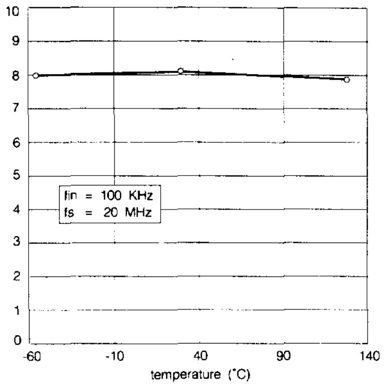

Figure 9 : Effective number of bits vs temperature.

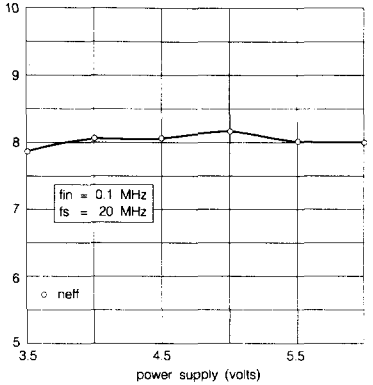

Figure 10 : Effective number of bits vs power supply.

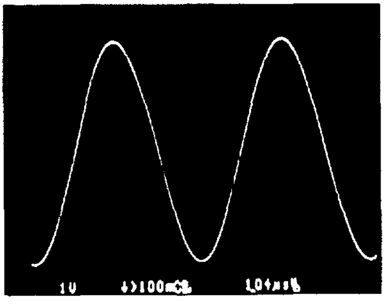

Figure 11 :200 kHz reconstructed waveform at F_S = 20 MHz.

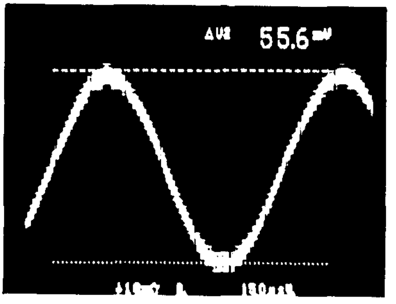

Figure 12 : Very small amplitude reconstructed waveform at 20 MHz sampling (20 LSB = 50 mV).

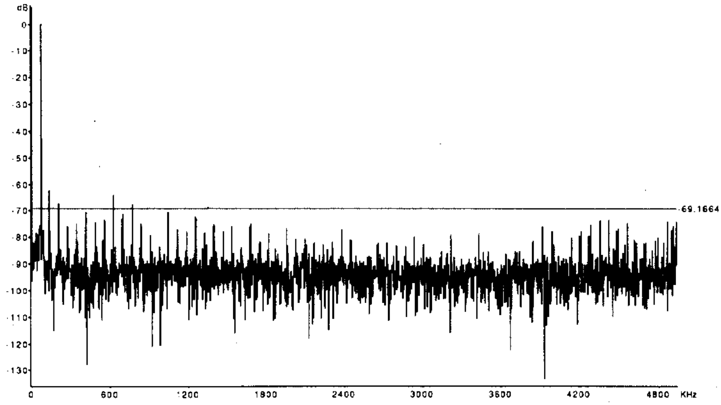

Figure 13 : 4096 pts FFT ; F_{in} = 100 kHz, F_S = 20 MHz.

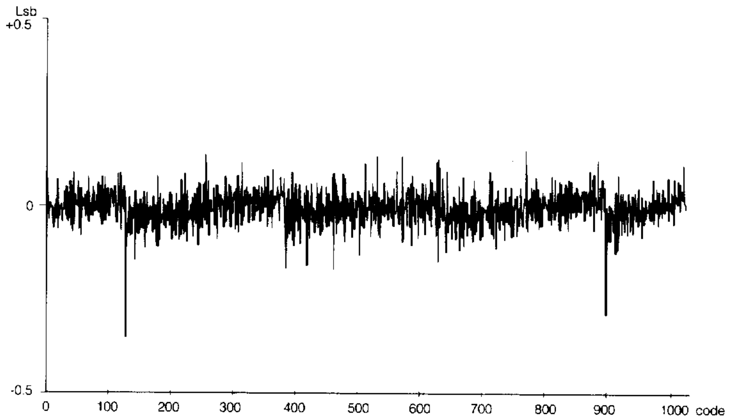

Figure 14 : Differential non linearity : F_{in} = 100 kHz, F_S = 20 MHz.

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DEFINITION OF TERMS

Signal-to-noise ratio (SNR) :
Determined by FFT analysis,

$$SNR = 10 . \log \left[\frac{P(F_{IN})}{P_n}\right] = 10 . \log \left[\frac{A^2(F_{IN})}{\Sigma A^2(j)}\right]_{j = F_{in}}$$

With :
- P (FIN) spectral power of the input frequency F_{IN}.
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN}.
- A (j) amplitude of the spectral component of frequency j.

Total harmonic distorsion (THD) :
Determined by FFT analysis,

$$THD = 10 . \log \left[\frac{P(F_{IN})}{P_{hm}}\right] = 10 . \log \left[\frac{A^2(F_{IN})}{\Sigma A^2(k.F_{IN})}\right] \text{ with } k \geqslant 2$$

With : P_{hm} harmonic noise power, which is defined as the sum of the powers of all harmonics of F_{IN}.

Number of effective bits (N_{eff}) :
Determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e) :

$$G_e = \frac{G - G_e}{G_o}$$

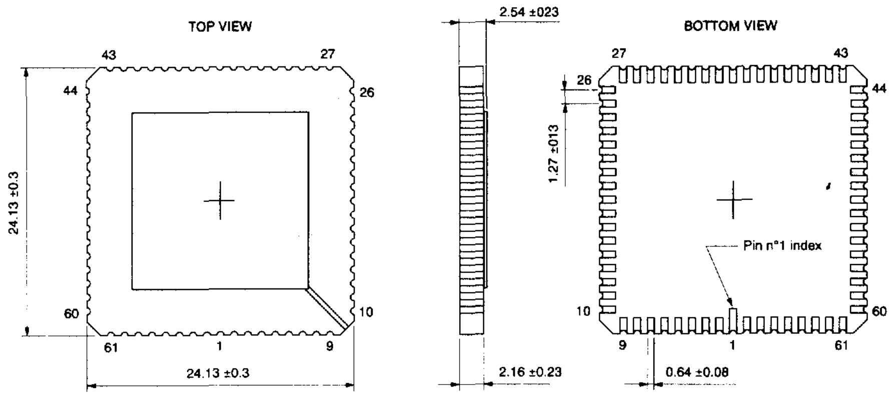
With :
- G_o slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL) :
Measured after trimming the offset and gain errors to zero.
The integral nonlinearity for an output code i, INL(i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.
The ADC integral nonlinearity INL is the maximum value of all | INL(i) |.

Differential nonlinearity (DNL) :
Measured after trimming the offset and gain errors to zero.
The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal ISB step size.
The ADC differential nonlinearity DNL is the maximum value of all | DNL(i) |.

MECHANICAL PACKAGE DATA

LCCC 68 - LEADLESS CERAMIC CHIP CARRIER PACKAGE (Dimensions in mm)



DIE MECHANICAL INFORMATION : JTS 83010

Pad layout : V634

Pad size : 0.100 x 0.120 mm

Die size : 8.700 x 7.500 mm

Die thickness : 380 μm

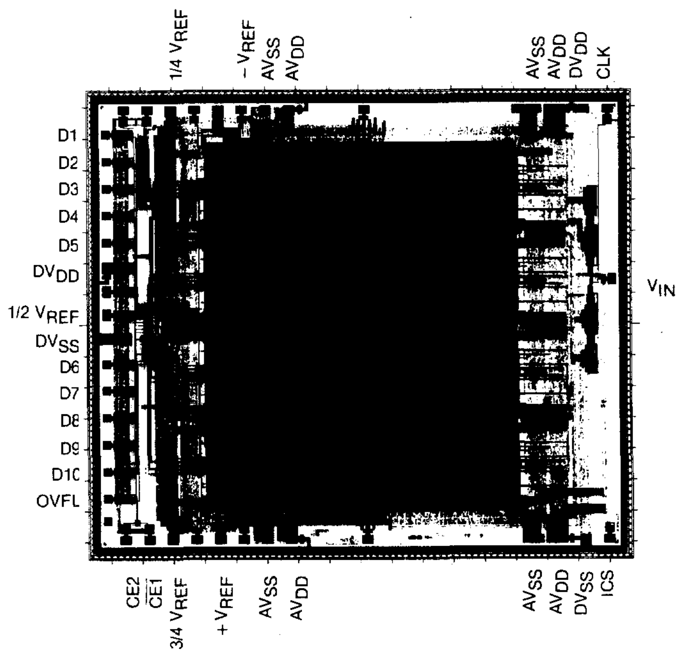
Metallization : Si (Back side)
Al (Front side)

Passivation : Nitride

Revision : A

Qualification lot package : LCCC 68

Back side bias : AV_{SS}



ORDERING INFORMATION

Package device

TS 83010 M E 1 B / T

- TS: TCS (1) prefix
- 83010: Device or family
- M: Temperature range :
  - M : –55, +125°C
  - V : –40, +85°C
  - C : 0, +70°C
- E: Package
  - E : LCCC 68 pins
- 1: Lead finish
  - 1 : Tin plated
  - 8 : Gold plated
  - ....not available
  - ....in B/T
- B/T: Quality level
  - -- : Standard
  - B/T : According to
  - . MIL-STD 883

Die form

J TS 83010 – 1 V A

- J: Die prefix
- TS: TCS prefix (1)
- 83010: Generic part number
- 1: Back side metallization
  - 1 = Nacked Si
- V: Screening levels (2)
  - V : Visual inspection
- A: Revision of the mask set

Temperature range
– : Tamb = 25°C

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sale office.