Signetics

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FAST Products	

FAST 74F786
Asynchronous Bus Arbiter

4-Bit Asynchronous Bus Arbiter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F786	6.6ns	55mA

FEATURES

- **Arbitrates between 4 asynchronous inputs**
- **Separate grant output for each input**
- **Common output enable**
- **On-board 4 input AND gate**
- **Metastable-free outputs**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F786N
16-Pin Plastic SO	N74F786D

DESCRIPTION

The 74F786 is an asynchronous 4-bit arbiter designed for high speed real-time applications. The priority of arbitration is determined on a first-come first-served basis. Separate Bus Grant ($\overline{BG}_n$) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}$ outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal a separate 4 input AND gate is provided which may also be used as an independent AND gate. Unused Bus Request ($\overline{BR}_n$) inputs may be disabled by tying them High.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR}_0$ - $\overline{BR}_3$	Bus Request inputs (active Low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common Bus Grant output enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_{OUT}	AND gate output	150/40	3.0mA/24mA
$\overline{BG}_0$ - $\overline{BG}_3$	Bus Grant outputs (active Low)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

The 'F786 is designed so that contention between two or more request signals will not glitch or display a metastable condition. In this situation an increase in the $\overline{BR}_n$ to $\overline{BG}_n$ t_{PHL} may be observed. A typical 'F786 has an h = 6.6ns, τ = .41ns and and T_0 = 5µsec.

Where:

h= Typical propagation delay through the device and τ and T_0 are device parameters derived from test results and can most nearly be defined as:

τ= A function of the rate at which a latch in a metastable state resolves that condition.

T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device.

For further information, please refer to the 'F786 application notes.

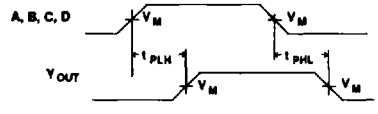
The $\overline{BR}_n$ inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is Low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. Removing a request while a previous request is being serviced can cause a grant to be changed when arbitrating between three or four requests. For that reason, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}_n$ inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}_n$ outputs will be held in the High state until the selection is made. This guarantees that an erroneous $\overline{BG}_n$ will not be generated even though a metastable condition may occur internal to the device.
When the $\overline{EN}$ is in the High state the $\overline{BG}_n$ outputs are forced High.

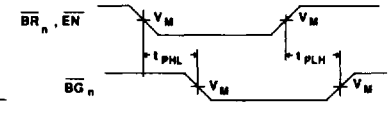
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A, B, C, D to Y_{OUT}	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{BR}_n$ to $\overline{BG}_n$	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{EN}$ to $\overline{BG}_n$	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BR}_a$ to $\overline{BG}_b$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns

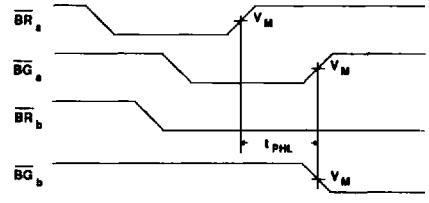
AC WAVEFORMS



Waveform 1. AND Gate Input to Output Delays



Waveform 2. Bus Request or Enable to Bus Grant Delays

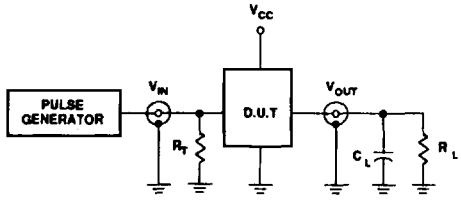


Waveform 3. Bus Request to Bus Grant Delay

NOTE: a and b represent any of the Bus Requests or Grants. $\overline{BG}_a$ Low-to-High transition and the $\overline{BG}_b$ High-to-Low transition occur simultaneously.

For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



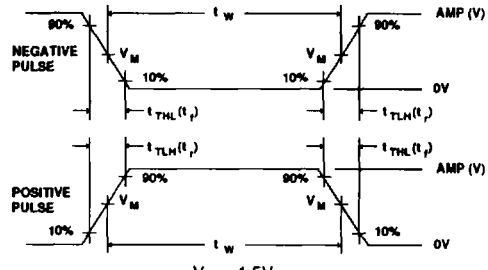
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns