MOTOROLA

MC10901

Advance Information

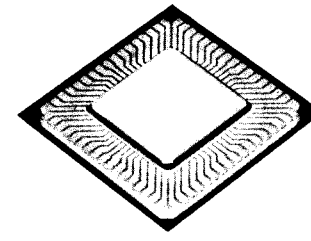
8 X 8 BIT EXPANDABLE MULTIPLIER

The MC10901 is a high speed 8 x 8-bit multiplier that can multiply two eight-bit unsigned or signed 2's complement numbers and generate the sixteen-bit unsigned or signed product. The device can be used as a stand-alone eight-bit multiplier or as a building block for larger multiplier arrays.

The part performs the algebraic function defined as P = XY + K + M + C7, where K and M are 8-bit input fields used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is an asynchronous, sequential add technique. This algorithm eliminates the need for subtractors which simplifies the multiplier network.

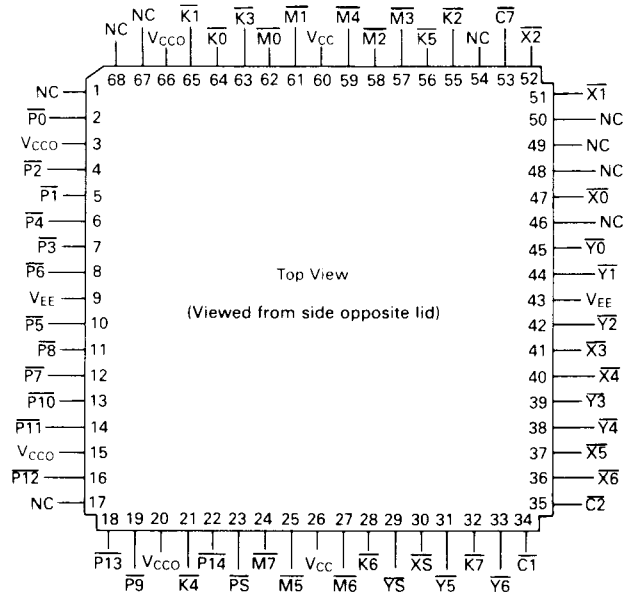
- 8 x 8-Bit Parallel Multiplication.
- Two's complement, Unsigned Magnitude, or Mixed Mode Multiplication.
- Two 8-Bit Expansion Inputs for Summing Partial Products.
- Easily Expandable Into Larger Arrays.
- Single Chip, Bipolar Technology.
- 17 Nanosecond Typical Multiply Time.

MECL-LSI
8 × 8-BIT MULTIPLIER

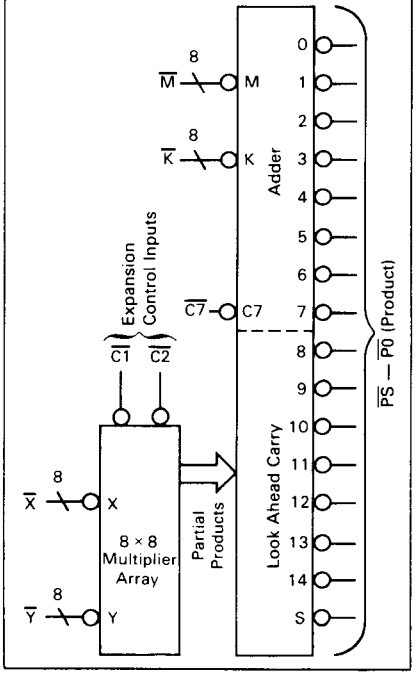


CASE 745 — Z Suffix
68 Pin, JEDEC Std.
Leadless Package
(Bottom view)

INPUT/OUTPUT DIAGRAM



LOGIC DIAGRAM



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The MC10901 is a high-speed programmable 8 x 8-bit multiplier utilizing the MECL Macrocell Array. The MC10901 uses an asynchronous, sequential add technique for multiplying two numbers in either straight magnitude or two's complement notation. The device generates the function: P = X·Y + K + M + C7, where;

· = times
+ = plus
X = 8-bit multiplicand where X0 is LSB, XS is MSB
Y = 8-bit multiplier where Y0 is LSB, YS is MSB
K = 8-bit constant where K0 is LSB, K7 is MSB
M = 8-bit constant where M0 is LSB, M7 is MSB
C7 = 1-bit constant in bit position 2^7
P = 16-bit product where P0 is LSB and PS is MSB

Two control inputs, $\overline{C1}$ and $\overline{C2}$, are provided for simplifying expansion to larger array sizes. The control inputs can be programmed to select either two's complement or straight magnitude multiplication. A carry-lookahead technique is used to further improve multiplier performance.

DEVICE OPERATION

The multiplication matrix for the MC10901 is shown in Table 1. This matrix shows how the MC10901 calculates the product. The product is the binary sum of all the terms in the matrix. Note that all the terms in the matrix show positive values. The MC10901 requires negative or inverted inputs and produces a product of negative or inverted outputs when positive logic is used. If negative logic is used, no inversion is required on the inputs, while the outputs will be the "true" value.

Operation and expansion of the device are controlled by two inputs $\overline{C1}$ and $\overline{C2}$. When $\overline{C2}$ is at a logic H, the X inputs are in straight magnitude form. A low on $\overline{C2}$ indicates the X inputs are in two's complement form. The Y inputs and $\overline{C1}$ function the same as above. For a straight multiply, control inputs are programmed in the high state. For a two's complement multiply $\overline{C1}$ and $\overline{C2}$ are programmed in the low state. Due to the nature of the algorithm, correction terms need to be added to obtain the correct two's complement signed product. The sign bits of the X and Y inputs must be added to the product in their respective bit locations. This can be accomplished by connecting $\overline{X}$s and $\overline{Y}$s to the $\overline{M7}$ and $\overline{K7}$ inputs, see figure 1. For expansion into larger arrays, an additional input, $\overline{C7}$, has been provided. $\overline{C7}$ accomplishes the same function as a $\overline{M7}$ or $\overline{K7}$ input. If a straight magnitude number is to be multiplied by a two's complement number only the sign bit of the two's complement number is to be added in as correction.

EXPANSION RULES

The MC10901 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

1. For an M-bit by N-bit multiplier, an (M + N) bit product is formed. The number of MC10901's equals (M x N) /64. As an example, a 32 x 32-bit array (figure 3) requires (32 x 32) /64 = 16 packages.

TABLE 1 — MULTIPLICATION MATRIX FOR MC10901
(P = (X) times (Y) plus K plus M plus C7)

								C7							
								K7	K6	K5	K4	K3	K2	K1	K0
								M7	M6	M5	M4	M3	M2	M1	M0
								XS·(C2⊕Y0)	X6·Y0	X5·Y0	X4·Y0	X3·Y0	X2·Y0	X1·Y0	X0·Y0
							XS·(C2⊕Y1)	X6·Y1	X5·Y1	X4·Y1	X3·Y1	X2·Y1	X1·Y1	X0·Y1	
						XS·(C2⊕Y2)	X6·Y2	X5·Y2	X4·Y2	X3·Y2	X2·Y2	X1·Y2	X0·Y2		
	C1·C2·$\overline{YS}$				XS·(C2⊕Y3)	X6·Y3	X5·Y3	X4·Y3	X3·Y3	X2·Y3	X1·Y3	X0·Y3			
	C1·C2·$\overline{XS}$			XS·(C2⊕Y4)	X6·Y4	X5·Y4	X4·Y4	X3·Y4	X2·Y4	X1·Y4	X0·Y4				
	C1·$\overline{C2}$·XS·YS		XS·(C2⊕Y5)	X6·Y5	X5·Y5	X4·Y5	X3·Y5	X2·Y5	X1·Y5	X0·Y5					
	$\overline{C1}$·C2·XS·$\overline{YS}$	XS·(C2⊕Y6)	X6·Y6	X5·Y6	X4·Y6	X3·Y6	X2·Y6	X1·Y6	X0·Y6						
C1·C2	XS·YS·(C1⊕C2)	YS·(C1⊕X6)	YS·(C1⊕X5)	YS·(C1⊕X4)	YS·(C1⊕X3)	YS·(C1⊕X2)	YS·(C1⊕X1)	YS·(C1⊕X0)							
PS	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Note: For magnitude operations (C1 = 0, C2 = 0 or C1 = H, C2 = H), the C7 input must be tied to a "High" voltage state in order to eliminate the possibility of overflow and invalid results. For X = 255, Y = 255, K = 255, and M = 255, the product will be the maximum value possible of 65,535 (PS – P0 = 1). If C7 was also used as an input during magnitude operations, the most significant product bit, PS will be a "1" (PS = L) during an overflow condition where the result exceeds 65,535.

For 2's complement or mixed mode multiplications, the multiplication matrix (Table 1) produces the proper product at the PS through P0 outputs.

2. The normal parallelogram structure consists of several stages, each multiplying 8 bits of multiplier times 8 bits of multiplicand and adds the partial products.
3. The sign bits of the multiplicand and multiplier must be added to the product. As an example, an 8 x 16-bit multiplier would require the sign bit of the 8-bit word to be added to the least significant 8th bit of the product. Likewise the sign bit of the 16-bit word is to be added to the least significant 16th bit of the product. The X sign bit and Y sign bit must be added to the product with a binary weight (power of 2) equivalent to their respective binary weights.
4. The control inputs $\overline{C1}$ and $\overline{C2}$ must be programmed correctly depending on the multiplier type and on the position of the MC10901 within the array:
   A) For magnitude arrays, all control inputs are programmed "H".
   B) For two's complement arrays, the programming is controlled by the position of the multiplier and the terms required by the algorithm.

A simple means of determining the required control line states is shown in the following table:

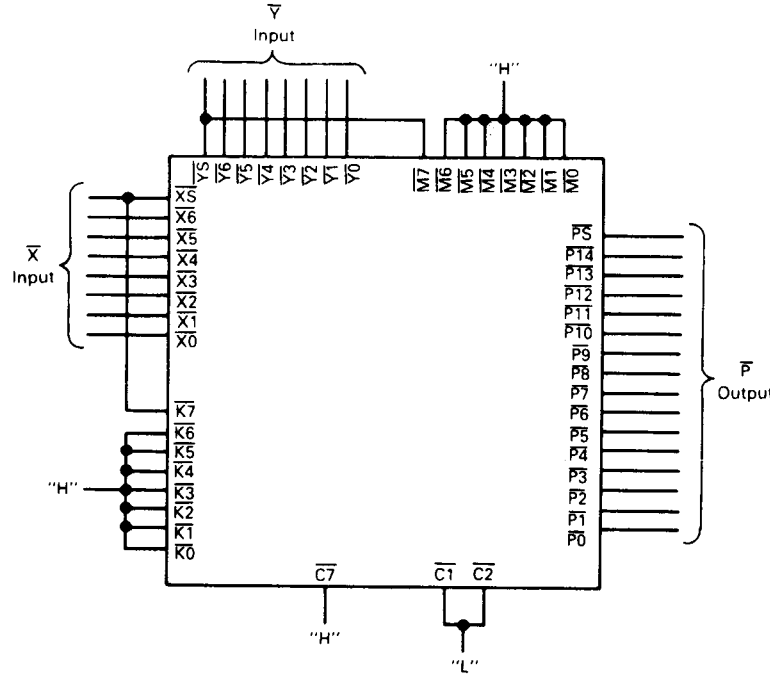
Multiplication Inputs	$\overline{C1}$	$\overline{C2}$
NO SIGN BITS	HI	HI
X_S ONLY	HI	LOW
X_S ONLY	LOW	HI
BOTH SIGN BITS	LOW	LOW

The maximum times possible for various N-bit by N-bit arrays are:

Number Of Bits	Total Multiply Time (ns) Max.	Package Count
8	24.3	1
16	51.8	4
24	81.5	9
32	111.2	16

Because of the versatility of the MC10901, many other arrays can be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can be constructed. Applications of such arrays include digital filters, FFT's, complex multipliers, and recursive and nonrecursive filter elements.

FIGURE 1
8 X 8-Bit 2's Complement Multiplier

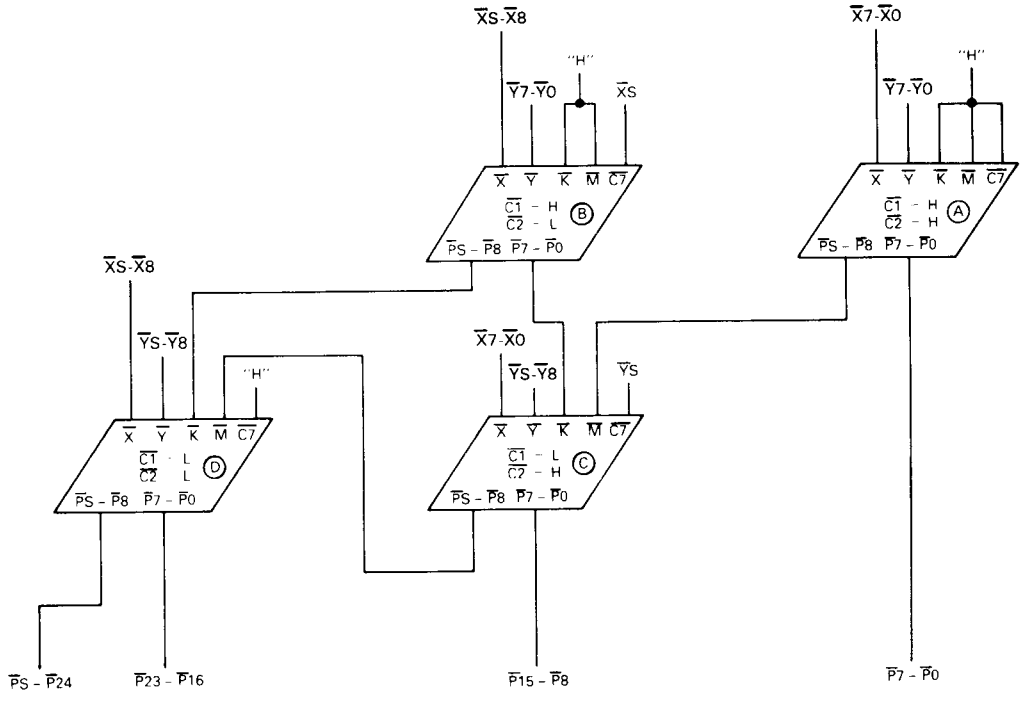


16 X 16-BIT EXAMPLE

Figure 2 shows 4 MC10901's in a 16 x 16-bit array. A 32-bit two's complement product is produced from a 16-bit multiplier and a 16-bit multiplicand. At the first level of multiplication, no partial products have been obtained so the $\overline{K}$ and $\overline{M}$ expansion inputs are tied high. These inputs on the first level can be used to add a constant to the least significant end of the product. Further levels require the $\overline{K}$ and $\overline{M}$ inputs to add the accumulated partial products. Control inputs $\overline{C1}$ and $\overline{C2}$ are programmed according to their relative position of each device in the array. Since both $\overline{X}$ and $\overline{Y}$ are in two's complement form, their respective sign bits must be added to the accumulated products for correction. This can be accomplished by inputing the sign bit of the $\overline{X}$ input to $\overline{C7}$ of device B and sign bit of the $\overline{Y}$ bus to $\overline{C7}$ of device C. The same expansion techniques are extended to the 32 x 32-bit multiplier in Figure 3.

However, when adding the sign bits to the array for correction, the sign bits must be added to the $\overline{C7}$ input of the devices that have $\overline{C1}$ = H, $\overline{C2}$ = L or $\overline{C1}$ = L, $\overline{C2}$ = H in the 32nd bit of the product, as indicated in Figure 3. The sign bits cannot be added to the $\overline{C7}$ input of devices that have $\overline{C1}$ = H and $\overline{C2}$ = H, as indicated in Table 1.

FIGURE 2 — 16 X 16-BIT 2'S COMPLEMENT MULTIPLIER



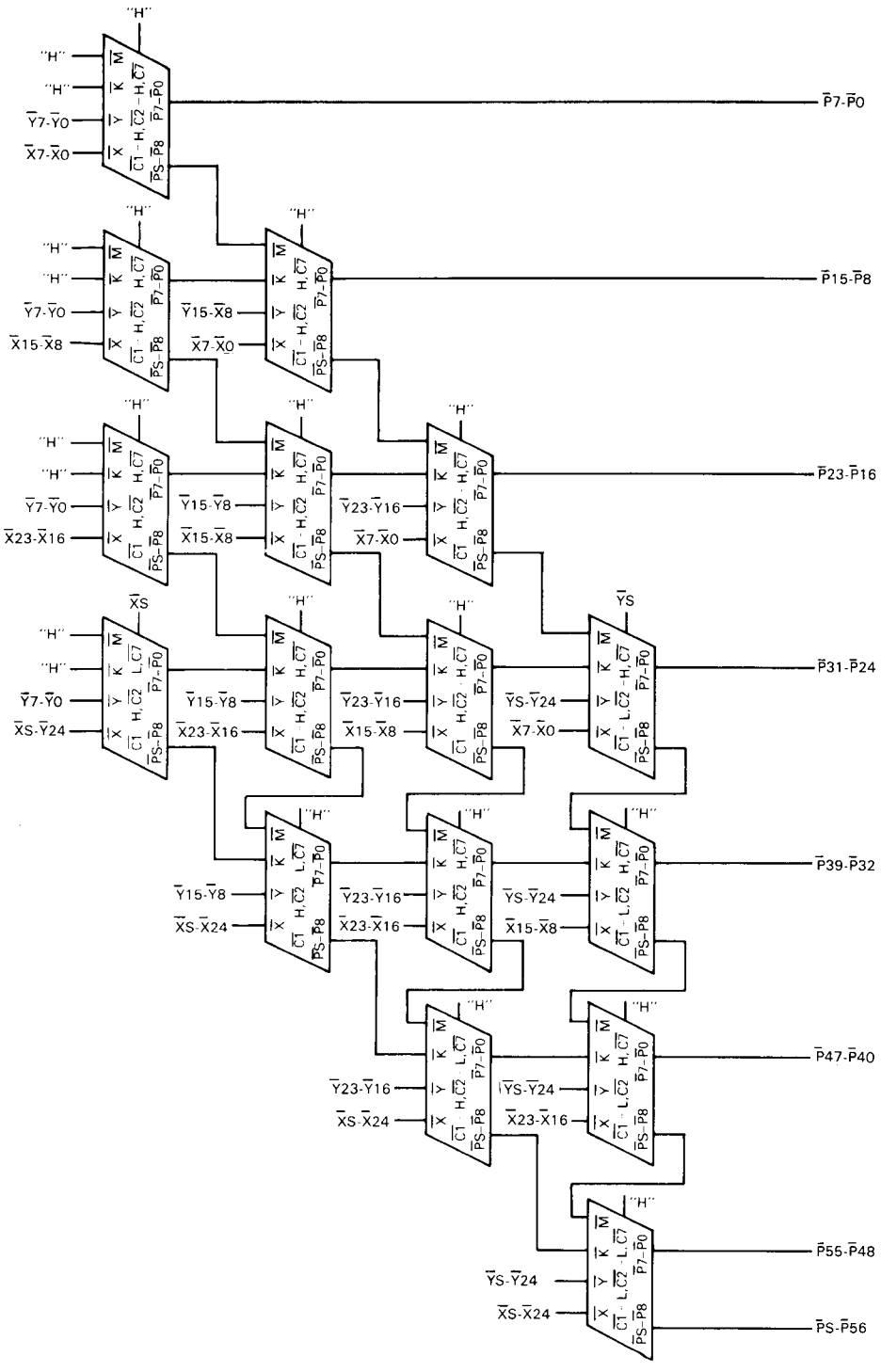


FIGURE 3 — 32 X 32-BIT 2'S COMPLEMENT MULTIPLIER

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TABLE 2 — ABSOLUTE MAX RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_o	<30 <100	mAdc
Storage Temperature	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

TABLE 3 — RECOMMENDED OPERATING CONDITIONS — MC10901

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temperature (Functional)	T_A	0 to +70	°C
Output Drive	—	50 Ω to −2.0 Vdc	—
Max Junction Temp	T_J	130	°C

TABLE 4 — ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board with heatsink and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	Test Voltage Values (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
0°C	−0.840	−1.95	−1.145	−1.490	−5.2
+25°C	−0.810	−1.95	−1.105	−1.475	−5.2
+70°C	−0.730	−1.95	−1.050	−1.450	−5.2

Characteristics	Symbol	Pin Under Test	MC10901 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Unit	Voltage Applied to Pins Listed Below V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CCO}) (V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	9,43	—	868	—	695	868	—	868	mAdc	—	—	—	—	9,43	3,15,20 26,60,66
Input Current C1, C2, X, Y	I_{inH}	—	—	650	—	—	650	—	650	µAdc	47	—	—	—		
K4, M4, M5, M6, M7	I_{inH}	—	—	300	—	—	300	—	300	µAdc	47	—	—	—		
All Others	I_{inH}	—	—	200	—	—	200	—	200	µAdc	47	—	—	—		
	I_{INL}	—	—	—	0.5	—	—	—	—	µAdc	—	47	—	—		
Logic "H" Output Voltage	V_{OH}	2	-1.000	-0.840	-0.960	—	-0.810	0.905	-0.730	Vdc	34,35,53 47	—	—	—		
Logic "L" Output Voltage	V_{OL}	2	-1.950	-1.665	-1.950	—	-1.650	-1.950	-1.625	Vdc	34,35,53	47	—	—		
Logic "H" Threshold Voltage	V_{OHA}	2	-1.02	—	-0.980	—	—	0.925	—	Vdc	34,35,53	—	47	—		
Logic "L" Threshold Voltage	V_{OLA}	2	—	-1.645	—	—	-1.630	—	-1.605	Vdc	34,35,53	—	—	47		

NOTE: All inputs have input pulldown resistors (~68KΩ) between the input and V_{EE}.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

Table 5 defines the timing characteristics of the MC10901 over operating voltage and temperature ranges. Worst-Case Setup and Hold and Propagation Delays are *calculated* for V_{EE} = −5.2 Volts ± 10% and a $T_J$max = 115°C. The maximum recommended operating junction temperature is +130°C.

Calculated limits are based on several performance factors as described in Motorola's Preliminary Design Manual for the MECL 10,000 Macrocell Array. Factors include worst-case delays due to Macro selections, Fan-Out, Metal Lengths, Wire-OR, and Input Follower options. AC measurements are performed on each device to assure process integrity; however, Motorola does not guarantee limits at this time.

FIGURE 4 — SWITCHING WAVEFORM DEFINITION
Propagation Delays

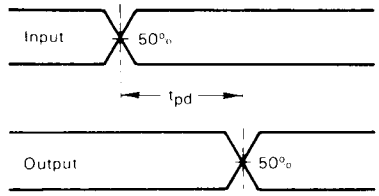


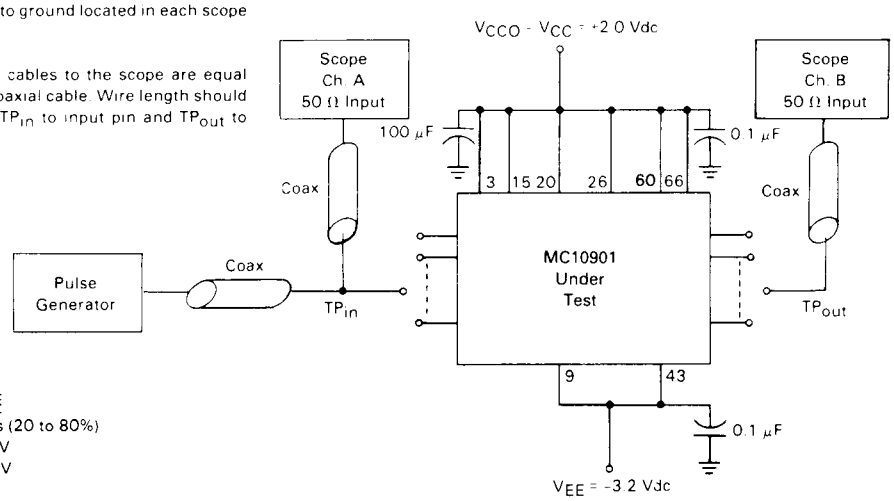
TABLE 5 — PROPAGATION DELAY (Nanoseconds)

Input	Output	0 to 70°C T_A (T_J not to exceed 115°C)	
		Typ	Max
$\overline{X7}$ – $\overline{X0}$, $\overline{Y7}$ – $\overline{Y0}$, $\overline{C1}$, $\overline{C2}$	$\overline{P6}$ – $\overline{P0}$	13.9	19.9
	$\overline{P7}$	13.0	18.6
	$\overline{P14}$ – $\overline{P8}$	17.0	24.3
	$\overline{PS}$	16.3	23.3
$\overline{M7}$ – $\overline{M0}$	$\overline{P6}$ – $\overline{P0}$	7.8	11.2
	$\overline{P7}$	6.9	9.8
	$\overline{P14}$ – $\overline{P8}$	9.3	13.3
	$\overline{PS}$	8.6	12.3
$\overline{K4}$ – $\overline{K0}$	$\overline{P6}$ – $\overline{P0}$	8.2	11.7
	$\overline{P7}$	7.2	10.3
	$\overline{P14}$ – $\overline{P8}$	9.7	13.8
	$\overline{PS}$	8.9	12.7
$\overline{K6}$, $\overline{K5}$	$\overline{P6}$ – $\overline{P0}$	9.4	13.4
	$\overline{P7}$	10.5	15.0
	$\overline{P14}$ – $\overline{P8}$	12.9	18.4
	$\overline{PS}$	12.2	17.4
$\overline{K7}$	$\overline{P7}$	9.9	14.1
	$\overline{P14}$ – $\overline{P8}$	13.9	19.9
	$\overline{PS}$	12.2	18.8
$\overline{C7}$	$\overline{P7}$	10.8	15.4
	$\overline{P14}$ – $\overline{P8}$	14.9	21.2
	$\overline{PS}$	14.1	20.1

FIGURE 5 — SWITCHING TEST CIRCUIT

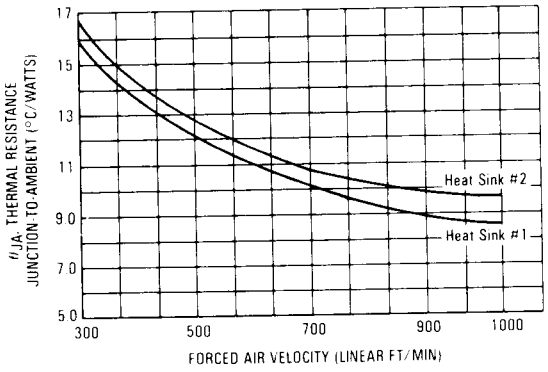
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be 1.4 inch from TP_{in} to input pin and TP_{out} to output pin.



INPUT PULSE
$t_r = t_f$ = 1.0 ns (20 to 80%)
V_{OH} = +1.11 V
V_{OL} = +0.31 V

FIGURE 6 — THERMAL CHARACTERISTICS (TYPICAL)



Heat Sink #1 is from THERMALLOY #15832-1, 3 Horizontal Fins, 0.563 inches square, Model No. 2284C.
Heat Sink #2 is from WAKEFIELD #4493, Vertical Fins, 0.5 inches square.
NOTE: $T_J = (\theta_{JA})(P_D) + T_A$ WHERE T_J is the Junction Temperature, T_A is the Ambient Temperature,
$P_D = (I_{EE})(V_{EE}) + (15\ mW)$ (number of 50 Ω outputs).
Still air θ_{JA} (with no heat sink) = 35°C/W.