INFORMATION STORAGE DEVICES

ISD1000A Series

Single-Chip Voice Record/Playback Devices 16- and 20-Second Durations

GENERAL DESCRIPTION

Information Storage Devices' ISD1000A ChipCorder™ Series provides high-quality, single-chip record/playback solutions for 16- and 20-second messaging applications. The ISD1000A Series replaces the ISD1000 Series, with improved noise characteristics, and it is fully compatible with ISD1000 Series devices. The CMOS devices include an on-chip oscillator, microphone preamplifier, automatic gain control, antialiasing filter, smoothing filter, and speaker amplifier. In addition, the ISD1000A Series is fully microprocessor-compatible, allowing complex messaging and addressing to be achieved.

Recordings are stored in on-board non-volatile memory cells, providing zero-power message storage. This unique solution is made possible through ISD's patented Direct Analog Storage Technology (DAST™), whereby voice and audio signals are stored directly, in their natural analog form, into memory. Direct analog storage allows natural voice reproduction in a single-chip, solid-state solution.

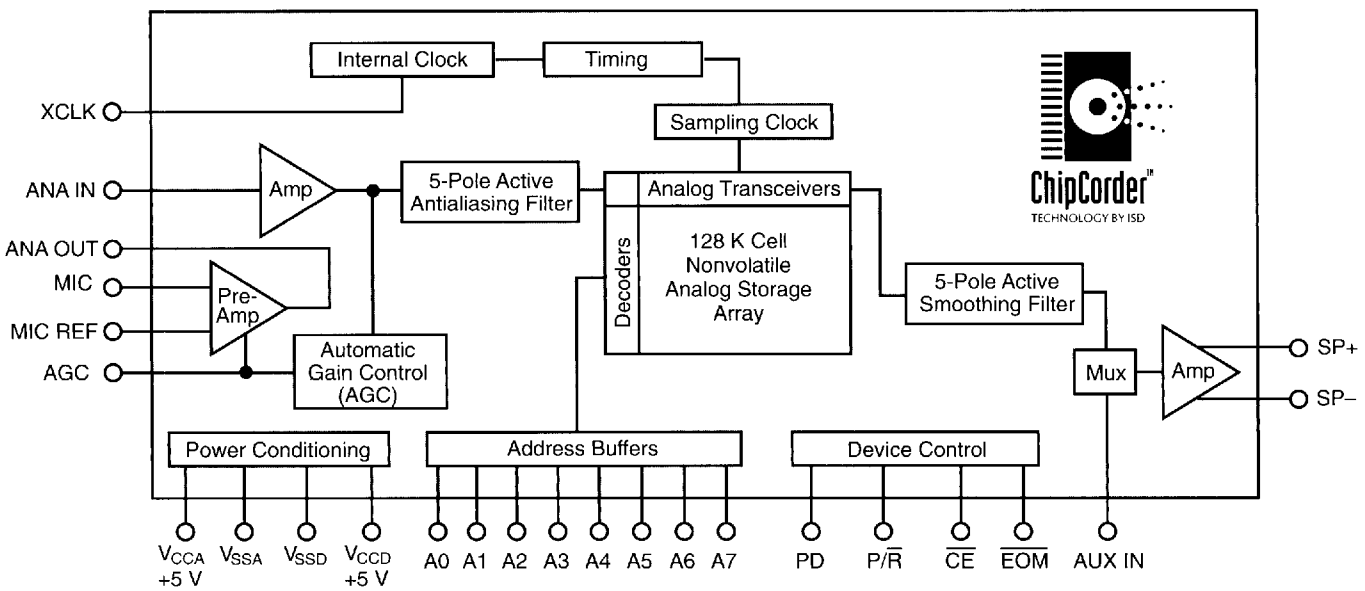
ISD1000A SERIES SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Upper Pass Band (KHz)
ISD1016A	16	8	3.4
ISD1020A	20	6.4	2.7

FEATURES

- **Easy-to-use single-chip voice record/playback solution**
  - No external ICs required
  - No development system required
- **High-quality, natural voice/audio reproduction**
- **Manual switch or microprocessor controllable**
  - Playback can be edge- or level-activated
- **Single-chip durations of 16 and 20 seconds**
- **Directly cascadable for longer durations**
- **Zero-power message storage**
  - Eliminates battery backup circuits
- **Power-Down Mode**
  - 1 µA standby current (typical)
- **Fully addressable to handle multiple messages**
- **100-year message retention (typical)**
- **100K record cycles (typical)**
- **On-chip clock source**
- **On-chip Automatic Gain Control (AGC)**
- **Single +5 Volt Supply**
  - Low-voltage (3.6 V to 4.0 V) versions available
- **Available in die form, DIP, and SOIC packaging**

ISD1000A SERIES BLOCK DIAGRAM



GENERAL DESCRIPTION

The ISD1000A ChipCorder™ Series devices are designed to record and play back audio and voice information in a single chip with a minimum of circuit complexity. This compact, easy-to-use, nonvolatile, low-power solution has been made possible by ISD's patented DAST™ technology — a breakthrough in Direct Analog Storage Technology in EEPROM. ISD's DAST technology results in storage density that is eight times greater than digital memory. The DAST nonvolatile analog array consists of 128K cells — the equivalent of 1 Mbits of digital storage.

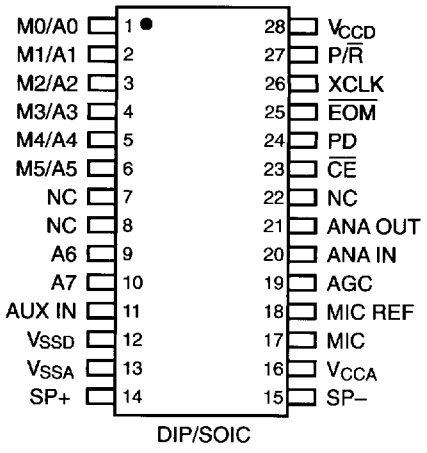
The ISD1000A Series eliminates the need for digital conversion, digital compression, and voice synthesis techniques which often compromise voice quality and are more complicated to use. The ISD1000A Series of devices includes signal conditioning circuits and control functions which enable a complete, high-quality recording and playback system in a single device. The ISD1000A is available in two versions, which store voice in 16- or 20-second DAST arrays. Additional devices may be cascaded to achieve longer recording durations. The nonvolatile storage array is based on production-proven, low-power CMOS EEPROM technology.

The highly integrated ISD1000A Series contains all the basic functions required for high-quality voice recording and playback. The noise-cancelling Microphone Preamplifier and Automatic Gain Control (AGC) record both low-volume and high-volume sounds. The AGC attack and release times are adjusted by an external resistor and capacitor. Antialiasing is performed by a continuous fifth-order Chebyshev filter, requiring no external components or clocks to give toll-quality reproduction. The low corner of the passband is user-settable by two external capacitors. The devices contain their own temperature-stabilized timebase oscillator.

The ISD1000A devices drive a speaker directly through differential outputs. This boosts power by four times and eliminates the need for a series capacitor or an output amplifier. The device will operate from a single 5-volt power supply or from batteries. The device also includes a power down function for applications where minimum power consumption is critical. The CMOS-based design, combined with the nonvolatile storage array, assures the lowest possible overall power consumption.

On-chip control functions make the ISD1000A Series very easy to use in a wide array of applications. Each device offers a variety of operating modes and interface options. The devices may be used in applications that require little more than a few switches and a battery. The devices may also be integrated into electronic systems where digital addresses can be provided for more sophisticated message addressing and control. The

ISD1000A SERIES PINOUTS



DIP/SOIC

ISD1000A DAST arrays are organized in 160 segments. Addresses A0 through A7 provide access to each segment in the array for message addressing. Addressing provides the capability of constructing messages by concatenating stored phrases and sounds.

ISD1000A SERIES — PIN DESCRIPTIONS

Microphone Input (MIC)

An external microphone should be AC coupled to this pin via a series capacitor. The user-selectable value of the input series capacitor, together with the internal 10 KΩ resistance on this pin, determines the low frequency cutoff for the ISD1000A Series passband.

Microphone Reference Input (MIC REF)

By connecting this pin to V_{SSA} (analog ground) via a series capacitor, common mode noise can be rejected at the preamplifier. The capacitor value should be exactly the same value as the input coupling capacitor used for microphone input. Using this approach may provide up to a 10 dB noise improvement. IF THIS INPUT IS UNUSED, IT MUST BE LEFT DISCONNECTED.

Analog Output (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin. It has a maximum gain of about 24 dB for small input signal levels.

Analog Input (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 2.7 KΩ input impedance of ANA IN, can be selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

Automatic Gain Control Input (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 µF give satisfactory results in most cases. For AGC voltages of 1.5 V and below, the preamplifier is at its maximum gain of 24 dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8 V.

Speaker Outputs (SP+/SP-)

The SP+ and SP- pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, however, for direct-drive loudspeakers, the two opposite-polarity outputs give an improvement in output power of up to four times over a single-ended connection. Furthermore, a single-ended connection requires an AC-coupling capacitor between the SP pin and the speaker. When the SP+ and SP- connections are used, this capacitor is not required.

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD1000A devices or the outputs of other speaker drivers.

CONNECTION OF SPEAKER OUTPUTS IN PARALLEL MAY CAUSE DAMAGE TO THE DEVICE. NEVER GROUND OR DRIVE AN UNUSED SPEAKER OUTPUT.

Power Down Input (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When $\overline{EOM}$ pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the Record/Playback space.

Chip Enable Input ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all Playback and Record operations. The address inputs and Playback/Record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. When $\overline{CE}$ is taken HIGH, the ISD1000A is unselected, and the auxiliary input is directed into the speaker amplifier.

Playback/Record Input (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a Playback cycle while a LOW level selects a Record cycle. For a Record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a Record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a Playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an operational mode, or if $\overline{CE}$ is held LOW in address mode. (See Table 1, Page 5 for more Operational Modes).

Address/Mode Inputs (A0-A7)

The Address/Mode Inputs provide two functions in the ISD1000A Series: 1. Message address (A6 or A7 = LOW) and 2. ISD1000A Series Operational Mode Options (A6 AND A7 = HIGH).

Operational mode options are shown in Table 1 (Page 4). There are a maximum of 160 message addresses (or segments). Each segment corresponds to one of 160 rows in the analog storage array. The message addresses (segments) are in locations 0 through 159 contiguous. The playback/record duration of each segment depends upon the device and is as follows:

Part Number	Segment Playback/Record Duration
ISD1016A	0.100 sec.
ISD1020A	0.125 sec.

An operation may be started at any address, as defined by address pins A0-A7. Record or playback continues with automatic incrementing of the internal on-chip address until either $\overline{CE}$ is brought HIGH (Record), an end of message marker is encountered (Playback with $\overline{CE}$ HIGH), or an overflow (device full) condition results.

Optional External Clock Input (XCLK)

This signal is normally tied to ground in application circuits. If, however, greater timing precision is desired, (internal clock has +2.25 % tolerance over temperature and voltage range), the chip can be externally clocked through this pin. For the ISD10xxA"I," (Industrial Temperature), the internal clock variance has a 5% tolerance over the temperature and voltage ranges. A regulated power supply is recommended.

For the ISD1016A the external clock should be a 1024 KHz signal, and for the ISD1020A, a 819 KHz signal. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. IF THE XCLK IS NOT USED, THIS INPUT MUST BE CONNECTED TO GROUND.

End-Of-Message Output ($\overline{EOM}$)

A non-volatile marker is automatically inserted at the end of each recorded message. It remains there until the message

is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message, or in the event of a message overflow (device full).

In addition, the ISD1000A Series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5V. In this case, EOM goes LOW and the device is fixed in Playback-only mode. The $\overline{EOM}$ marker provides a convenient handshake signal for a processor, and also facilitates the cascading of devices.

Auxiliary Input (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH and Playback has ended, or if the device is in overflow. When cascading multiple ISD1000A devices, the AUX IN pin is used to connect a Playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

Voltage Inputs (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD1000A Series devices use separate power busses. These +5 V busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

Ground Inputs (V_{SSA}, V_{SSD})

The ISD1000A Series of devices utilizes separate analog and digital ground busses. These pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground.

OPERATIONAL MODES

The ISD1000A Series is designed with several built-in operational modes provided to allow maximum functionality with a minimum of additional components, described in detail below. The operational modes use the address pins on the ISD1000A devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSBs) are HIGH, the remaining address signals are interpreted as mode bits and NOT as address bits. Therefore, operational modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using operational modes. First, all operations begin initially at address 0, which is the beginning of the ISD1000A address space. Later operations can begin at other address locations, depending on the operational mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from Record to Playback, Playback to Record, or when a Power-Down cycle is executed.

Second, an Operational Mode is executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current address/mode levels are sampled and executed.

(Note: The two MSBs are on pins 9 and 10 for each ISD1000A Series member.)

OPERATIONAL MODE DESCRIPTIONS

The Operational Modes can be used in conjunction with a microcontroller, or they can be hard-wired to provide the desired system operation.

M0 — Message Cueing

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for Playback only, and is typically used with the M4 Operational Mode.

M1 — Delete $\overline{EOM}$ Markers

The M1 Operational Mode allows sequentially recorded messages to be concatenated into a single message with only one $\overline{EOM}$ marker set at the end of the combined message. When this operational mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — Used for Cascading

During playback, $\overline{EOM}$ pulses LOW at array overflow only.

M3 — Message Looping

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message CAN completely fill the ISD1000A device and will loop from beginning to end without $\overline{EOM}$ going LOW.

M4 — Consecutive Addressing

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 — $\overline{CE}$ Level Activated

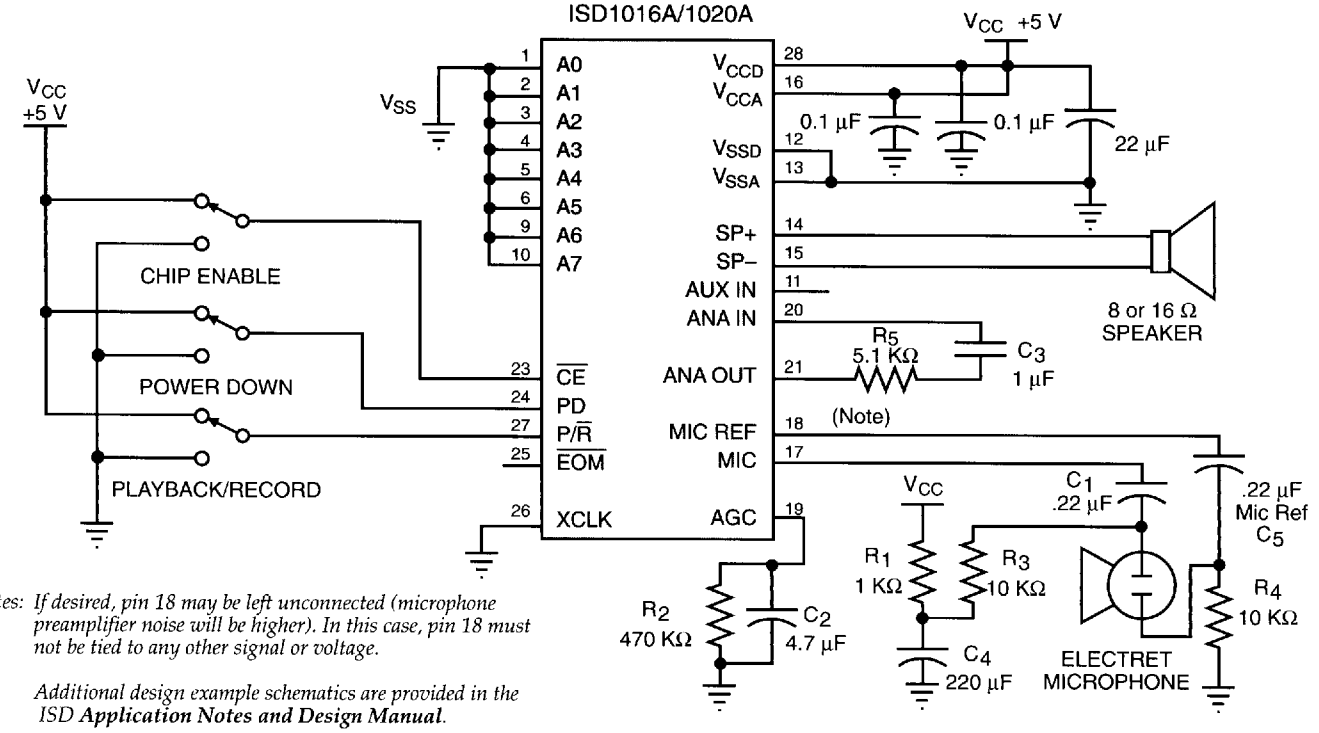
The default mode for ISD1000A devices is for CE to be edge-activated on Playback and level-activated on Record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during Playback. This is specifically useful for terminating Playback operations using the $\overline{CE}$ signal. In this mode, $\overline{CE}$ LOW begins a Playback cycle, $\overline{CE}$ HIGH stops the cycle, and $\overline{CE}$ LOW again will begin playing at the point where the message was stopped without resetting the address pointer.

TABLE 1. OPERATIONAL MODES

Mode Control	Function	Typical Use	Jointly* Compatible
M0	Message cueing	Fast-forward through messages	M4, M5
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5
M2	Cascading	Adding devices to extend duration	
M3	Looping	Continuous playback from address 0	M1, M5
M4	Consecutive addressing	Record/Play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0,M1, M3, M4

** Indicates additional operational modes which can be used simultaneously with the given mode.*

APPLICATION EXAMPLE – DESIGN SCHEMATIC



Notes: If desired, pin 18 may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage.

*Additional design example schematics are provided in the ISD **Application Notes and Design Manual**.*

APPLICATION EXAMPLE – BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power up chip and select record/playback mode	1. PD = LOW 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A7
3	Begin playback/record	$\overline{CE}$ = Pulsed LOW
4	End cycle	$\overline{CE}$ = HIGH and $\overline{EOM}$ reached

APPLICATION EXAMPLE – PASSIVE COMPONENTS

Part	Function	Comments
R1	Microphone power supply decoupling	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3	Microphone biasing resistor	Provides biasing for microphone operation
C1	Microphone DC–blocking capacitor. Low-frequency cutoff	Decouples microphone bias from chip. Provides single-pole low-freq. cutoff
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low-frequency cutoff capacitor	Provides additional pole for low-frequency cutoff
C4	Microphone power supply decoupling	Reduces power supply noise
C5	Common-mode capacitor	Provides common-mode noise rejection

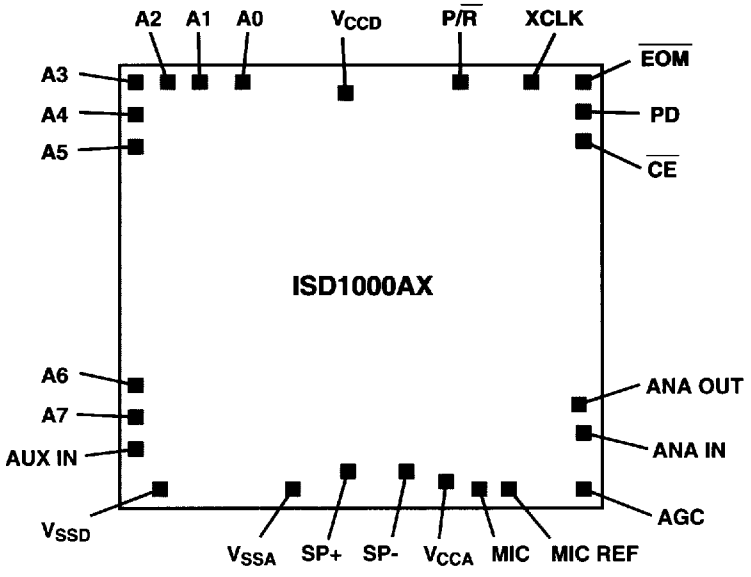
DIE BONDING PHYSICAL LAYOUT (1)

ISD1000AX

I. Die Dimensions
X: 5359 microns
Y: 5258 microns

II. Die Thickness
425 microns

III. Pad Opening
109 microns (4.3 mils)



PIN/PAD DESIGNATIONS (1,2)

Pin	Pin Name	X Axis	Y Axis	Pin	Pin Name	X Axis	Y Axis
A0	Address	-1712.5	2445.5	V_{CCA}	V_{CC} Analog Power Supply	952.5	-2412
A1	Address	-2068	2445.5	MIC	Microphone Input	1217.5	-2459
A2	Address	-2278	2445.5	MIC REF	Microphone Reference	1439	-2459
A3	Address	-2509.5	2368	AGC	Automatic Gain Control	2450.5	-2410
A4	Address	-2509.5	2145.5	ANA IN	Analog Input	2484.5	-1980.5
A5	Address	-2509.5	1885.5	ANA OUT	Analog Output	2466.5	-1715.5
A6	Address	-2509.5	-1525.5	$\overline{CE}$	Chip Enable	2495.5	1989
A7	Address	-2509.5	-1764	PD	Power Down	2495.5	2201
AUX IN	Auxiliary Input	-2509.5	-2178.5	$\overline{EOM}$	End of Message	2493	2443
V_{SSD}	V_{SS} Digital Power Supply	-2359.5	-2456.5	XCLK	External Clock	1970	2445.5
V_{SSA}	V_{SS} Analog Power Supply	-469.5	-2456.5	P/$\overline{R}$	Playback/Record	900	2445.5
SP+	Speaker Output +	-29	-2362.5	V_{CCD}	V_{CC} Digital Power Supply	-52.5	2390
SP–	Speaker Output –	508	-2362.5				

Note: 1. Applies to ISD1000A Series product fabricated subsequent to February, 1993.
2. Pad coordinates (in microns) relative to die center

ABSOLUTE MAXIMUM RATINGS

Condition	Value
Temperature under bias	–65° C to +125° C
Storage temperature range	–65° C to +150° C
Voltage applied to any pin	(V_{SS} - 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ± 20 mA)	(V_{SS} - 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300° C
V_{CC} - V_{SS}	- 0.3 V to + 7.0 V

Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

DC PARAMETERS

Operating Conditions: T_A = 0° C to 70° C (1), V_{CC} = 4.5 V to 6.5 V (2), V_{SS} = 0 V (3); unless otherwise noted

Symbol	Parameters	Min	Typ (4)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = - 1.6 mA
V_{OH1}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = - 10 µA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	R_{EXT} = ∞ (5)
I_{SB}	V_{CC} Current (Standby)		1	10	µA	(5)
I_{IL}	Input Leakage Current			±1	µA	
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R_{AUX}	AUX Input Resistance		10		KΩ	
$R_{ANA\ IN}$	ANA IN Input Resistance		3.0		KΩ	
A_{PRE1}	Preamp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Preamp Gain 2		-45	15	dB	AGC = 2.5 V
A_{AUX}	AUX IN/SP+ Gain	0.9		1.0	V/V	
A_{ARP}	ANA IN to SP+/-		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Preamp Out Source		-1		mA	@ V_{OUT} = 1.0 V
I_{PREL}	Preamp In Sink		0.8		mA	@ V_{OUT} = 2.0 V

Notes: 1. Case temperature.
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.
4. Typical values @ T_A = 25° C and 5.0 V.
5. V_{CCA} and V_{CCD} connected together.

AC PARAMETERS (ISD1016A — 16-SECOND DURATION)

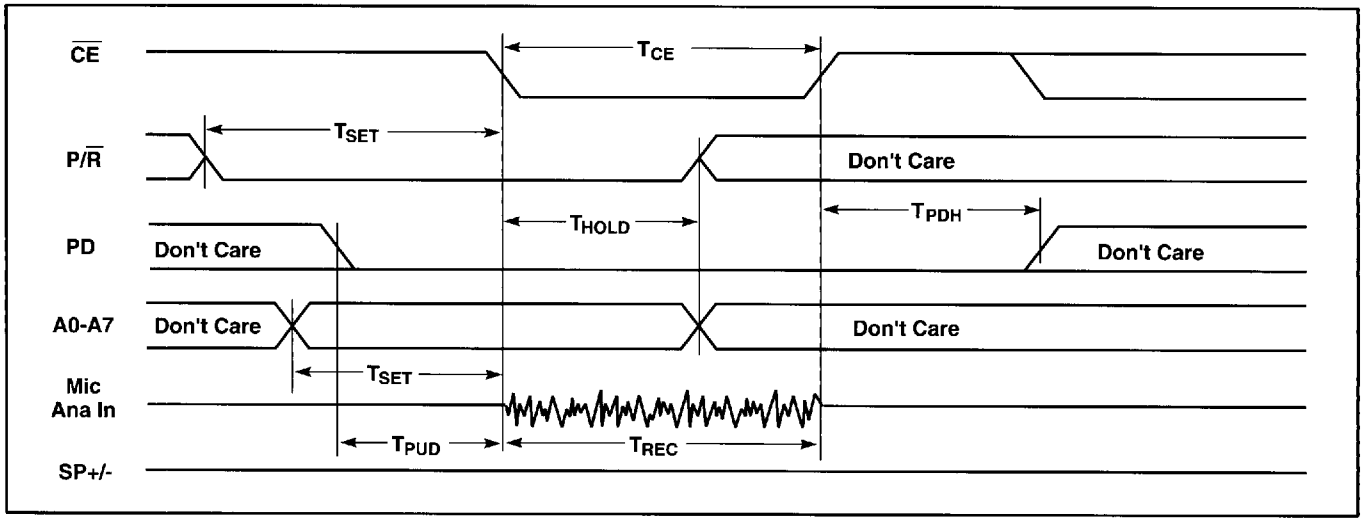
Operating Conditions: T_A = 25° C to 70° C (1), V_{CC} = 4.5 V to 6.5 V (2), V_{SS} = 0 V (3); unless otherwise noted

Symbol	Characteristic	Min	Typ (4)	Max	Units	Conditions
FS	Internal Clock Sampling Freq.		8		KHz	
BW	Passband (5)		3400		Hz	
THD	Total Harmonic Distortion		1		%	@ 1 KHz
P_{OUT}	Speaker Output Power			50	mW	R_{EXT} = 16 Ω (6)
V_{OUT}	Voltage Across Speaker Pins			2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	Mic Input Voltage			20	mV	Peak-to-Peak (7)
V_{IN2}	Ana In Input Voltage			50	mV	Peak-to-Peak
V_{IN3}	Aux In Input Voltage			1.25	V p-p	R_{EXT} = 16 Ω
T_{SET}	Control/Address Setup Time	300			nsec	
T_{HOLD}	Control/Address Hold Time	0			nsec	
T_{CE}	$\overline{CE}$ Pulse Width	100			nsec	
T_{PUD}	Power-Up Delay	18.75			msec	
T_{PDR}	PD Pulse Width - Record		25		msec	
T_{PDP}	PD Pulse Width - Play		12.5		msec	
T_{PDS}	PD Pulse Width - Static		100		nsec	
T_{PDH}	Power Down Hold	0			nsec	
T_{REC}	Record Time		16		sec	
T_{PLAY}	Playback Time		16		sec	
T_{EOM}	$\overline{EOM}$ Pulse Width		12.5		msec	

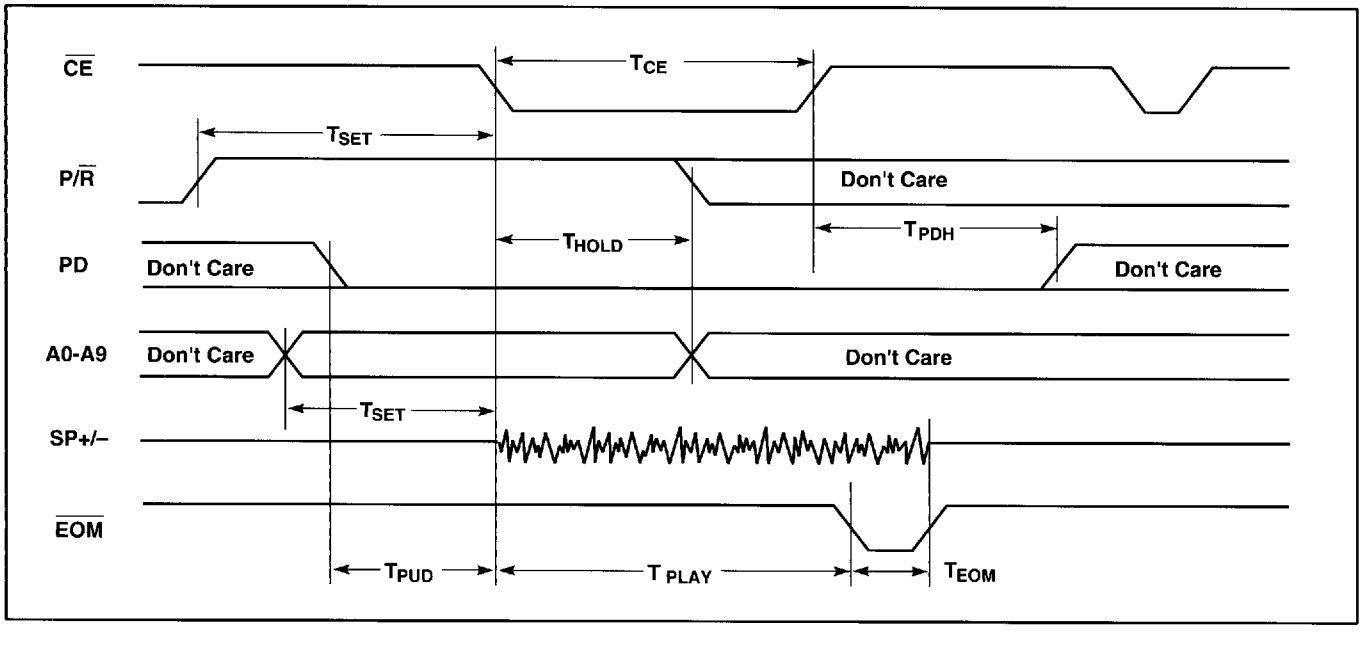
Notes: 1. Case temperature.
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.
4. Typical values @ T_A = 25° C and 5.0 V.
5. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
6. From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.
7. With 12 KΩ series resistor at ANA IN.

TIMING DIAGRAMS (ISD1016A)

RECORD



PLAYBACK



AC PARAMETERS (ISD1020A — 20-SECOND DURATION)

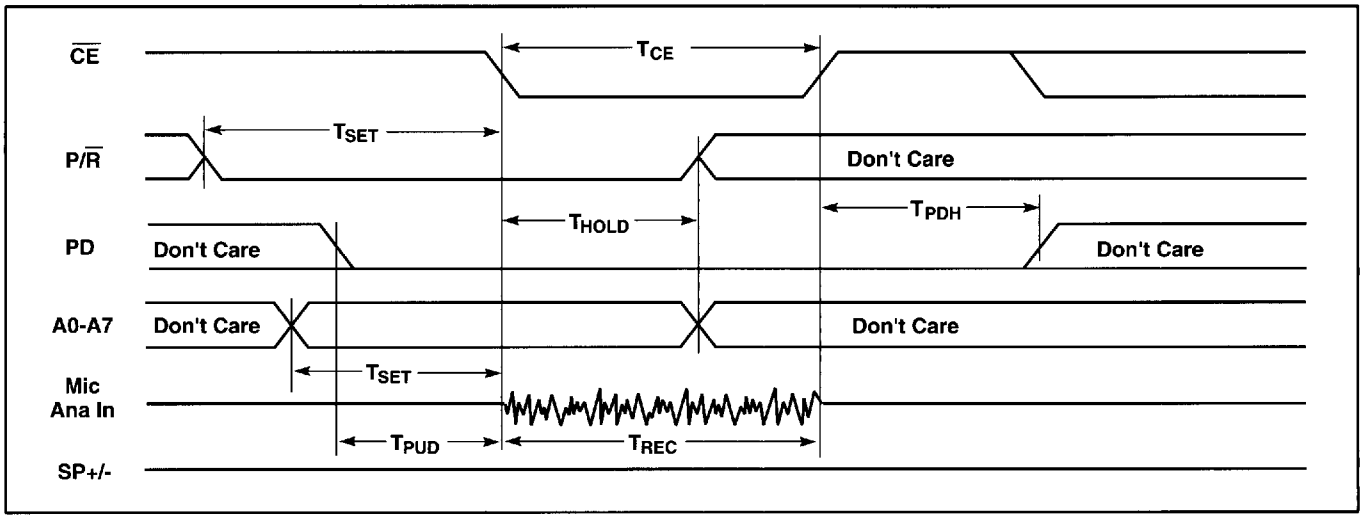
Operating Conditions: T_A = 25° C to 70° C (1), V_{CC} = 4.5 V to 6.5 V (2), V_{SS} = 0 V (3); unless otherwise noted

Symbol	Characteristic	Min	Typ (4)	Max	Units	Conditions
FS	Internal Clock Sampling Freq.		6.4		KHz	
BW	Passband (3)		2700		Hz	
THD	Total Harmonic Distortion		1		%	@ 1 KHz
P_{OUT}	Speaker Output Power			50	mW	R_{EXT} = 16 Ω (6)
V_{OUT}	Voltage Across Speaker Pins			2.5	V p-p	R_{EXT} = 600 Ω
V_{IN1}	Mic Input Voltage			20	mV	Peak-to-Peak (7)
V_{IN2}	Ana In Input Voltage			50	mV	Peak-to-Peak
V_{IN3}	Aux In Input Voltage			1.25	V p-p	R_{EXT} = 16 Ω
T_{SET}	Control/Address Setup Time	300			nsec	
T_{HOLD}	Control/Address Hold Time	0			nsec	
T_{CE}	$\overline{CE}$ Pulse Width	100			nsec	
T_{PUD}	Power-Up Delay	31.25			msec	
T_{PDR}	PD Pulse Width - Record		31.25		msec	
T_{PDP}	PD Pulse Width - Play		15.625		msec	
T_{PDS}	PD Pulse Width - Static		100		nsec	
T_{PDH}	Power Down Hold	0			nsec	
T_{REC}	Record Time		20		sec	
T_{PLAY}	Playback Time		20		sec	
T_{EOM}	$\overline{EOM}$ Pulse Width		15.6		msec	

Notes: 1. Case temperature.
2. $V_{CC} = V_{CCA} = V_{CCD}$.
3. $V_{SS} = V_{SSA} = V_{SSD}$.
4. Typical values @ T_A = 25° C and 5.0 V.
5. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
6. From AUX IN; if ANA IN is driven at 50 mV p-p, the P_{OUT} = 12.2 mW, typical.
7. With 12 KΩ series resistor at ANA IN

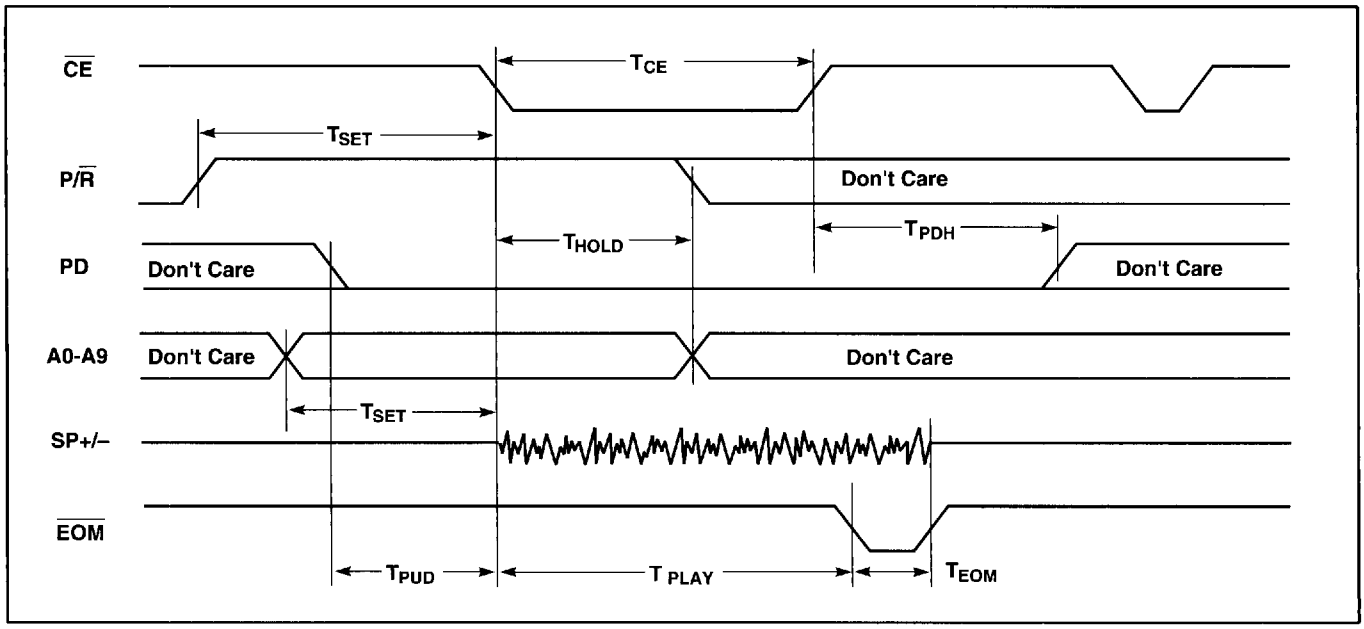
TIMING DIAGRAMS (ISD1020A)

RECORD



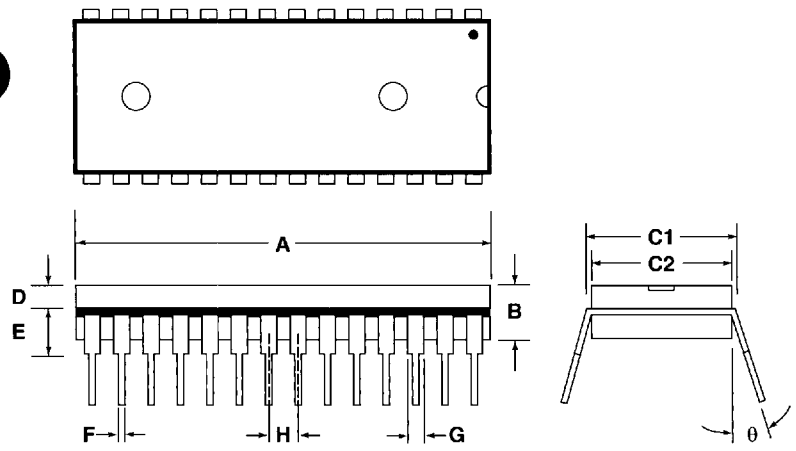
TIMING DIAGRAMS (ISD1020A, CONT.)

PLAYBACK



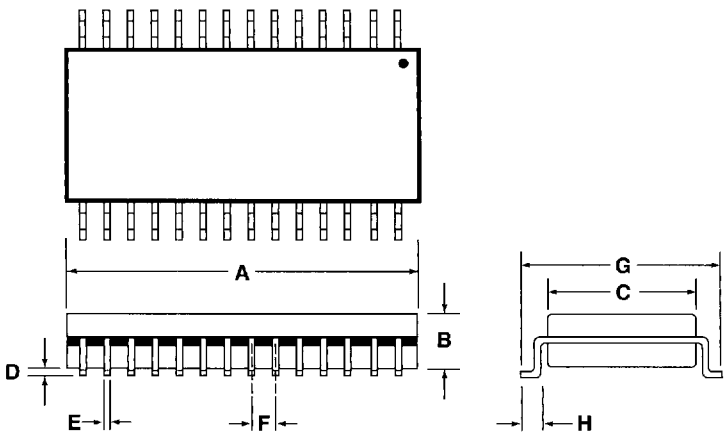
PACKAGE DIAGRAMS

28-Lead Plastic Dual In-Line Package (DIP) Type P



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.7	36.83	36.95
B		.150			3.89	
C1	.600		.625	15.24		15.88
C2	.530	.540	.550	13.46	13.72	13.97
D	1.25	1.30	1.35	2.92	3.05	3.18
E	.125	.130	.135	3.18		3.43
F	.015	.018	.022	0.38	0.46	0.56
G	.055	.060	.065	1.40	1.52	1.65
H		.100			2.54	
θ	0°	7°	15°	0°	7°	15°

28-Lead Plastic Small Outline Package (SOIC) Type G



	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	.706	.714	.718	17.93	18.14	18.24
B	.086	.088	.090	2.18	2.24	2.29
C	.340	.346	.350	8.64	8.79	8.89
D	.004	.007	.010	.102	.178	.254
E	.014	.016	.020	.360	.410	.480
F		.050			1.27	
G	.463	.470	.477	11.76	12.00	12.12
H	.020	.031	.042	.510	.790	1.07

ORDERING INFORMATION

When placing an order for the ISD1000A Series devices, please refer to the following part numbers:

Part No.	Rec/Play Duration	Description
ISD1016AP	16 sec.	28-pin plastic dual in-line package (DIP)
ISD1016API	16 sec.	Industrial Temperature, -40°C to 85°C (DIP)
ISD1016APL*	16 sec.	Low Voltage, 3.6 V to 4.0 V (DIP)
ISD1016AG	16 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1016AGI	16 sec.	Industrial Temperature, -40°C to 85°C (SOIC)
ISD1016AGL*	16 sec.	Low Voltage, 3.6 V to 4.0 V (SOIC)
ISD1016AX	16 sec.	Bare unpackaged die
ISD1020AP	20 sec.	28-pin plastic dual in-line package (DIP)
ISD1020API	20 sec.	Industrial Temperature, -40°C to 85°C (DIP)
ISD1016APL*	20 sec.	Low Voltage, 3.6 V to 4.0 V (DIP)
ISD1020AG	20 sec.	28-lead small-outline integrated circuit (SOIC)
ISD1020AGI	20 sec.	Industrial Temperature, -40°C to 85°C (SOIC)
ISD1016AGL*	20 sec.	Low Voltage, 3.6 V to 4.0 V (SOIC)

** Note: Please contact your ISD Sales Office or Representative for ISD1000A"L" (Low Voltage) Data Sheet Addendum.*

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Information contained in this ISD1000A Series product specification supersedes all data for the ISD1000A Series products published by ISD prior to October, 1993.

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