THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

TSPC860

PRELIMINARY

32 BIT QUAD INTEGRATED POWER QUICC™ COMMUNICATION CONTROLLER

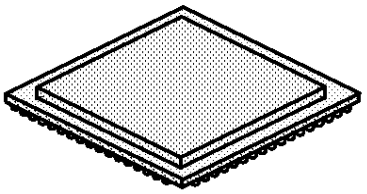
DESCRIPTION

The TSPC860 PowerPC™ QUad Integrated Communication Controller (**Power QUICC™**) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications and networking systems. The Power QUICC (pronounced "quick") can be described as a PowerPC-based derivative of TS68EN360 (QUICC™).

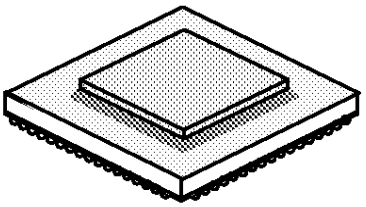
The CPU on the TSPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data caches. The communications processor module (CPM) of the TS68360 QUICC has been enhanced with the addition of the interprocessor-integrated controller (I^2C) channel. Moderate to high digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the TSPC860 to support any type of memory, including high performance memories and newer dynamic random access memories (DRAMs). Overall system functionality is completed with the addition of a PCMCIA socket controller supporting up to two sockets and a real-time clock.

MAIN FEATURES (see also page 5)

- PowerPC single issue integer core.
- Precise exception model.
- Extensive system development support
  - on-chip watchpoints and breakpoints,
  - program flow tracking,
  - On-chip emulation (OnCE) development interface.
- High performance (52 K Dhrystone 2.1 MIPS @50 MHz, 3.3 V, 1.3 Watts total power).
- Low power (< 241 mW @25 MHz, 2.4 V internal, 3.3 V I/O-core, caches, MMUs, I/O).
- MPC8XX PowerPC system interface, including a periodic interrupt timer, a bus monitor, and real-time clocks.
- CPU32+ Processor (4.5 MIPS at 25 MHz)
  - 32-bit version of the CPU32 Core (fully compatible with the CPU32),
  - Background Debug Mode,
  - Byte-Misaligned Addressing.
- Up to 32-bit Data Bus
  (Dynamic Bus Sizing for 8 and 16 bits).
- Fully Static Design).
- V_{CC} = +3.3 V.
- f_{max} = 40 MHz (66 MHz : tbc).
- Military temperature range : –55°C < T_C < +125°C.
- P_D = typ 0.9 W (0.25 to 1.3 Watts).



PBGA 357
ZP suffix



CBGA 357 (to be confirmed)
G suffix

SCREENING / QUALITY

This product will be manufactured in full compliance with :

- Mil-STD-883 class B (tbc).
- DSCC / QML (tbc).
- Or according to TCS standard.

1. TSPC860 ARCHITECTURE OVERVIEW

The TSPC860 is functionally composed of three major blocks :

- A 32–bit PowerPC core with MMUs and caches
- A system interface unit
- A communications processor module

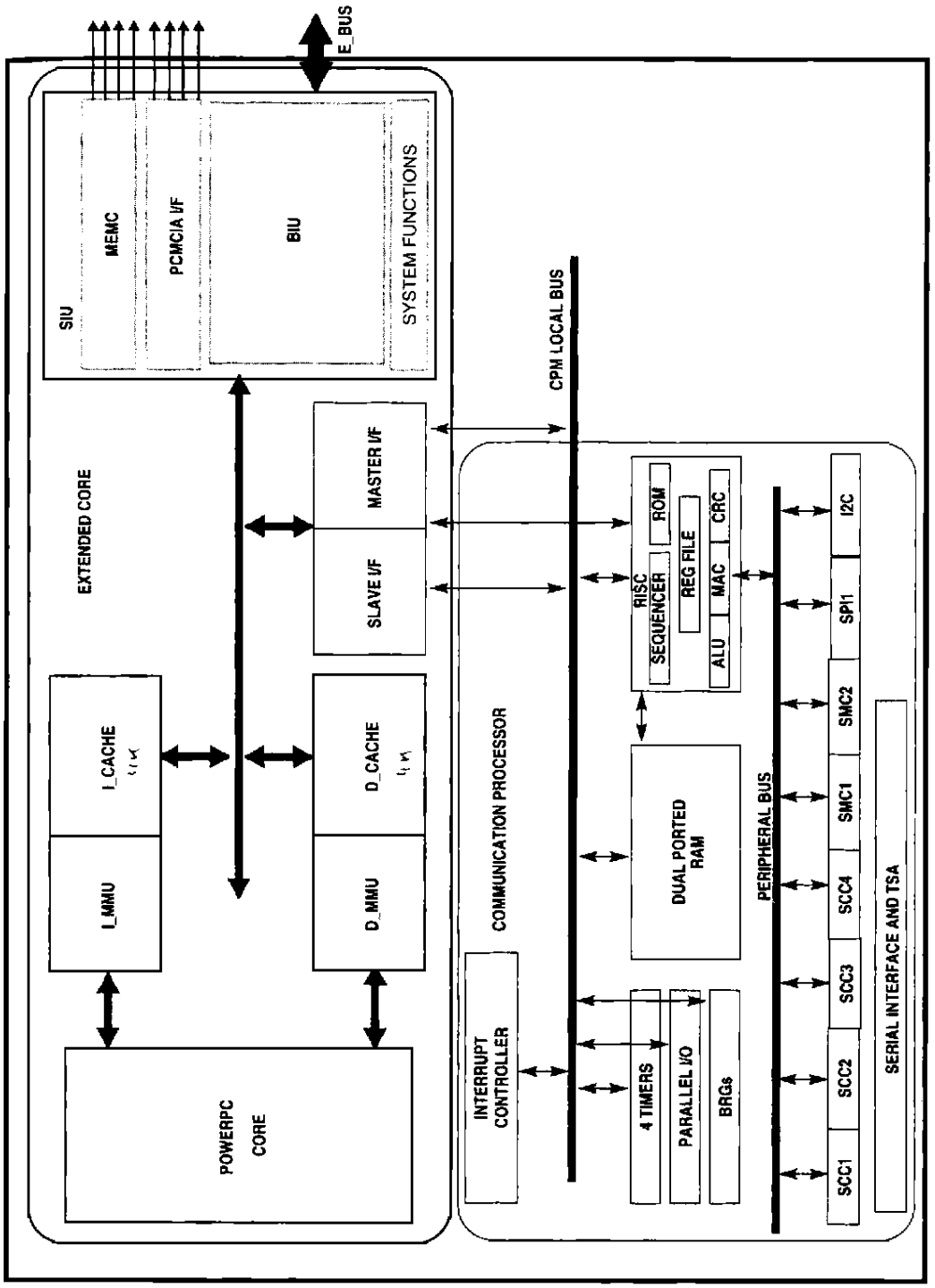
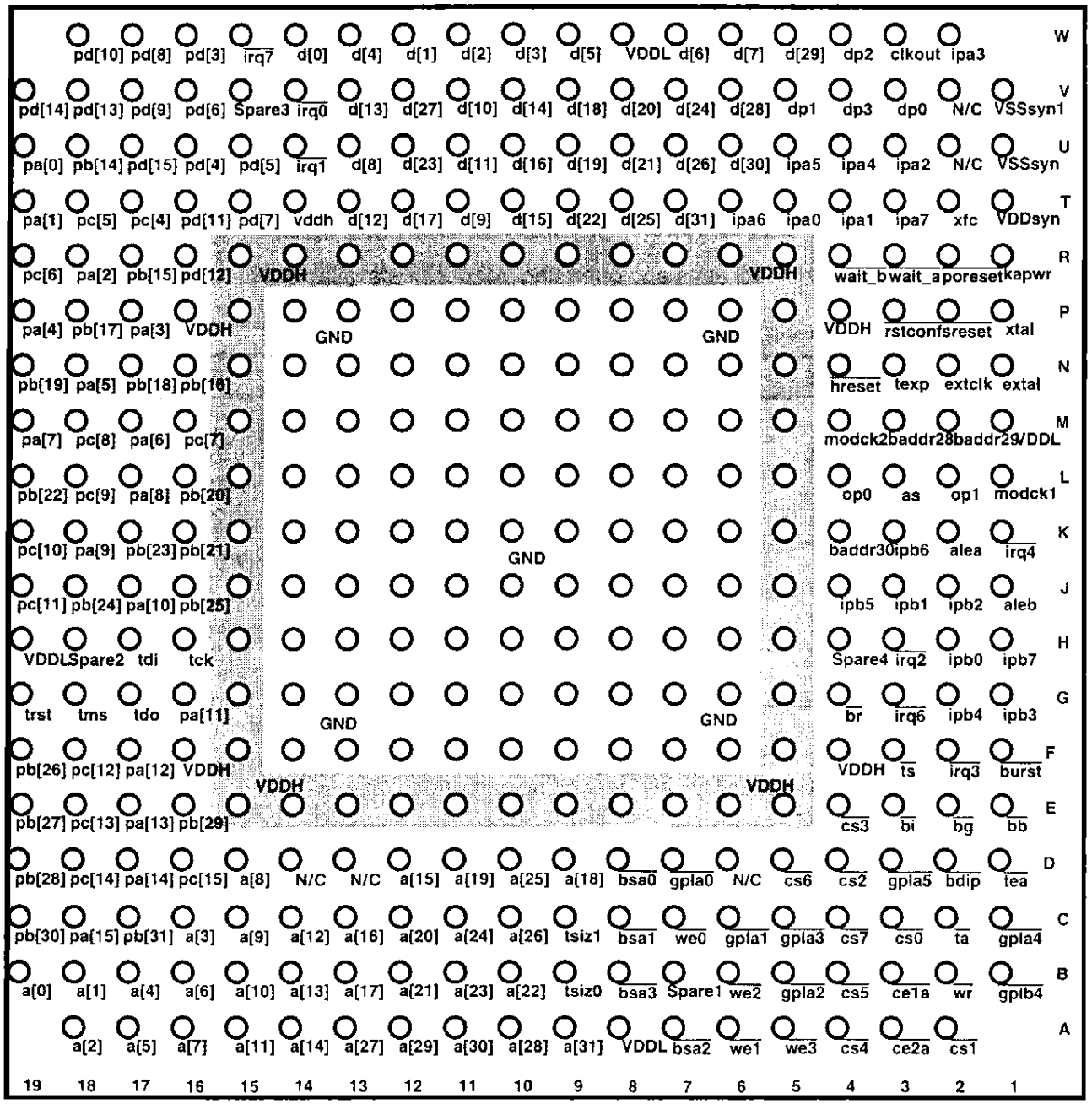


Figure 1 : **Block diagram view of the TSPC860**

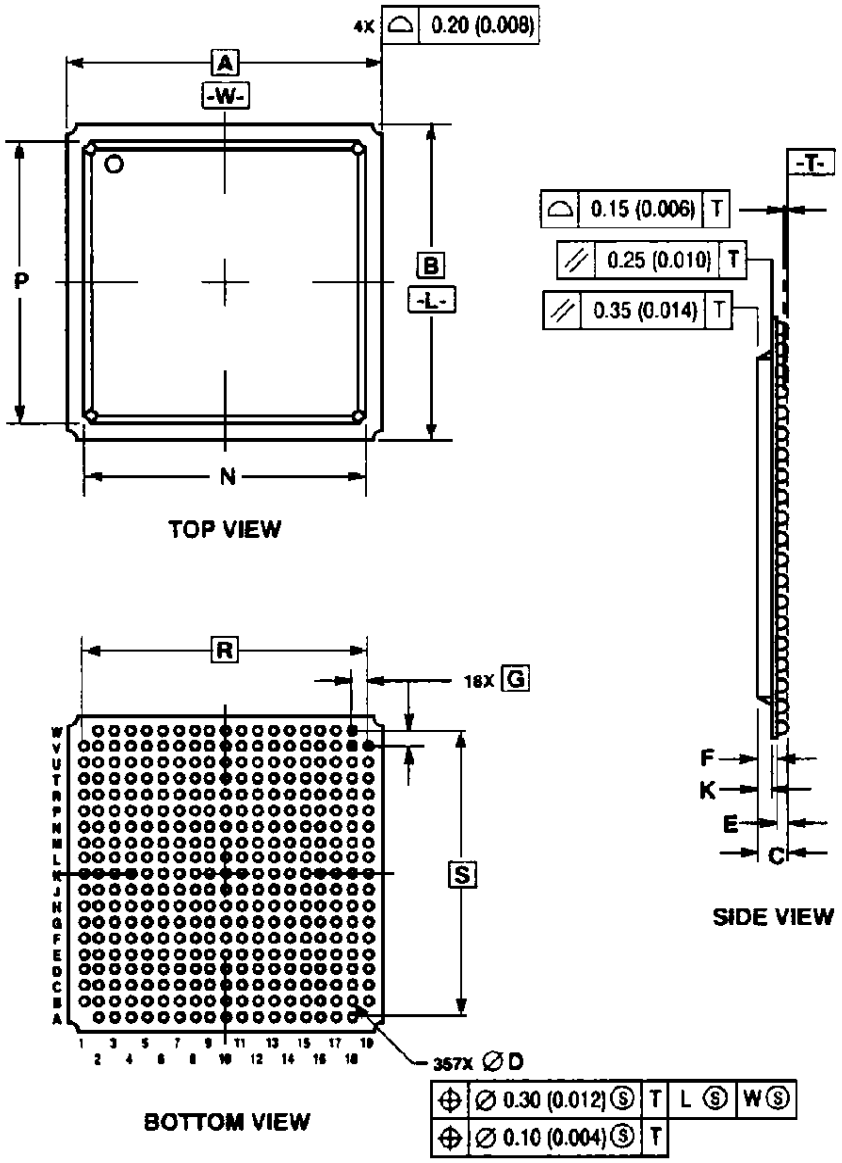
2. PIN ASSIGNEMENT - PBGA



TOP VIEW

3. PACKAGE DIMENSIONS

3.1. Plastic Ball Grid Array



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.00 BSC		0.984 BSC	
B	25.00 BSC		0.984 BSC	
C	---	2.05	---	0.081
D	0.60	0.90	0.024	0.035
E	0.50	0.70	0.020	0.028
F	0.95	1.35	0.037	0.053
G	1.27 BSC		0.50 BSC	
K	0.70	0.90	0.028	0.035
N	22.40	22.60	0.882	0.890
P	22.40	22.60	0.882	0.890
R	22.86 BSC		0.900 BSC	
S	22.86 BSC		0.900 BSC	

Note : For more information on the printed circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to AN-1232,"Plastic Ball Grid Array Application Note" available from your local Motorola sales office.

3.2. Ceramic Ball Grid Array

To be confirmed

4. POTENTIAL AVAILABLE VERSION

Device	Number of SCCS	ATM support	Ethernet support	Multi-Channel HDLC support
MPC860DC	2	–	SCCI	–
MPC860DE	2	–	Yes	–
MPC860DH	2	–	Yes	Yes
MPC860	4	–	–	–
MPC860EN	4	–	Yes	–
MPC860MH	**4**	**–**	**Yes**	**Yes**
MPC860SAR		Yes	Yes	Yes
MPC860T	4	–	10/100	Yes

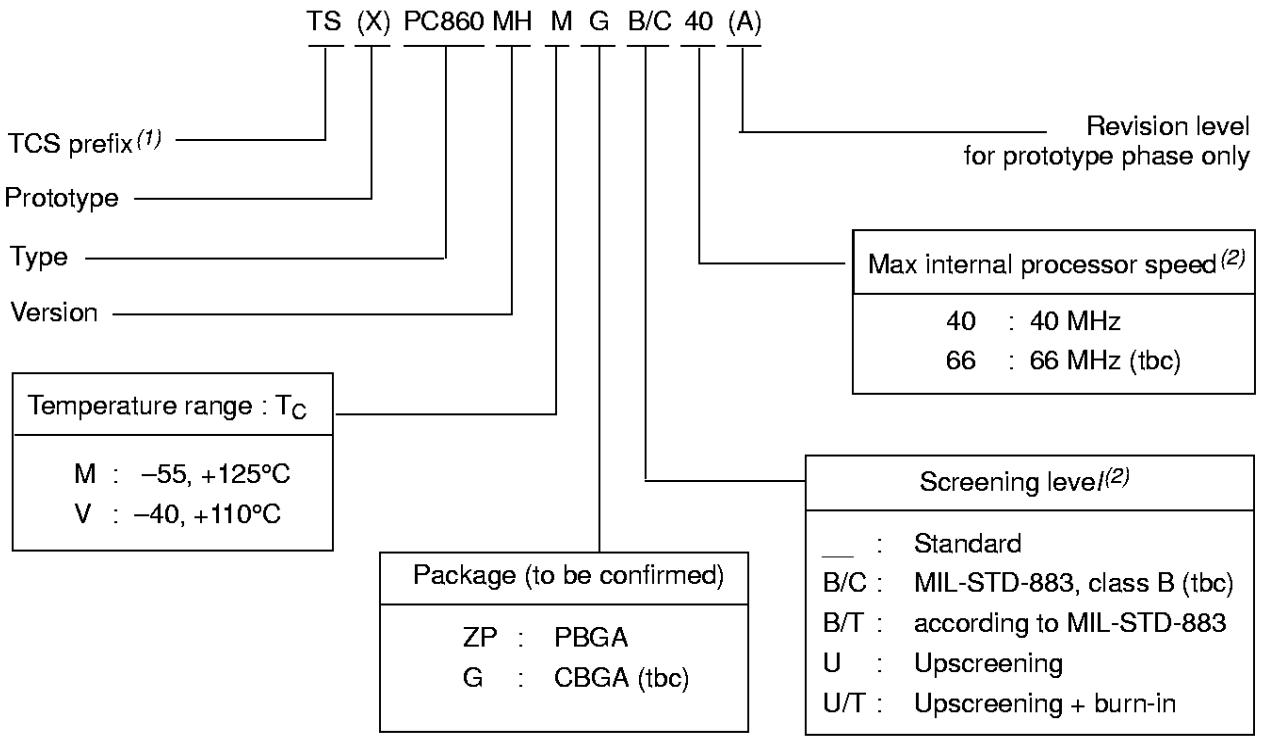
TCS is intending to introduce only the "MH" version

5. MAIN FEATURES (Cont'd)

- Fully static design
- Four major power saving modes
- 357 OMPAC ball grid array packaging (plastic)
- 32-bit address and data busses
- Flexible memory management
- 4-kbyte physical address, two-way, set-associative data cache
- 4-kbyte physical address, two-way, set-associative instruction cache
- Eight–bank memory controller
  - Glueless interface to SRAM, DRAM, EPROM, FLASH and other peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with bit masks
- System interface unit
  - Clock synthesizer
  - Power management
  - Reset controller
  - PowerPC decrementer and time base
  - Real-time clock register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1 JTAG test access port
- Communications processor module
  - Embedded 32-bit RISC controller architecture for flexible I/O
  - Interfaces to PowerPC core through on-chip dual-port RAM and virtual DMA channel controller
  - Continuous mode transmission and reception on all serial channels
  - Serial DMA channels for reception and transmission on all serial channels
  - I/O registers with open-drain and interrupt capability
  - Memory-memory and memory-I/O transfers with virtual DMA functionality

  - **Protocols** supported by ROM or downloadable microcode and include, but limited to, the digital portion of :
    - Ethernet / IEEE 802.3 CS/CDMA
    - HDLC2 / SDLC and HDLC bus
    - Apple talk
    - Signaling system #7 (RAM microcode only)
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BiSync) communications
    - Totally transparent
    - Totally transparent with CRC
    - Profibus (RAM microcode option)
    - Asynchronous HDLC
    - DDCMP
    - V.14 (RAM microcode option)
    - X.21 (RAM microcode option)
    - V.32bis datapump filters
    - IrDA serial infrared
    - Basis rate ISDN (BRI) in conjunction with SMC channels
    - Primary rate ISDN (MH version only)
  - Four hardware serial communications controller channels supporting the protocols
  - Two hardware serial management channels
    - Management for BRI devices as general circuit interface controller multiplexed channels
    - low-speed UART operation
  - Hardware serial peripheral interfaces
  - I^2C (microwire compatible) interface
  - Time-slot assigner
  - Port supports Centronics interfaces anc chip-to-chip
  - Four independent baud rate generators and four input clock pins for supplying clocks to SMC and SCC serial channels
  - Four independant 16-bit timers which can be interconnected as two 32-bit timers

6. ORDERING INFORMATION



(1) THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES

(2) For availability of the different versions, contact your TCS sale office

This product is manufactured by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - 38521 SAINT-EGREVE - FRANCE.

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