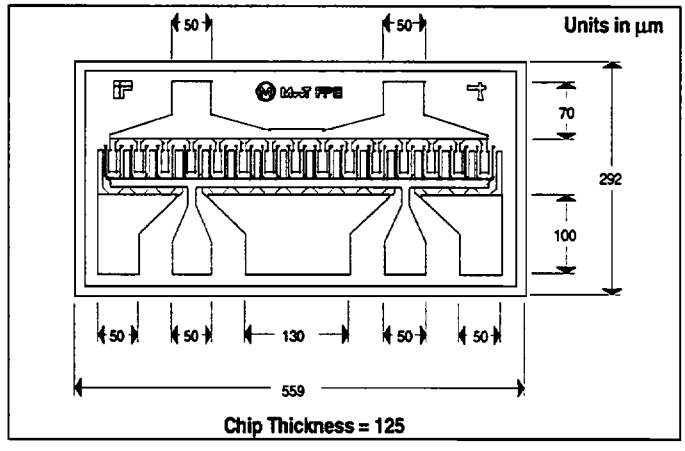
MICROWAVE TECHNOLOGY

MwT-6
18 GHz High Power GaAs FET



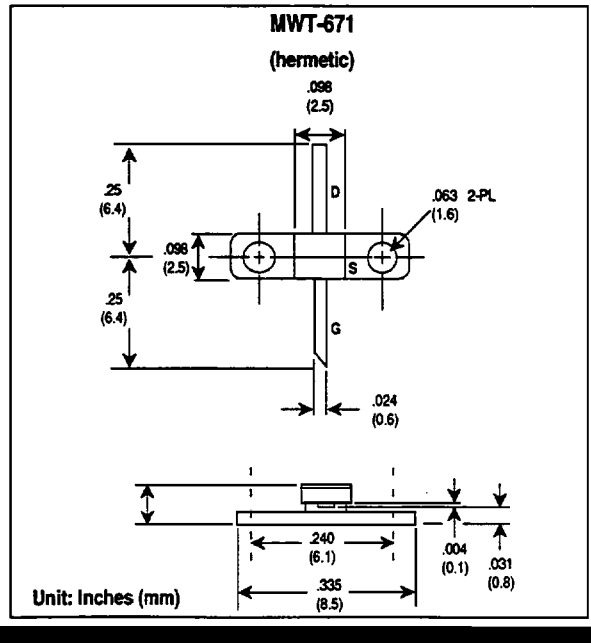
- 0.5 WATT POWER OUTPUT AT 12 GHz
- +39 dBm THIRD ORDER INTERCEPT
- HIGH ASSOCIATED GAIN
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 900 MICRON GATE WIDTH
- CHOICE OF CHIP AND ONE PACKAGE TYPE

DESCRIPTION

The MwT-6 GaAs MESFET is ideally suited to narrow-band applications such as cellular telephone, PCN, point-to-point communications links, and other wireless applications as the driver transistor for the output power amplifier. The third-order intercept performance of the MwT-6 is excellent, typically 12 dB above the 1 dB compression point. The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

RF SPECIFICATIONS AT Ta = 25°C

				MwT-6 HP MwT-671 HP	
SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1dB Compression VDS=6.0 V IDS= 150 mA	12 GHz	dBm	26.0	27.0
SSG	Small Signal Gain VDS=6.0 V IDS= 150 mA	12 GHz	dB	7.5	8.0
PAE	Power Added Efficiency VDS=6.0 V IDS= 150 mA	12GHz	%	25	35
IDSS	Recommended IDSS Range for Optimum P1dB		mA		240-330



DC SPECIFICATIONS AT Ta = 25 °C

SYMBOL	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Idss	Saturated Drain Current Vds=4.0 V VGS=0.0 V	mA	90		360
Gm	Transconductance Vds=2.0 V VGS=0.0 V	mS	108	145	
Vp	Pinch-off Voltage Vds=3.0 V IDS=6.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Voltage Igs=-0.6 mA, Igd=0	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd=-0.6 mA, Igs=0	V	-8.0	-12.0	
Rth	Thermal Resistance* MwT-6 Chip MwT-671	°C/W		60 60*	

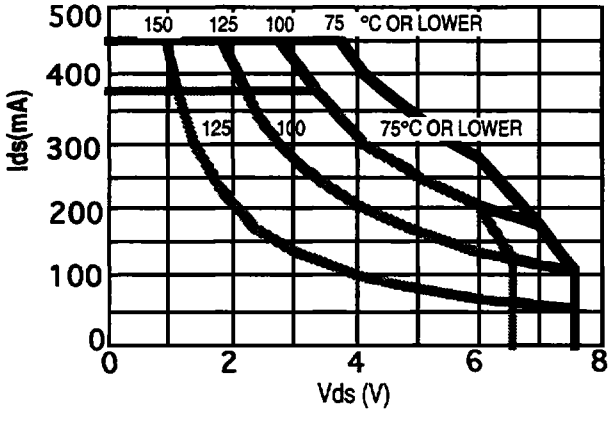
*** Overall Rth depends on case mounting**

MAXIMUM RATINGS AT Ta = 25 ° C

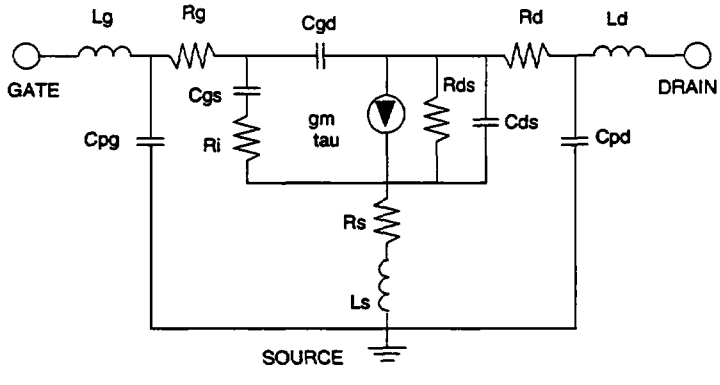
SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	360	540

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

SAFE OPERATING LIMITS vs. Case Temperature — Absolute Maximum — Continuous Maximum



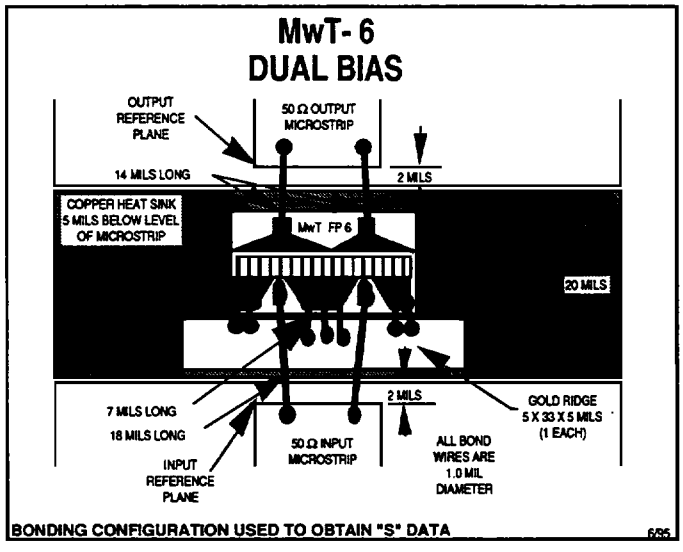
DEVICE EQUIVALENT CIRCUIT MODEL

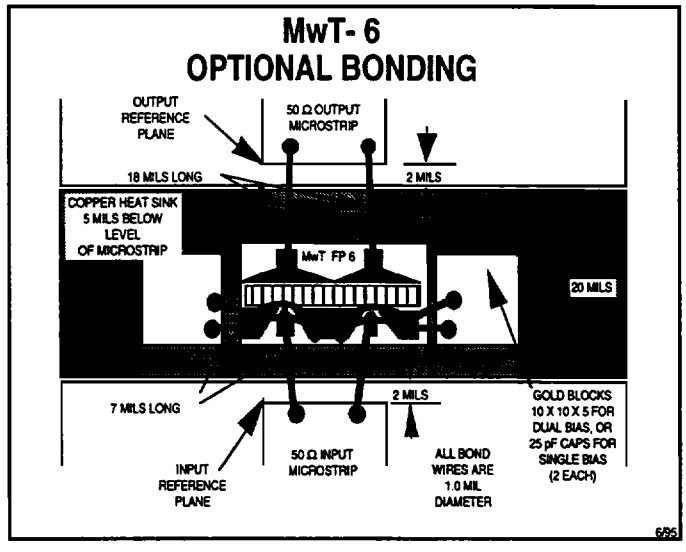


PARAMETER		VALUE		PARAMETER		VALUE	
Gate Bond Wire Inductance	Lg	0.14	nH	Source Resistance	Rs	0.72	Ω
Gate Pad Capacitance	Cpg	0.05	pF	Source Inductance	Ls	0.04	nH
Gate Resistance	Rg	0.15	Ω	Drain-Source Resistance	Rds	125.0	Ω
Gate-Source Capacitance	Cgs	1.0	pF	Drain-Source Capacitance	Cds	0.14	pF
Channel Resistance	Ri	2.0	Ω	Drain Resistance	Rd	1.44	Ω
Gate-Drain Capacitance	Cgd	0.07	pF	Drain Pad Capacitance	Cpd	0.017	pF
Transconductance	gm	112.0	mS	Drain Inductance	Ld	2.0	nH
Transit time	tau	2.0	psec				

RECOMMENDED ASSEMBLY CONFIGURATION

Shown below is the assembly and bonding configuration used for S-Parameter measurements of the MwT-6 chip. This configuration is recommended for optimum performance. For single-bias applications the gold blocks may be replaced by capacitors. An additional interconnecting bond would then be required. Contact MwT for additional applications information.





BIN SELECTION

Every MwT-6 wafer has been probed for Idss and the data stored on computer disk. Customers may select from Idss values in any of 18 current bins, as shown below, to insure consistent performance in their circuit. The shaded bins are typically available in smaller quantity and caution is advised before designing these bins into high production applications. MwT's "Smart Wafer Picker" reads the stored Idss Data from the disk and devices from customer selected bins are quickly and automatically picked from the wafer and loaded into shipping containers.

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS	90-	105-	120-	135-	150-	165-	180-	195-	210-	225-	240-	255-	270-	285-	300-	315-	330-	345-
(mA)	105	120	135	150	165	180	195	210	225	240	255	270	285	300	315	330	345	360

BIN ACCURACY

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may deviate as much as +/- 1 bin within the range identified on the label of each die shipping container, and +/- 2 bins within the selected range.

TYPICAL COMMON SOURCE SCATTERING PARAMETERS

MwT-6 CHIP: VDS = 6.0 V, IDS = 0.6 IDSS = 150 mA

FREQUENCY (GHz)	S11		S21		S12		S22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.00	.95	-46.7	6.82	149.6	.036	64.1	.43	-24.2
2.00	.90	-82.1	5.56	127.0	.058	48.0	.37	-42.7
3.00	.86	-107.7	4.48	109.7	.069	37.5	.33	-55.9
4.00	.85	-125.3	3.68	97.1	.074	30.2	.30	-66.4
5.00	.83	-139.7	3.12	85.8	.075	27.4	.28	-75.1
6.00	.83	-150.0	2.67	76.3	.078	25.0	.28	-84.8
7.00	.83	-158.4	2.32	67.9	.077	23.2	.28	-93.6
8.00	.82	-165.2	2.05	60.6	.077	22.2	.29	-102.6
9.00	.83	-170.9	1.84	54.0	.075	21.0	.30	-111.6
10.00	.84	-176.2	1.68	47.9	.069	21.8	.32	-119.6
12.00	.87	173.9	1.43	34.8	.065	31.9	.37	-134.1
14.00	.86	165.7	1.20	22.0	.078	38.0	.43	-144.3
16.00	.87	160.5	1.02	12.5	.083	38.1	.50	-153.0
18.00	.89	154.6	.91	3.7	.091	42.1	.57	-159.6
20.00	.91	147.7	.80	-5.6	.098	46.7	.61	-165.7

MwT-671HP: VDS = 6.0 V, IDS = 150 mA

FREQUENCY (GHz)	S11		S21		S12		S22		MSG
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	dB
1.00	.91	-63.8	7.26	129.7	.03	46.2	.45	-32.8	23.5
2.00	.82	-108.2	5.35	94.2	.05	23.3	.40	-54.6	20.7
3.00	.78	-138.3	3.95	66.8	.05	10.7	.39	-72.6	18.5
4.00	.78	-161.0	3.10	43.7	.06	1.7	.40	-90.2	17.2
5.00	.76	179.2	2.50	25.5	.07	-4.4	.41	-109.5	15.5
6.00	.78	164.0	2.13	8.6	.08	-12.0	.44	-125.8	14.2
7.00	.79	149.3	1.97	-6.0	.10	-28.4	.44	-143.4	13.0
8.00	.81	135.8	1.81	-19.3	.10	-40.5	.47	-161.9	12.4
9.00	.84	123.2	1.87	-36.1	.11	-51.1	.50	-178.2	12.1
10.00	.86	109.2	1.78	-51.1	.13	-63.2	.52	160.1	11.2
11.00	.85	94.4	1.80	-69.8	.15	-73.9	.54	140.0	10.8
12.00	.85	87.4	1.80	-84.3	.17	-84.4	.55	123.8	10.4

DEVICE HANDLING PROCEDURE

1) Open package in clean room environment only.
2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
4) Assembly should be performed with parts no hotter than 300° C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
5) Die attach with clean AuSn alloy under forming gas at 280 to 300° C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150° C should be used with a heater stage temperature of 200 to 225° C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5%.
7) Store in a clean, dry, inert environment such as nitrogen at room temperature.
8) CAUTION: Handling of chips other than as specified above may cause permanent damage.