

**FEATURES**

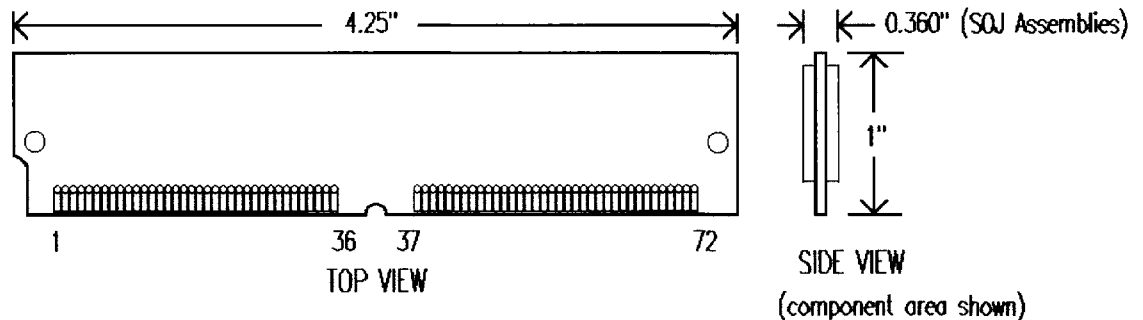
- 72-pin industry standard four-byte single-in-line memory module
- JEDEC compliant: 21-C, Fig. 4-10A, C (Release 5)  
No. 95 MO-116
- Supports 90°, 40° and 22.5° connectors
- High performance, CMOS
- Single 5.0V ± 10% power supply
- TTL-compatible inputs and outputs
- Fast Page Mode access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, HIDDEN
- Refresh: 2048 refresh cycles every 32 ms
- Dimensions: 4.25" (length) x 1.00" (height) x 0.360" (max thickness)

**PERFORMANCE RANGE**

SYMBOL	PARAMETER	Rating	
		60 ns	70 ns
t <sub>RAC</sub>	RAS Access Time	60 ns (max)	70 ns (max)
t <sub>CAC</sub>	CAS Access Time	15 ns (max)	20 ns (max)
t <sub>AA</sub>	Access Time from Column Address	30 ns (max)	35 ns (max)
t <sub>RC</sub>	Random Read or Write Cycle Time	110 ns (min)	130 ns (min)
t <sub>PC</sub>	Fast Page Mode Cycle Time	40 ns (min)	45 ns (min)

**ORDERING INFORMATION**

DESCRIPTION	PART NUMBER	ENGINEERING DESCRIPTOR
8M x 40, 60 ns, Tin/Lead Tabs, SOJ	21394C	CL001D08400B0BJ-60
8M x 40, 70 ns, Tin/Lead Tabs, SOJ	21395C	CL001D08400B0BJ-70
8M x 40, 60 ns, Gold Tabs, SOJ	21396C	CL001E08400B0BJ-60
8M x 40, 70 ns, Gold Tabs, SOJ	21397C	CL001E08400B0BJ-70

**CARD OUTLINE**

**GENERAL DESCRIPTION**

The 8M x 40 SIMM uses dynamic RAM devices and is designed for use as a general-purpose four-byte wide memory assembly with eight data bits per byte and an extra 8 bits being used for Error Checking & Correction (ECC). The SIMM is populated with twenty 4M x 4 DRAMs.

Presence Detect (PD) bits provide information about SIMM density, addressing, performance and features.

During Read or Write Cycles, each byte may be uniquely addressed via 22 address bits, with the first 11 bits (A0~A10) latched on  $\overline{RAS}$  and the latter 11 bits (A0~A10) latched on  $\overline{CAS}$ . READ or WRITE cycles are selected with the  $\overline{WE}$  input, with a logic low indicating a WRITE cycle and a logic HIGH indicating a READ cycle. During a WRITE cycle, data-in is latched by the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last.

FAST PAGE MODE operation allows for faster READs or WRITEs within a row-address-defined page boundary. A FAST PAGE MODE cycle is initiated with  $\overline{RAS}$  followed by  $\overline{CAS}$ , then strobing  $\overline{CAS}$  to latch different column addresses while holding  $\overline{RAS}$  LOW.

Returning  $\overline{RAS}$  and  $\overline{CAS}$  high terminates a memory cycle and returns the DRAMs to a reduced-current STANDBY state.

Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{RAS}$  cycle (READ, WRITE) or  $\overline{RAS}$  refresh cycle ( $\overline{RAS}$ -ONLY, CBR, or HIDDEN) so that all 2048 combinations of  $\overline{RAS}$  addresses (A0~A10) are executed at least every 32 ms. The CBR refresh and HIDDEN refresh cycles will invoke the on-chip refresh address counters for automatic  $\overline{RAS}$  addressing.

**PIN DESCRIPTION**

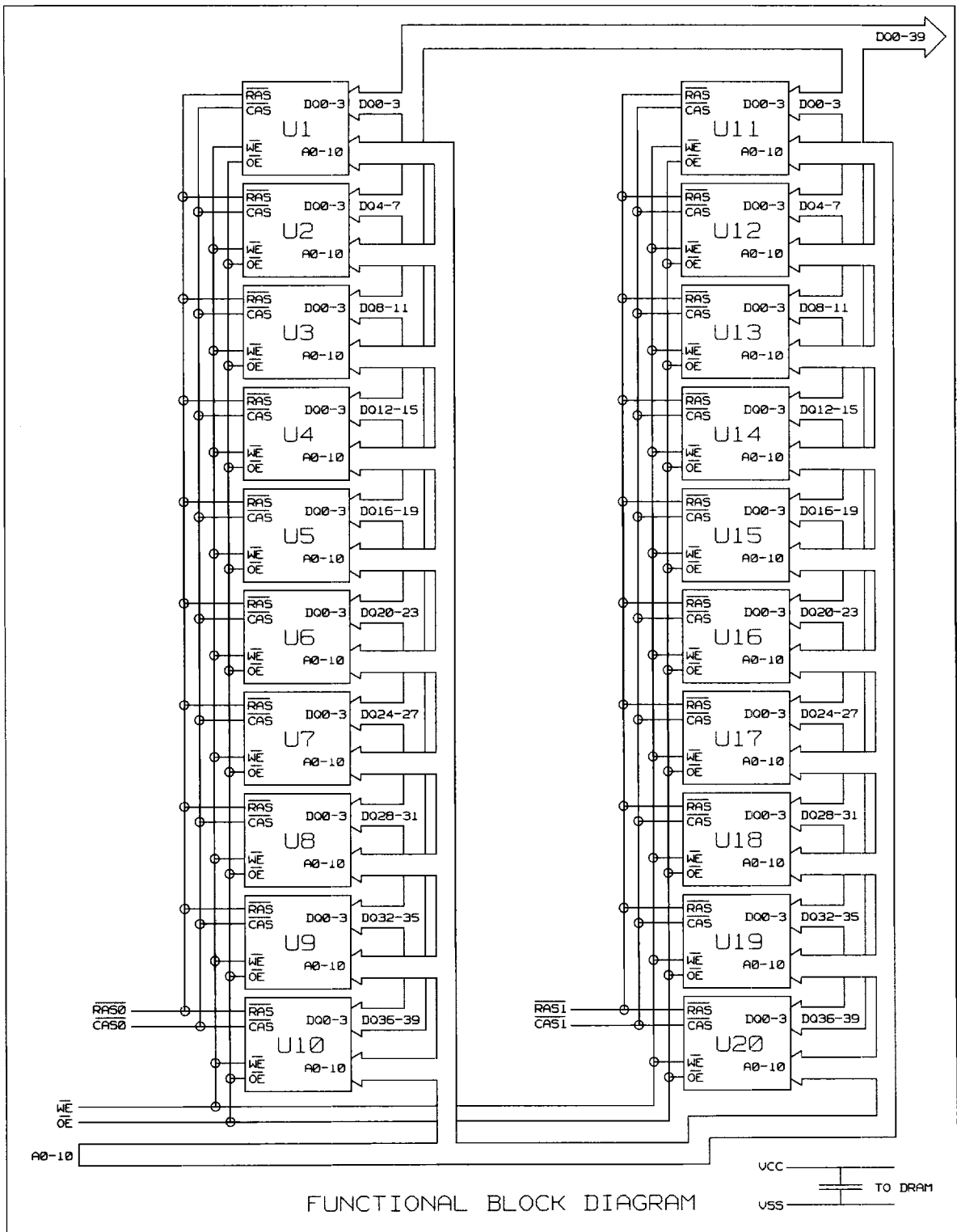
RAS0,RAS1	Row Address Strobe
CAS0,CAS1	Column Address Strobe
WE	Write Enable
A0~A10	Address Inputs
DQ0~39	Data In/Out
VCC	Power (+5.0V )
VSS	Ground
NC	No Connection
PD1~5	Presence Detects

**PRESENCE DETECT**

PIN SYMBOL	CONFIGURATION	
	60 ns	70 ns
PD1	NC	NC
PD2	VSS	VSS
PD3	NC	VSS
PD4	NC	NC
PD5	VSS	VSS

**PIN CONFIGURATION**

#	Name	#	Name	#	Name	#	Name	#	Name	#	Name
1	VSS	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	VSS	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	CAS0	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	DQ37
6	DQ4	18	A6	30	VCC	42	NC	54	DQ27	66	DQ38
7	DQ5	19	OE	31	A8	43	CAS1	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	RAS0	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	RAS1	57	DQ30	69	PD3
10	VCC	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	WE	59	VCC	71	DQ39
12	A0	24	DQ12	36	DQ18	48	PD(ECC)	60	DQ32	72	VSS



**TRUTH TABLE**

FUNCTION		RAS	CAS	WE	ROW ADDR	COL ADDR	DATA IN/OUT
Standby		H	H-X	X	X	X	Hi-Z
Read		L	L	H	ROW	COL	Valid D <sub>OUT</sub>
Early-Write		L	L	L	ROW	COL	Valid D <sub>IN</sub>
Fast Page Mode-Read	1st Cycle	L	H-L	H	ROW	COL	Valid D <sub>OUT</sub>
	2nd Cycle	L	H-L	H	N/A	COL	Valid D <sub>OUT</sub>
Fast Page Mode-Write	1st Cycle	L	H-L	L	ROW	COL	Valid D <sub>IN</sub>
	2nd Cycle	L	H-L	L	N/A	COL	Valid D <sub>IN</sub>
RAS-Only Refresh		L	H	X	ROW	N/A	Hi-Z
Hidden Refresh	Read	L-H-L	L	H	ROW	COL	Valid D <sub>OUT</sub>
	Write	L-H-L	L	L	ROW	COL	Valid D <sub>IN</sub>
CAS-Before-RAS Refresh		H-L	L	H	X	X	Hi-Z

X:"H" or "L" D<sub>IN</sub>:Data In D<sub>OUT</sub>:Data Out Hi-Z:High Impedance N/A:Not Applicable

**ABSOLUTE MAXIMUM RATINGS (Note 1,22)**

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V <sub>CC</sub>	Power Supply Voltage	-1.0 to 7.0	V	2
V <sub>IN</sub>	Voltage on any Pin Relative to V <sub>SS</sub>	-1.0 to 7.0	V	2
V <sub>OUT</sub>		-1.0 to 7.0	V	2
T <sub>opr</sub>	Operating Temperature	0 to 70	°C	
T <sub>stg</sub>	Storage Temperature	-55 to 125	°C	
P <sub>D</sub>	Power Dissipation	20.0	W	17,31
I <sub>OS</sub>	Short Circuit Output Current	50	mA	17

**RECOMMENDED OPERATING CONDITIONS** ( $T_A = 0$  to  $70^\circ\text{C}$ ) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V	
$V_{SS}$	Ground	0	0	0	V	
$V_{IH}$	Input High Voltage	2.4		$V_{CC} + 1.0$	V	22
$V_{IL}$	Input Low Voltage	-1		0.8	V	22

 $T_A$ : Ambient temperature

**CAPACITANCE** ( $f = 1$  MHz;  $T_A = 25^\circ\text{C}$ ) (Note 22)

SYMBOL	PARAMETER	MAX.	UNITS	NOTES
$C_{I1}$	Input Capacitance (A0-A10)	100	pF	
$C_{I2}$	Input Capacitance (RAS0~RAS1)	70	pF	
$C_{I3}$	Input Capacitance (CAS0~CAS1)	70	pF	
$C_{I4}$	Input Capacitance ( $\overline{WE}$ )	140	pF	
$C_{I5}$	Input Capacitance ( $\overline{OE}$ )	140	pF	
$C_{O1}$	Output Capacitance (Data In/Out)	14	pF	

 $T_A$ : Ambient temperature

**DC CHARACTERISTICS**

(Recommended operating conditions unless otherwise noted.) (Note 18,22)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	NOTES	
I <sub>CC1</sub>	OPERATING CURRENT: Average Power Supply Operating Current (RAS,CAS, Address Cycling @ t <sub>RC</sub> = t <sub>RC(min)</sub> , V <sub>CC</sub> = V <sub>CC(max)</sub> ) (mA)	60 ns	-	1120	3,4,5,6, 16	
		70 ns	-	1020		
I <sub>CC2</sub>	STANDBY CURRENT (TTL): Power Supply Standby Current (RAS=CAS=V <sub>CC</sub> , Data out is disabled (Hi-Z), all other inputs =V <sub>CC</sub> , V <sub>CC</sub> =V <sub>CC(max)</sub> ) (mA)	Don't Care	-	40		
I <sub>CC3</sub>	RAS-ONLY REFRESH CURRENT: Average Power Supply Current, RAS-Only Mode (RAS, Address Cycling, CAS=V <sub>IH</sub> @ t <sub>RC</sub> =t <sub>RC(min)</sub> , V <sub>CC</sub> =V <sub>CC(max)</sub> ) (mA)	60 ns	-	2200	3,4,5,6,16, 31	
		70 ns	-	2000		
I <sub>CC4</sub>	FAST PAGE MODE CURRENT: Average Power Supply Current, FPM (RAS=V <sub>IL</sub> , CAS, Address Cycling @ t <sub>PC</sub> =t <sub>PC(min)</sub> , V <sub>CC</sub> =V <sub>CC(max)</sub> ) (mA)	60 ns	-	820	3,4,5,7,16	
		70 ns	-	720		
I <sub>CC5</sub>	STANDBY CURRENT (CMOS): Power Supply Standby Current (RAS=CAS=V <sub>CC</sub> -0.2V, Data Out is disabled (Hi-Z), V <sub>CC</sub> = V <sub>CC(max)</sub> ) (mA)	Don't Care	-	20		
I <sub>CC6</sub>	CAS-BEFORE-RAS, REFRESH CURRENT: Average Power Supply Current, CAS-Before-RAS Mode (RAS,CAS Cycling @ t <sub>RC</sub> =t <sub>RC(min)</sub> , V <sub>CC</sub> = V <sub>CC(max)</sub> ) (mA)	60 ns	-	2200	3,4,5,6,16, 31	
		70 ns	-	2000		
I <sub>LI</sub>	INPUT LEAKAGE CURRENT: Input Leakage Current, any input (0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , all other pins not under test=0V, V <sub>CC</sub> = V <sub>CC(max)</sub> ) (μA)	<b>A0~A10</b>		-200	200	
		<b>RAS0~RAS1</b>		-100	100	
		<b>CAS0~CAS1</b>		-100	100	
		<b>WE</b>		-200	200	
		<b>OE</b>		-200	200	
I <sub>LO</sub>	OUTPUT LEAKAGE CURRENT: (Data Out is disabled (Hi-Z), 0 ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> ) (μA)		-20	20		
V <sub>OH</sub>	OUTPUT HIGH LEVEL: Output "H" Level Voltage (I <sub>OUT</sub> =-5mA) (V)		2.4	-	2	
V <sub>OL</sub>	OUTPUT LOW LEVEL: Output "L" Level Voltage (I <sub>OUT</sub> =+4.2mA) (V)		-	0.4	2	

**AC CHARACTERISTICS**
**READ, WRITE, AND REFRESH CYCLES (COMMON PARAMETERS)**

(Recommended operating conditions unless otherwise noted.) (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
$t_{RC}$	Random READ or WRITE Cycle Time (ns)	110	-	130	-	
$t_{RP}$	RAS Precharge Time (ns)	40	-	50	-	
$t_{CP}$	CAS Precharge Time (ns)	10	-	10	-	
$t_{RAS}$	RAS Pulse Width (ns)	60	10000	70	10000	23
$t_{CAS}$	CAS Pulse Width (ns)	15	10000	20	10000	23
$t_{ASR}$	Row Address Setup Time (ns)	0	-	0	-	22
$t_{RAH}$	Row Address Hold Time (ns)	10	-	10	-	
$t_{ASC}$	Column Address Setup Time (ns)	0	-	0	-	22
$t_{CAH}$	Column Address Hold Time (ns)	10	-	15	-	22
$t_{RCD}$	RAS to CAS Delay Time (ns)	20	45	20	50	10
$t_{RAD}$	RAS to Col. Address Delay Time (ns)	15	30	15	35	15,23
$t_{RSH}$	RAS Hold Time (ns)	15	-	20	-	22
$t_{CSH}$	CAS Hold Time (ns)	60	-	70	-	
$t_{CRP}$	CAS to RAS Precharge Time (ns)	5	-	5	-	22
$t_{RPC}$	RAS Precharge to CAS hold Time (ns)	5	-	5	-	22
$t_T$	Transition Time (Rise and Fall) (ns)	3	30	3	30	22
$t_{AR}$	Column Address Hold Time Referenced to RAS (ns)	-	-	-	-	

**READ CYCLES (Note 8,18)**

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
$t_{RAC}$	Access Time from $\overline{RAS}$ (ns)	-	60	-	70	9,10,15,30
$t_{CAC}$	Access Time from $\overline{CAS}$ (ns)	-	15	-	20	9,10,30
$t_{AA}$	Access Time from Address (ns)	-	30	-	35	9,15,30
$t_{RCS}$	Read Command Setup Time (ns)	0	-	0	-	22
$t_{RCH}$	Read Command Hold Time to $\overline{CAS}$ (ns)	0	-	0	-	14,22
$t_{RRH}$	Read Command Hold Time to $\overline{RAS}$ (ns)	0	-	0	-	14,22
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time(ns)	30	-	35	-	22
$t_{CLZ}$	$\overline{CAS}$ to Output in Low-Z (ns)	0	-	0	-	9,22
$t_{DZC}$	Data to $\overline{CAS}$ Low Delay Time (ns)	-	-	-	-	
$t_{CDD}$	$\overline{CAS}$ High to Data Delay Time (ns)	15	-	18	-	27
$t_{OFF}$	Output Buffer Turn-Off Delay (ns)	0	15	0	20	12,24

**WRITE CYCLES (Note 8,18)**

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
$t_{WCS}$	Write Command Set Up Time (ns)	0	-	0	-	13
$t_{WCH}$	Write Command Hold Time (ns)	10	-	15	-	
$t_{WCP}$	Write Command Pulse Width (ns)	10	-	15	-	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time (ns)	15	-	20	-	22
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time (ns)	15	-	20	-	
$t_{DS}$	$D_{IN}$ Setup Time (ns)	0	-	0	-	25
$t_{DH}$	$D_{IN}$ Hold Time (ns)	10	-	15	-	22
$t_{WCR}$	Write Command Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	
$t_{DHR}$	Data in Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	

**FAST PAGE MODE CYCLES (Note 8,18)**

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t <sub>PC</sub>	Fast Page Mode Cycle Time (ns)	40	-	45	-	
t <sub>RASP</sub>	Fast Page Mode RAS Pulse Width (ns)	60	100000	70	100000	22
t <sub>CPRH</sub>	RAS Hold Time from CAS Precharge (ns)	35	-	40	-	22
t <sub>CFA</sub>	Access Time from CAS Precharge (ns)	-	35	-	40	9,21,22,30
t <sub>CPW</sub>	WE Delay Time From CAS Precharge (ns)	60	-	70	-	13

**REFRESH CYCLE (Note 8,18)**

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t <sub>CHR</sub>	CAS Hold Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	15	-	22
t <sub>CSR</sub>	CAS Setup Time (CAS-before-RAS Refresh Cycle) (ns)	5	-	5	-	22
t <sub>WRP</sub>	WE Setup Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	10	-	22
t <sub>WRH</sub>	WE Hold Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	10	-	22
t <sub>REF</sub>	Refresh Period (2048 cycles) (ms)	-	32	-	32	

**NOTES**

1. Permanent damage to the device may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages referenced to  $V_{SS}$ .
3.  $I_{CC}$  is specified as an average current.
4. This parameter depends on output loading and/or cycle rates.
5. Specified values are obtained with the output open.
6. Address can be changed a maximum of once while  $\overline{RAS}=V_{IL}$ .
7. Address can be changed a maximum of once while  $\overline{CAS}=V_{IH}$ .
8.  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals. Transition time ( $t_T$ ) is measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ , and is assumed to be 5ns for all inputs. All input signals must transit between  $V_{IH}$  and  $V_{IL}$  (or  $V_{IL}$  and  $V_{IH}$ ) without slope reversal.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. Operation within the  $t_{RCD(max)}$  limit ensures that  $t_{RAC(max)}$  can be met.  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
11. Assumes that  $t_{RAD} \leq t_{RAD(max)}$ .
12. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
13. This is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If  $t_{WCS} \geq t_{WCS(min)}$  the cycle is an early write cycle and the data out pins will remain high impedance (open circuit) for the duration of the cycle. If the above condition is not satisfied, the condition of the data out (at access time) is indeterminate.
14. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
15. Operation within the  $t_{RAD(max)}$  limit ensures that  $t_{RAC(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, then access time is controlled exclusively by  $t_{AA}$ .
16. Specified values are obtained with minimum cycle time.
17. Specified values are obtained with  $T_A = 25^\circ C$ .

18. An initial pause of 200 $\mu$ s is required after power-up followed by a minimum of eight initialization cycles (any 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$ -only Refresh cycles with  $\overline{\text{WE}}$  high) before proper device operation is assured. Also, any 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}$ -only Refresh cycles with  $\overline{\text{WE}}$  high are required after prolonged periods (greater than  $t_{\text{REF}}$ ) of  $\overline{\text{RAS}}$  inactivity before proper device operation is assured.
19. Measured with a load equivalent to 50pF and 500 ohms.
20. Write cycle is applicable instead of read cycle. Timing requirements for  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and Address are the same for Hidden Refresh Write Cycle as that shown for Hidden Refresh Read Cycle.  $\overline{\text{WE}}$ ,  $D_{\text{IN}}$  and  $D_{\text{OUT}}$  for Hidden Refresh Write Cycle are the same as for Write Cycle.
21.  $t_{\text{CPA}}$  is access time from  $\overline{\text{CAS}}$  precharge (that is caused by changing  $\overline{\text{CAS}}$  from "L" to "H"). Therefore, if  $t_{\text{CP}}$  is long, then  $t_{\text{CPA}}$  is longer than  $t_{\text{CPA}(\text{max})}$ .
22. Calculated based on data supplied by the DRAM manufacturer(s).
23. Maximum value is calculated based on data supplied by the DRAM manufacturer(s).
24. Minimum value is calculated based on data supplied by the DRAM manufacturer(s).
25. This parameter is referenced to the  $\overline{\text{CAS}}$  leading edge in Early Write cycles.
26.  $V_{\text{IN}} = 0$  Volt.
27. Either  $t_{\text{CDD}}$  or  $t_{\text{ODD}}$  must be satisfied.
28. Either  $t_{\text{DZC}}$  or  $t_{\text{DZO}}$  must be satisfied.
29.  $t_{\text{RASP}(\text{MIN})}$  is specified as two cycles of  $\overline{\text{CAS}}$  input are performed.
30. The access time is limited by all four parameters  $t_{\text{RAC}}$ ,  $t_{\text{CAC}}$ ,  $t_{\text{AA}}$ ,  $t_{\text{CPA}}$ .
31. This assumes all  $\overline{\text{RAS}}$  (and all  $\overline{\text{CAS}}$  for CBR refresh) are active.

For Timing Diagrams see “**FPM Timing Diagrams**” (Document No. **20432C**).

Available from fax-on-demand and Website: <http://www.celestica.com/memory/>

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