- **Low Skew Propagation Delay Specifications for Clock Driving Applications**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

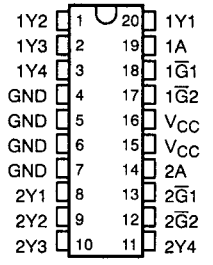
description

These devices contain dual-clock driver circuits that fan out one input signal to four outputs with minimum skew for clock distribution. They also offer two output-enable pins for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the A input.

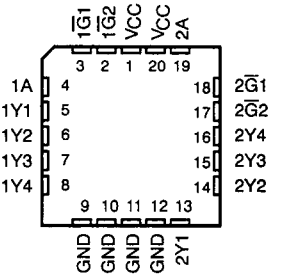
Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The 54AC11208 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11208 is characterized for operation from – 40°C to 85°C.

54AC11208 . . . J PACKAGE
74AC11208 . . . DW OR N PACKAGE
(TOP VIEW)



54AC11208 . . . FK PACKAGE
(TOP VIEW)



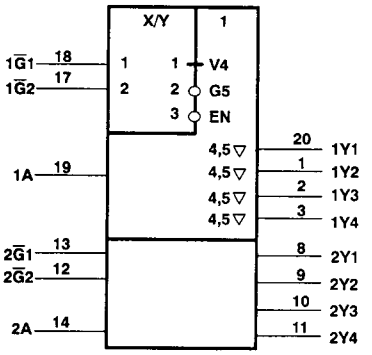
FUNCTION TABLES

OUTPUT CONTROL		DATA INPUT	OUTPUTS			
$1\overline{G}1$	$1\overline{G}2$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

OUTPUT CONTROL		DATA INPUT	OUTPUTS			
$2\overline{G}1$	$2\overline{G}2$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

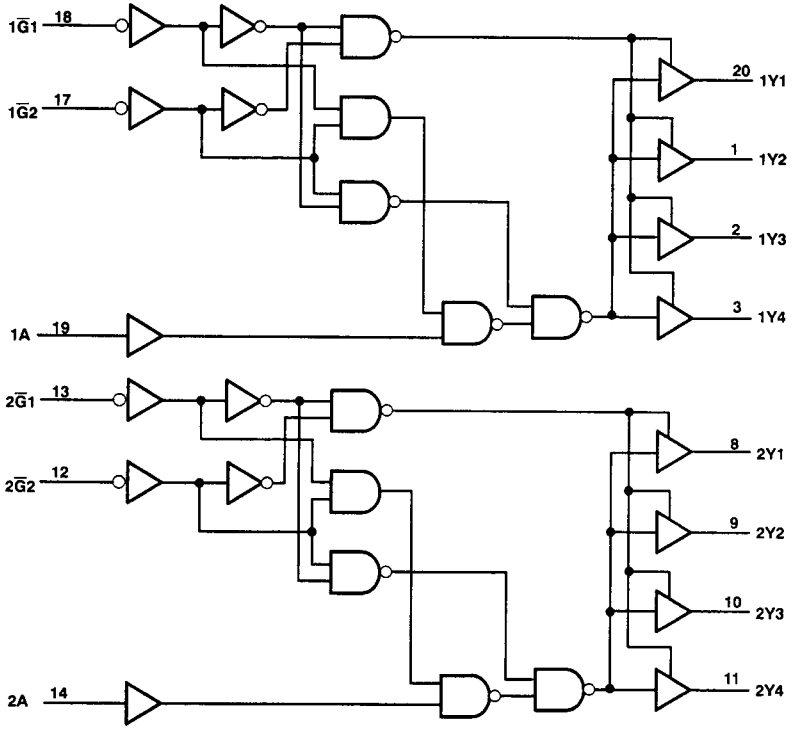
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) ..... ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ± 50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ± 50 mA
Continuous current through V_{CC} or GND pins ..... ± 200 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11208			74AC11208			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11208		74AC11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = – 50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = – 50 mA†	5.5 V				3.85				
	I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	$V_I = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	μA
I_I	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	$V_I = V_{CC}$ or GND	5 V		4						pF
C_o	$V_I = V_{CC}$ or GND	5 V		10						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11208		74AC11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.8	11.1	13.1	4.8	15.6	4.8	14.6	ns
t_{PHL}			5.1	12.2	14.3	5.1	16.7	5.1	15.6	
t_{PLH}	1$\overline{G}$n and 2$\overline{G}$n	Any Y	5.2	11.9	14.2	5.2	16.9	5.2	15.8	ns
t_{PHL}			7.8	13.3	15.7	7.8	18.4	7.8	17.4	
t_{PZH}	1$\overline{G}$2 or 2$\overline{G}$2	Any Y	5.1	11.8	14.2	5.1	17.2	5.1	15.7	ns
t_{PZL}	1$\overline{G}$1 or 2$\overline{G}$1		6.8	16.3	19.5	6.8	23.8	6.8	22.8	
t_{PHZ}	1$\overline{G}$2 or 2$\overline{G}$2	Any Y	3.4	6.9	8.6	3.4	9.6	3.4	9.2	ns
t_{PLZ}	1$\overline{G}$1 or 2$\overline{G}$1		4.1	7.5	9.4	4.1	10.5	4.1	10.2	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC11208		74AC11208		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	1A and 2A	Any Y	4.2	5.5	9	4.2	10.5	4.2	9.9	ns
t_{PHL}			4.2	7	9.3	4.2	10.8	4.2	10.1	
t_{PLH}	$1\overline{G}n$ and $2\overline{G}n$	Any Y	4.6	7.3	9.6	4.6	11.5	4.6	10.7	ns
t_{PHL}			4.8	7.7	10.2	4.8	11.8	4.8	11	
t_{PZH}	$1\overline{G}2$ or $2\overline{G}2$	Any Y	4.3	7.2	9.4	4.3	11.3	4.3	10.4	ns
t_{PZL}	$1\overline{G}1$ or $2\overline{G}1$		5.3	9	12.2	5.3	14.3	5.3	13.5	
t_{PHZ}	$1\overline{G}2$ or $2\overline{G}2$	Any Y	3	5.4	7.5	3	8.5	3	8	ns
t_{PLZ}	$1\overline{G}1$ or $2\overline{G}1$		3.7	5.7	7.5	3.7	8.5	3.7	8.2	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Notes 2 and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	74ACT11208			UNIT
			MIN	TYP	MAX	
t_{PLH}	1A and 2A	Any Y	6		8.5	ns
t_{PHL}			6		8.5	
$t_{sk(o)}$	1A and 2A	Any Y			1	ns

NOTES: 2. Load circuit and voltage waveforms are shown in Section 1.
3. Specifications are valid for all outputs switching simultaneously and in-phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF, f = 1 MHz	95	pF
		Outputs disabled		10	