June 1992
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FUJITSU

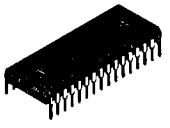
DATA SHEET

MB841000-70, -85, -10 (L, LL, and SL Versions)
CMOS 1M Low Power SRAM with Data Retention

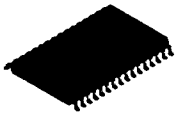
The Fujitsu MB841000 is a 131,072 word x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB841000 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

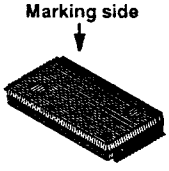
Parameter	L-version			LL-version			SL-version		
	-70L	-85L	-10L	-70LL	-85LL	-10LL	-70SL	-85SL	-10SL
Access Time (ns)	70	85	100	70	85	100	70	85	100
Standby Power	0.55 mW			0.275 mW			0.275 mW		
Data Retention Current	50 µA			40 µA			20 µA		
Data Retention Current (TA = °C to +40°C)	—			6 µA			3 µA		

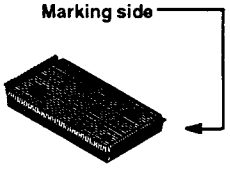


Plastic DIP
(DIP-32P-M01)



Plastic SOP
(FPT-32P-M03)





Plastic TSOP-I

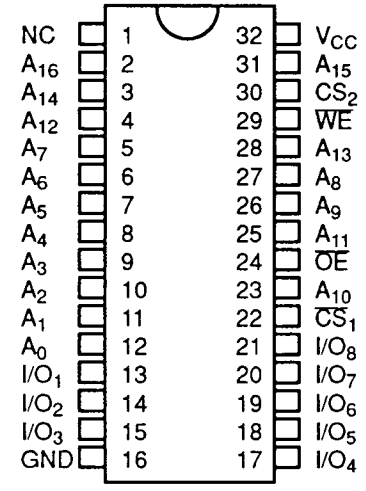
Normal Bend Leads
(FPT-32P-M06)

Reverse Bend Leads
(FPT-32P-M07)

- Organization: 131,072 words x 8 bits
- Data retention voltage: 2.0 V min.
- TTL compatible inputs and outputs
- Single +5 V power supply, +10% tolerance
- Static operation: no clock required
- Package and ordering information:
  - 32-pin plastic DIP (600 mil) order as MB841000-xxL(LL/SL)P
  - 32-pin plastic SOP (525 mil) order as MB841000-xxL(LL/SL)PF
  - 32-pin plastic TSOP-I (normal bend) order as MB841000-xxL(LL/SL)PFTN
  - 32-pin plastic TSOP-I (reverse bend) order as MB841000-xxL(LL/SL)PFTR

Pin Assignment

TOP VIEW



DIP and SOP

See pages 12 and 13 for TSOP pin assignmants.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

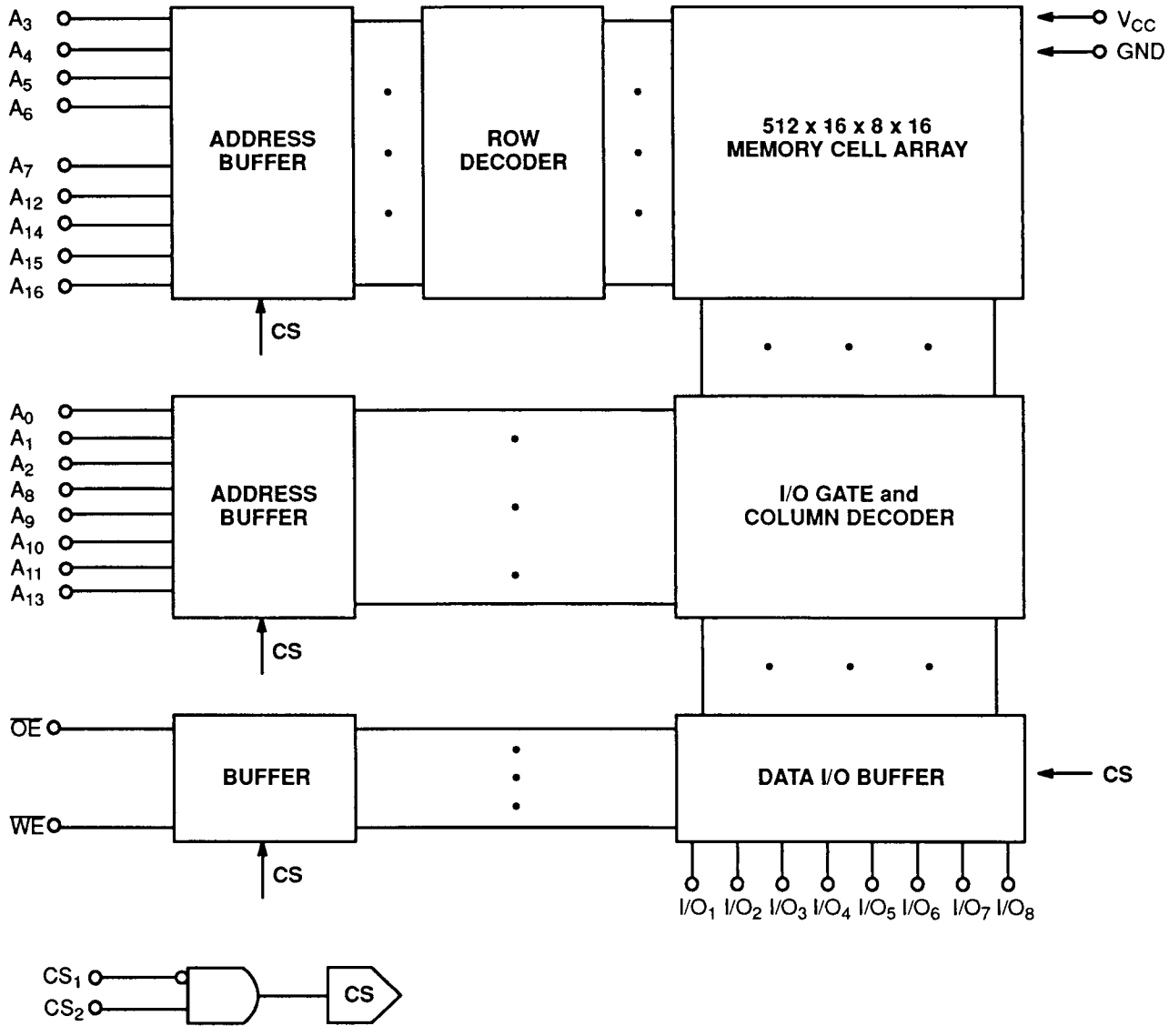
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−45 to +125	°C

— Note —

Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. MB841000 BLOCK DIAGRAM



CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0 V)	CI/O			10	pF
Input Capacitance (V_{IN} = 0 V)	CIN			8	pF

PIN DESCRIPTION

Symbol	Pin Name	Symbol	Pin Name
A_0 to A_{16}	Address Input	$\overline{WE}$	Write Enable
I/O_1 to I/O_8	Data Input/Output	V_{CC}	Power Supply (5 V±10%)
$\overline{OE}$	Output Enable	GND	Ground
$\overline{CS}_1$	Chip Select 1	NC	Not Connected
CS_2	Chip Select 2		

FUNCTION TRUTH TABLE*

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High–Z
X	L	X	X	Not Selected	I_{SB}	High–Z
L	H	H	H	D_{OUT} Disable	I_{CC}	High–Z
L	H	L	H	Read	I_{CC}	D_{OUT}
L	H	X	L	Write	I_{CC}	D_{IN}

*Legend: H = High; L = Low Level; X – Don't Care

RECOMMENDED OPERATING CONDITION

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	0		70	°C

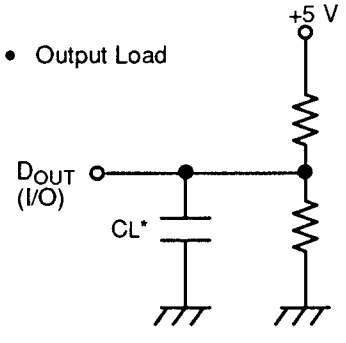
DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Test Condition	Symbol	MB841000-70L/-85L/-10L		MB841000-70/-85/-10 (LL and SL)		Unit
				Min	Max	Min	Max	
Standby Supply Current		$CS_2 \le 0.2$ V or $\overline{CS_1} \ge V_{CC}-0.2$ V ($CS_2 \le 0.2$ V or $CS_2 \ge V_{CC}-0.2$ V)	I_{SB1}		0.1		0.05	mA
		$\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$	I_{SB2}		3		3	mA
Active Supply Current		$V_{IN} = V_{IH}$ or V_{IL}, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$, $I_{OUT} = 0$ mA	I_{CC}		15		15	mA
Operating Supply Current	-70/-85	Cycle = Min., Duty = 100% $I_{OUT} = 0$ mA	I_{CC1}		80		80	mA
	-10				70		70	
Operating Supply Current		Cycle = 1µs, Duty = 100% $I_{OUT} = 0$ mA, $CS_2 \ge V_{CC}-0.2$ V, $\overline{CS_1} \le 0.2$ V, $V_{IL} \le 0.2$ V $V_{IH} \ge V_{CC}-0.2$ V	I_{CC2}		15		15	mA
Intput Leakage Current		$V_{IN} = 0$ V to V_{CC}	I_{LI}	−1	1	−1	1	µA
Output Leakage Current		$V_{I/O} = 0$ V to V_{CC}, $\overline{CS_1} = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	$I_{LI/O}$	−1	1	−1	1	µA
Input High Voltage[1]			V_{IH}	2.2	V_{CC} +0.3	2.2	V_{CC} +0.3	V
Input Low Voltage[1]			V_{IL}	−0.3[2]	0.8	−0.3[2]	0.8	V
Output High Voltage[1]		$I_{OH} = -1.0$ mA	V_{OH}	2.4		2.4		V
Output Low Voltage[1]		$I_{OL} = 2.1$ mA	V_{OL}		0.4		0.4	V

Notes: [1] All voltages are referenced to GND.
[2] −3.0 V min. for pulse width less than 20 ns. (V_{IL} min. = −0.3 V at DC level.

Fig.2 – AC TEST CONDITIONS



- Output Load
- Input Pulse Levels: 0.6 V to 2.4 V
- Input Pulse Rise and Fall Times: 5 ns (Transient between 0.8 V and 2.2 V)
- Timing Reference Levels: Input :V_{IL} = 0.8 V, V_{IH} = 2.2 V
  Output :V_{OL} = 0.8 V, V_{OH} = 2.0 V

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8K Ω	990 Ω	100 pF	except tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ
Load II	1.8K Ω	990 Ω	5 pF	tCLZ, tOLZ, tCHZ, tOHZ, tWLZ and tWHZ

AC CHARACTERISTICS

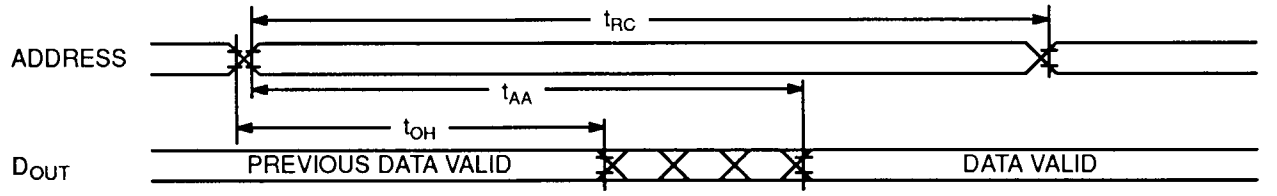
(Recommended operating conditions unless otherwise noted.)

READ Cycle[1]

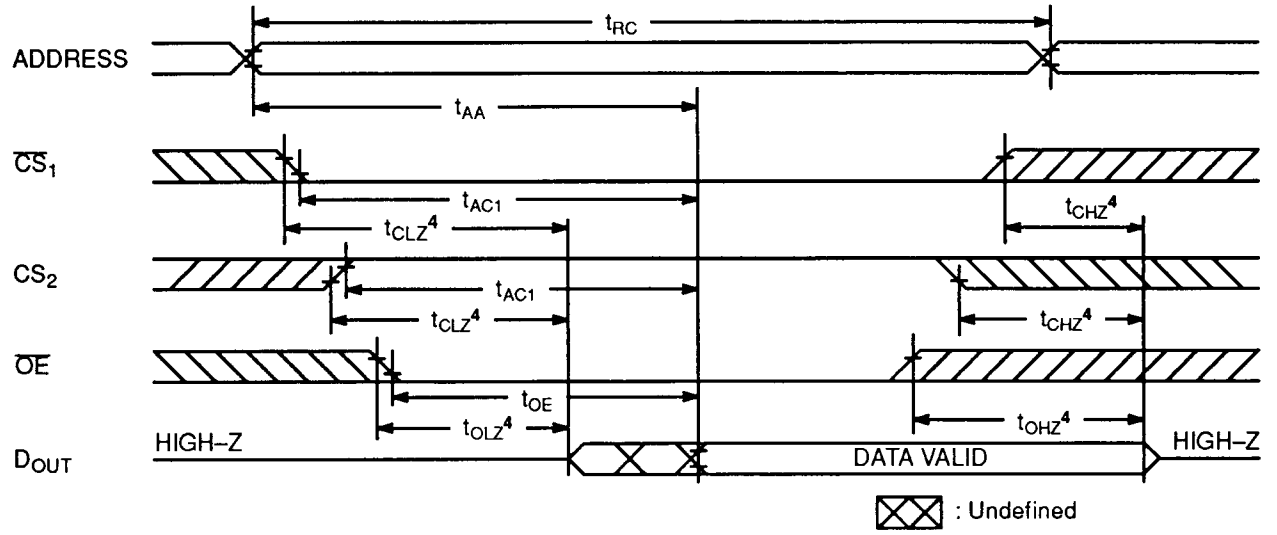
Parameter	Symbol	MB841000-70L/-70LL/-70SL		MB841000-85L/-85LL/-85SL		MB841000-10L/-10LL/-10SL		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		ns
Address Access Time[2]	t_{AA}		70		85		100	ns
$\overline{CS}_1$ Access Time[3]	t_{AC1}		70		85		100	ns
CS2 Access Time[3]	t_{AC2}		70		85		100	ns
Output Enable to Output Valid	t_{OE}		35		40		45	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns
Chip Select lto Output Low-Z[4]	t_{CLZ}	10		10		10		ns
Output Enable lto Output Low-Z[4]	t_{OLZ}	5		5		5		ns
Chip Select lto Output High-Z[4]	t_{CHZ}		25		30		35	ns
Output Enable lto Output High-Z[4]	t_{OHZ}		25		30		35	ns

READ Cycle Timing Diagram[1]

READ Cycle 1: ADDRESS CONTROLLED[2]



READ CYCLE 2: $\overline{CS1}$, CS2 CONTROLLED[3]



Notes: [1] $\overline{WE}$ is high for Read Cycle.

[2] Device is continuously selected, $\overline{CS_1} = \overline{OE} = V_{IL}$, $CS_2 = V_{IH}$.

[3] Address is valid prior to, or coinciding with, $\overline{CS_1}$ transition low, or CS_2 transition high.

[4] Transition is measured at the point of ±500 mV from a steady state voltage with Load II as specified in Fig. 2.

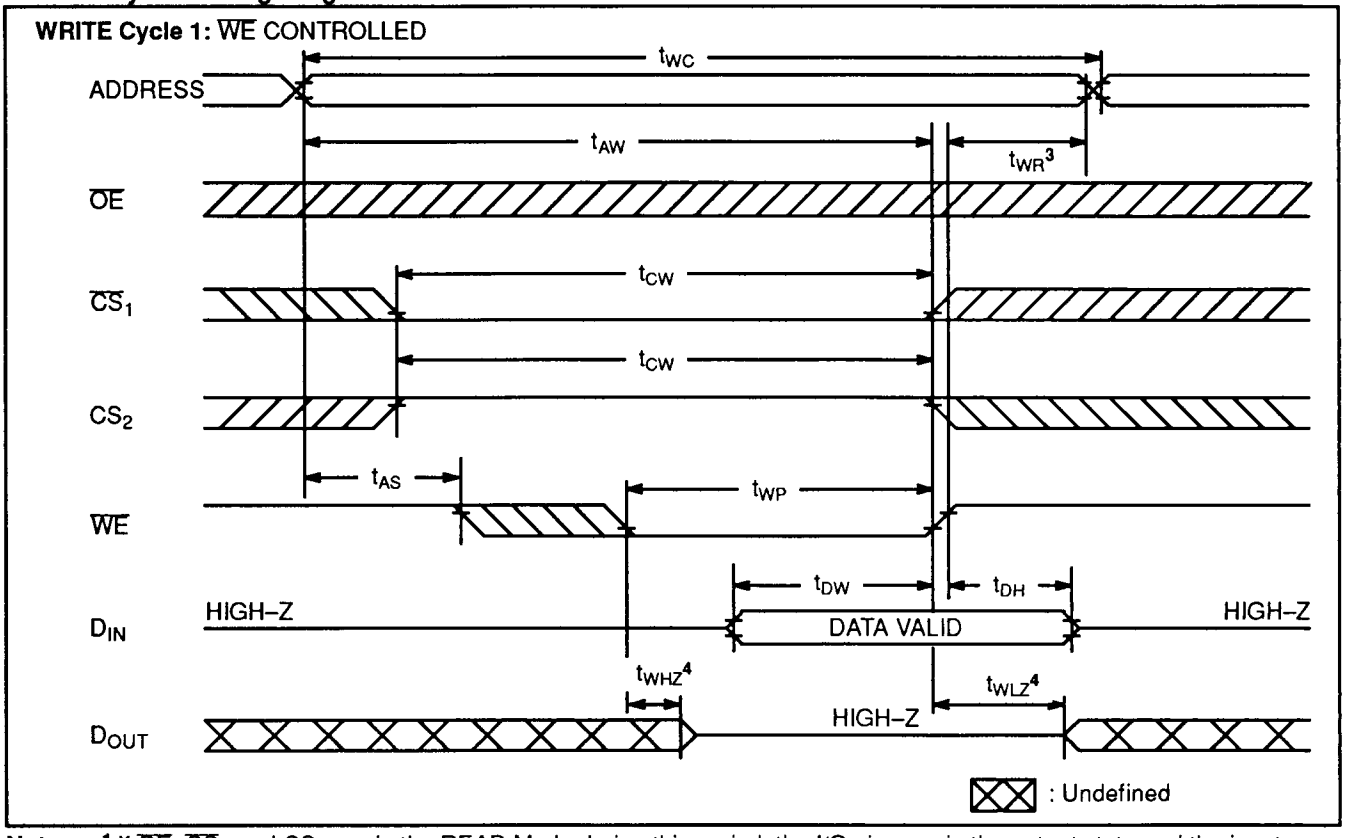
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE Cycle[1,2]

Parameter	Symbol	MB841000-70L/-70LL/-70SL		MB841000-85L/-85LL/-85SL		MB841000-10L/-10LL/-10SL		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		ns
Address Valid to End of Write	t_{AW}	55		70		85		ns
Chip Select to End of Write	t_{CW}	55		70		85		ns
Data Valid to End of Write	t_{DW}	35		35		40		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Pulse Width	t_{WP}	50		60		70		ns
Address Setup Time	t_{AS}	0		0		0		ns
Write Recovery Time[3]	t_{WR}	0		0		0		ns
Write Enable to Output Low[4]	t_{WLZ}	5		5		5		ns
Write Enable to Output High[4]	t_{WHZ}		25		30		35	ns

WRITE Cycle Timing Diagram[1,2]



Notes: [1] If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of the phase opposite to the outputs must not be applied.

[2] If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

[3] t_{WR} is defined from the end point of the WRITE Mode.

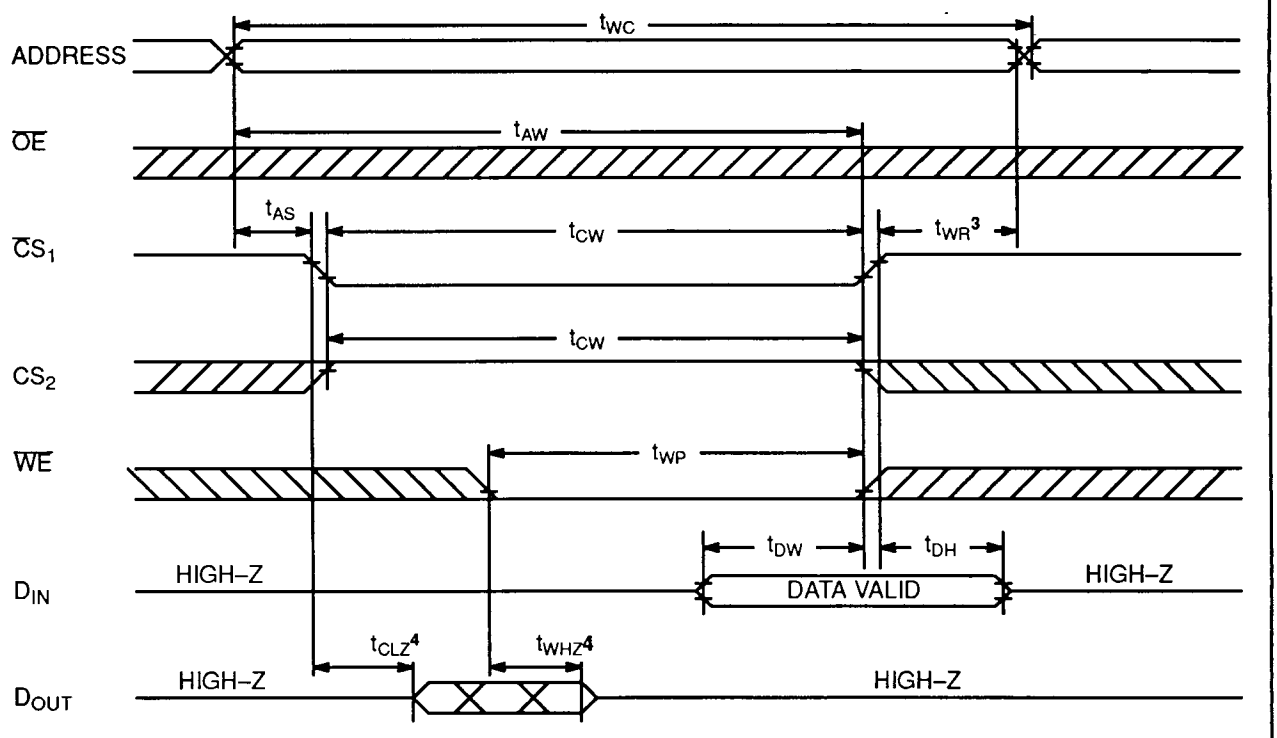
[4] Transition is measured at the point of ±500 mV from a steady state voltage with Load II as specified in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE Cycle Timing Diagram[1,2]

WRITE Cycle 2: $\overline{CS}_1$ CONTROLLED



Notes: [1] If $\overline{OE}$, $\overline{CS}_1$ and CS_2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of the phase opposite to the outputs must not be applied.

[2] If $\overline{CS}_1$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

[3] t_{WR} is defined from the end point of the WRITE Mode.

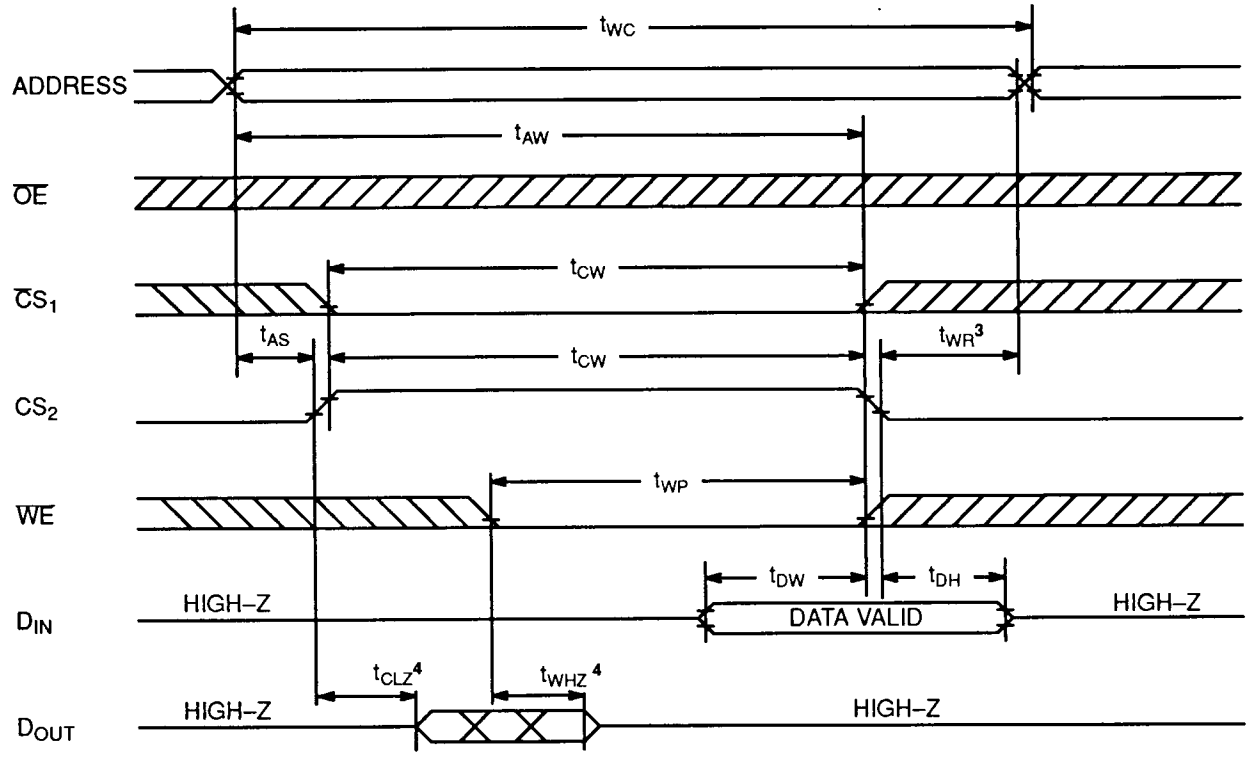
[4] Transition is measured at the point of ±500 mV from a steady state voltage with Load II as specified in Fig. 2.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

WRITE Cycle Timing Diagram[1,2]

WRITE Cycle 3: CS_2 CONTROLLED



Notes: [1] If $\overline{OE}$, $\overline{CS_1}$ and CS_2 are in the READ Mode during this period, the I/O pins are in the output state and the input signals of the phase opposite to the outputs must not be applied.

[2] If $\overline{CS_1}$ goes high or CS_2 goes low simultaneously with $\overline{WE}$ high, the output remains in high impedance state.

[3] t_{WR} is defined from the end point of the WRITE Mode.

[4] Transition is measured at the point of ±500 mV from a steady state voltage with Load II as specified in Fig. 2.

DATA RETENTION CHARACTERISTICS

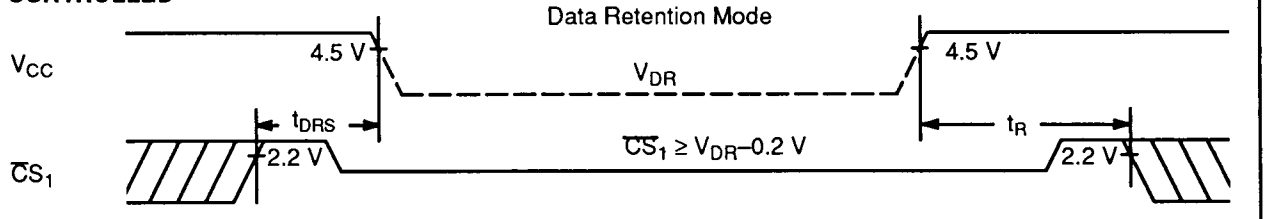
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Data Retention Supply Voltage		V_{DR}	2.0		5.5	V
Data Retention Supply Current[1]	L-Version	I_{DR}			0.05	mA
	LL-Version				0.04[2]	
	SL-Version				0.02[3]	
Data Retention Setup Time		t_{DRS}	0			ns
Operation Recovery Time[4]		t_R	t_{RC}			ns

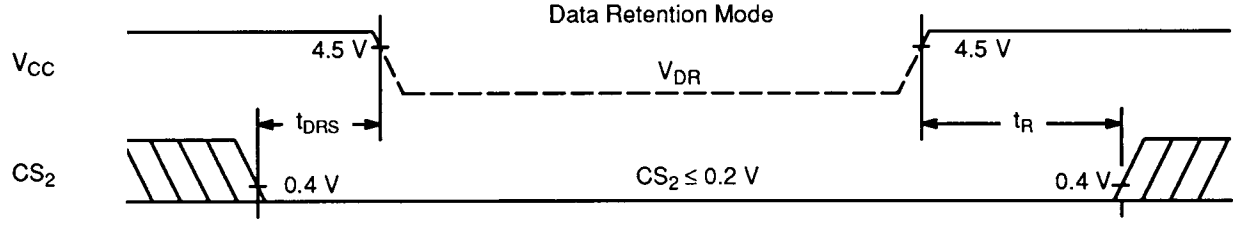
Notes: [1] $V_{CC} = V_{DR} = 3.0$ V
$\overline{CS_1} \geq V_{DR}-0.2$ V, $CS_2 \geq V_{DR}-0.2$ V or $CS_2 \leq 0.2$ V (at CS_1 CONTROLLED)
$CS_2 \leq 0.2$ V (at CS_2 CONTROLLED)
[2] $I_{DR} = 6$ µA max. at $V_{DR} = 3$ V, TA = 0°C to +40°C
[3] $I_{DR} = 3$ µA max. at $V_{DR} = 3$ V, TA = 0°C to +40°C
[4] t_{RC}: Read Cycle Time

Data Retention Timing

$\overline{CS_1}$ CONTROLLED



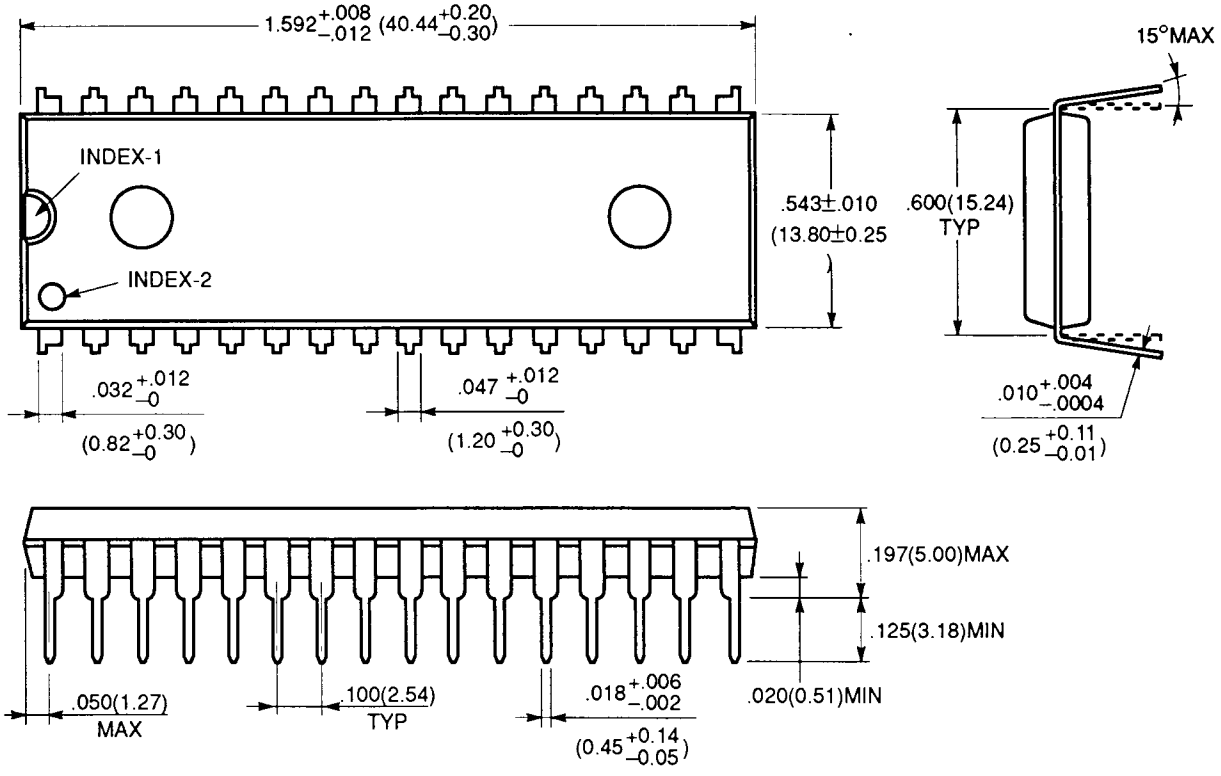
CS_2 CONTROLLED



PACKAGE DIMENSIONS

(Suffix: P)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-32P-M01)

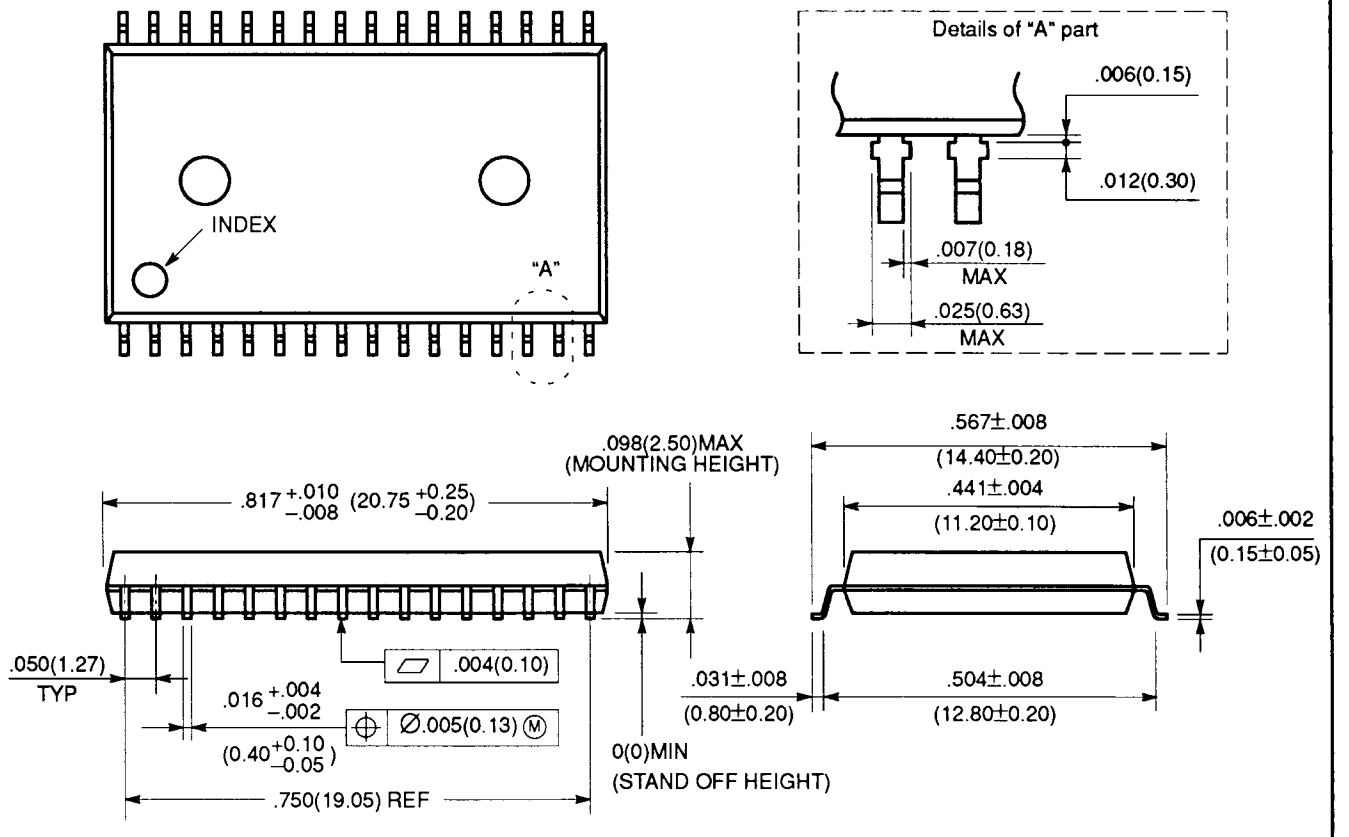


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PF)

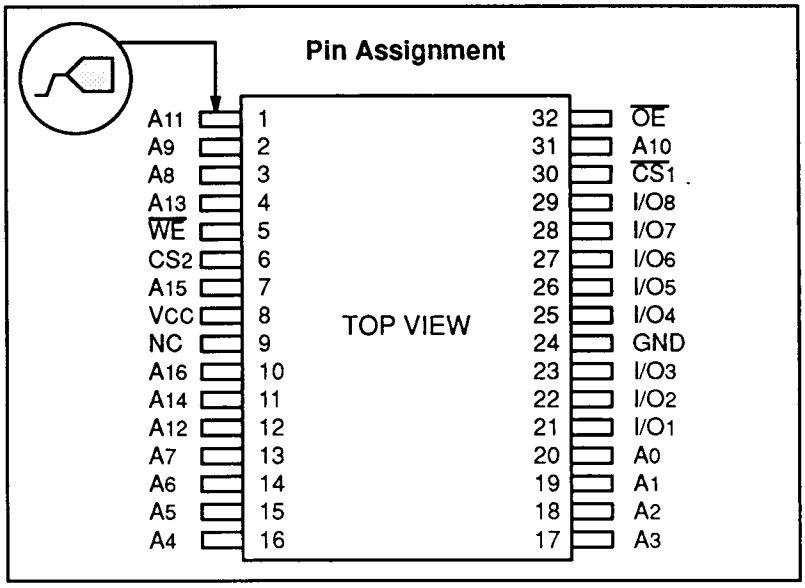
32-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-32P-M03)



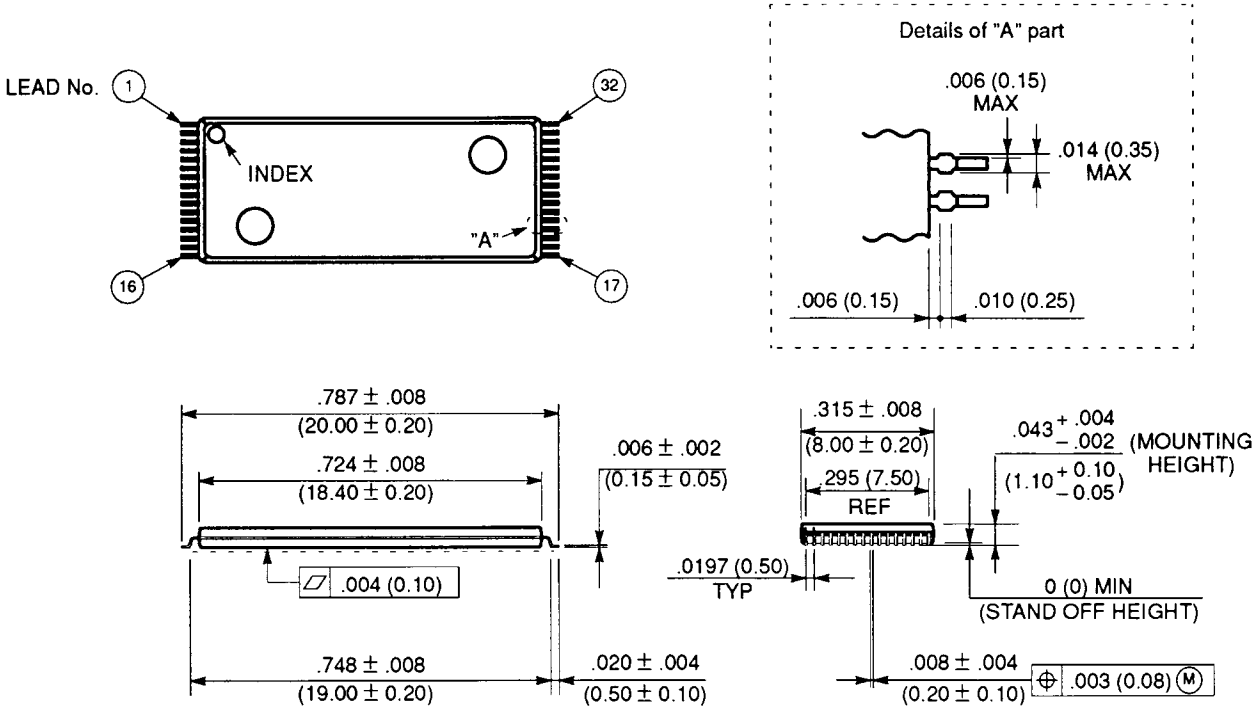
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PFTN)



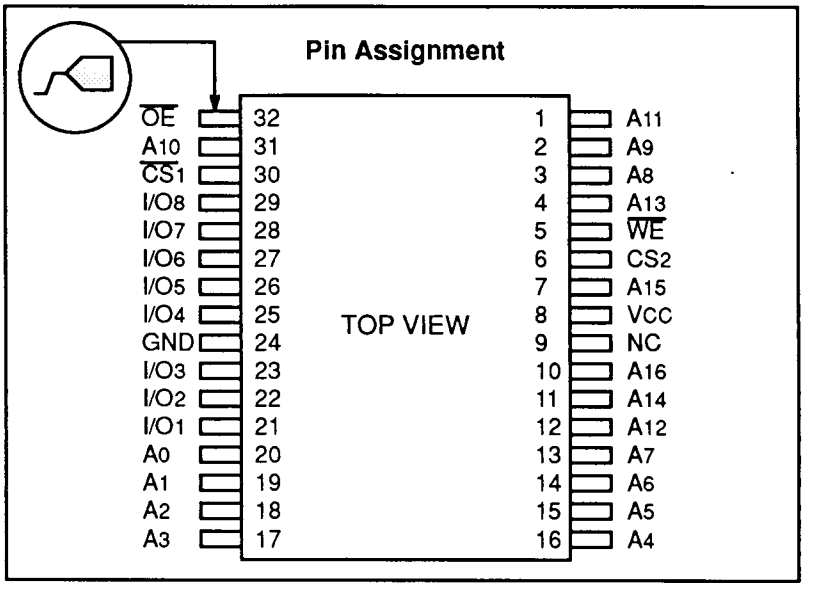
32–LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT–32P–M06)



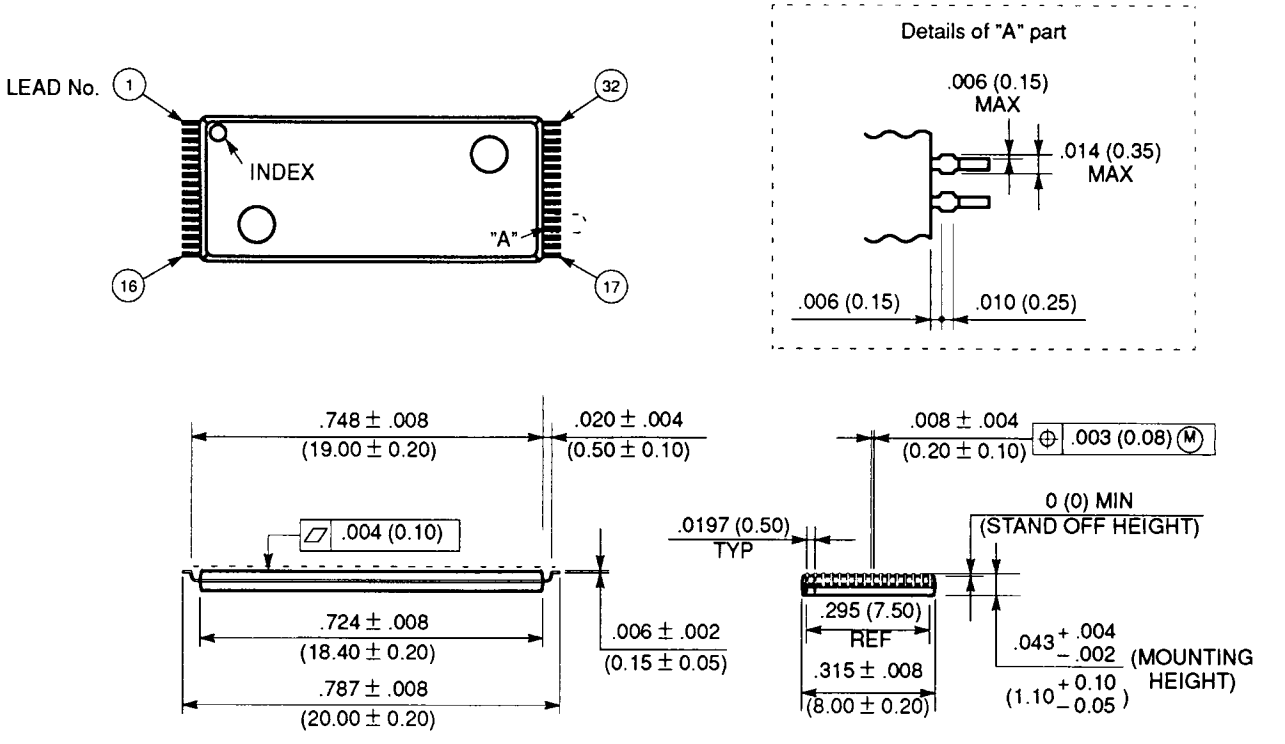
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PFTR)



32–LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT–32P–M07)



Dimensions in inches (millimeters)

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