# KS54AHCT 595/596
# KS74AHCT

## 8-Bit Shift Registers with Output Registers

T-46-07-05

## FEATURES

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage.
- Choice of 3-State ('595) or Open-Drain ('596) Parallel Outputs.
- Shift Register Has Direct Clear.
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL}$ = 24 mA @ $V_{OL}$ = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74AHCT: −40°C to +85°C
  KS54AHCT: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

## DESCRIPTION

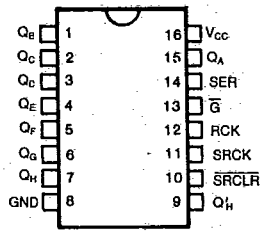
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('595) or open-drain ('596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

## PIN CONFIGURATION



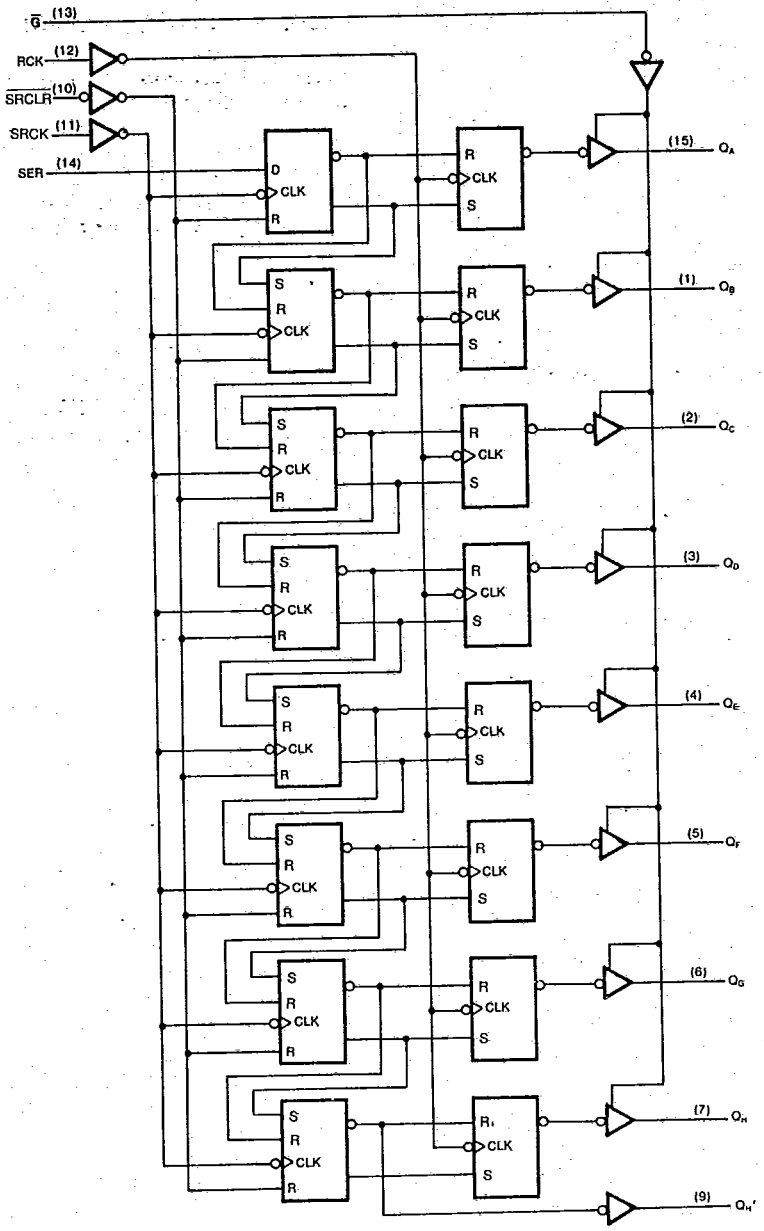

## FUNCTION TABLE

| INPUTS | | | | | FUNCTION |
|---|---|---|---|---|---|
| SER | SRCK | $\overline{SRCLR}$ | RCK | $\overline{G}$ | |
| X | X | X | X | H | $Q_A$ thru $Q_H$ outputs disable |
| X | X | X | X | L | $Q_A$ thru $Q_H$ outputs enable |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively. |
| X | ↓ | H | X | X | State of S.R. is not changed. |
| X | X | X | ↑ | X | S.R. data is stored into storage register. |
| X | X | X | ↓ | X | Storage register state is not changed. |

X: DON'T CARE

## LOGIC DIAGRAM

'595 or '596



# KS54AHCT KS74AHCT 595/596

## 8-Bit Shift Registers with Output Registers T-46-07-05

### Absolute Maximum Ratings*

Supply Voltage Range $V_{CC}$, ..... −0.5V to +7V
DC Input Diode Current, $I_{IK}$
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ..... ±20 mA
DC Output Diode Current, $I_{OK}$
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) .... ±20 mA
Continuous Output Current Per Pin, $I_O$
($-0.5V < V_O < V_{CC} + 0.5V$) ..... ±70 mA
Continuous Current Through
$V_{CC}$ or GND pins ..... ±250 mA
Storage Temperature Range, $T_{stg}$ ... −65°C to +150°C
Power Dissipation Per Package, $P_d$† ..... 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

### Recommended Operating Conditions

Supply Voltage, $V_{CC}$ ..... 4.5V to 5.5V
DC Input & Output Voltages*, $V_{IN}$, $V_{OUT}$ .. 0V to $V_{CC}$
Operating Temperature
Range KS74AHCT: −40°C to +85°C
KS54AHCT: −55°C to +125°C
Input Rise & Fall Times, $t_r$, $t_f$ ..... Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either $V_{CC}$ or GND)

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$=5V±10% Unless Otherwise Specified)

| Characteristic | Symbol | Test Conditions | $T_a$=25°C | KS74AHCT $T_a$=−40°C to +85°C | KS54AHCT $T_a$=−55°C to +125°C | Unit |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | |
| Minimum High-Level Input Voltage | $V_{IH}$ | | | 2.0 | 2.0 | 2.0 | V |
| Maximum Low-Level Input Voltage | $V_{IL}$ | | | 0.8 | 0.8 | 0.8 | V |
| Minimum High-Level Output Voltage (All '595 Outputs and '596 $Q_H$' Output) | $V_{OH}$ | $V_{IN}=V_{IH}$ or $V_{IL}$<br>$I_O=-20\mu A$<br>$I_O=-6mA$ | $V_{CC}$<br>4.2 | $V_{CC}-0.1$<br>3.98 | $V_{CC}-0.1$<br>3.84 | $V_{CC}-0.1$<br>3.7 | V |
| Maximum Low-Level Output Voltage | $V_{OL}$ | $V_{IN}=V_{IH}$ or $V_{IL}$<br>$I_O=20\mu A$<br>$I_O=12mA$<br>$I_O=24mA$ | 0 | 0.1<br>0.26<br>0.39 | 0.1<br>0.33<br>0.5 | 0.1<br>0.4 | V |
| Maximum Input Current | $I_{IN}$ | $V_{IN}=V_{CC}$ or GND | | ±0.1 | ±1.0 | ±1.0 | μA |
| Maximum 3-State Leakage Current | $I_{OZ}$ | Output Enable<br>$=V_{IH}$<br>$V_{OUT}=V_{CC}$ or GND | | ±0.5 | ±5.0 | ±10.0 | μA |
| Maximum Quiescent Supply Current | $I_{CC}$ | $V_{IN}=V_{CC}$ or GND<br>$I_{OUT}=0\mu A$ | | 8.0 | 80.0 | 160.0 | μA |
| Additional Worst Case Supply Current | $\Delta I_{CC}$ | per input pin<br>$V_I=2.4V$<br>other Inputs:<br>at $V_{CC}$ or GND<br>$I_{OUT}=0\mu A$ | | 2.7 | 2.9 | 3.0 | mA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r$, $t_f$≤2 ns), AHCT595, AHCT596

| Characteristic | | Symbol | Conditions† | | $T_a$=25°C $V_{CC}$=5.0V Typ | KS74AHCT $T_a$=−40°C to +85°C $V_{CC}$=5.0V±10% Min | KS74AHCT Max | KS54AHCT $T_a$=−55°C to +125°C $V_{CC}$=5.0V± 10% Min | KS54AHCT Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay, SRCK↑ to $Q'_H$ | | $t_{PLH}$ | $C_L$=50pF | | 9 | | 25 | | 18 | ns |
| | | $t_{PHL}$ | | | 9 | | 15 | | 18 | |
| Propagation Delay, RCK↑ to $Q_A$ thru $Q_H$ | | $t_{PLH}$ | $C_L$=50pF<br>$C_L$=150pF | | 11<br>14 | | 16<br>21 | | 19<br>25 | ns |
| | | $t_{PHL}$ | $C_L$=50pF<br>$C_L$=150pF | | 11<br>14 | | 17<br>22 | | 20<br>26 | |
| Output Enable Time, $\overline{G}$↓ to $Q_A$ thru $Q_H$ ('595 only) | | $t_{PZH}$ | $R_L$=1kΩ | $C_L$=50pF<br>$C_L$=150pF | 14<br>17 | | 20<br>25 | | 24<br>30 | ns |
| | | $t_{PZL}$ | $R_L$=1kΩ | $C_L$=50pF<br>$C_L$=150pF | 14<br>17 | | 20<br>25 | | 24<br>30 | |
| Output Disable Time, $\overline{G}$↑ to $Q_A$ thru $Q_H$ ('595 only) | | $t_{PHZ}$ | $R_L$=1kΩ<br>$C_L$=50pF | | 14 | | 20 | | 24 | ns |
| | | $t_{PLZ}$ | | | 14 | | 20 | | 24 | |
| Propagation Delay, $\overline{G}$↑ to $Q_A$ thru $Q_H$ ('596 only) | | $t_{PLH}$ | $C_L$=50pF<br>$C_L$=150pF | | 14<br>17 | | 20<br>25 | | 24<br>30 | ns |
| Propagation Delay, $\overline{G}$↓ to $Q_A$ thru $Q_H$ ('596 only) | | $t_{PHL}$ | $C_L$=50pF<br>$C_L$=150pF | | 14<br>17 | | 20<br>25 | | 24<br>30 | ns |
| Pulse Width | SRCK or RCK | $t_w$ | | | 10 | 15 | | 20 | | ns |
| | $\overline{SRCLR}$ Low | | | | 10 | 15 | | 20 | | |
| Setup Time | $\overline{SRCLR}$↑ to SRCK↑ | $t_{su}$ | | | 6 | 10 | | 12 | | ns |
| | SER to SRCK↑ | | | | 10 | 15 | | 20 | | |
| | SRCK↑ to RCK↑↑ | | | | 15 | 20 | | 25 | | |
| Hold Time, | | $t_h$ | | | −3 | 0 | | 0 | | ns |
| Input Capacitance | | $C_{IN}$ | | | 5 | | | | | pF |
| Output Capacitance | | $C_{OUT}$ | Output Disabled | | 10 | | | | | pF |
| Power Dissipation Capacitance* | | $C_{PD}$ | | | | | | | | pF |

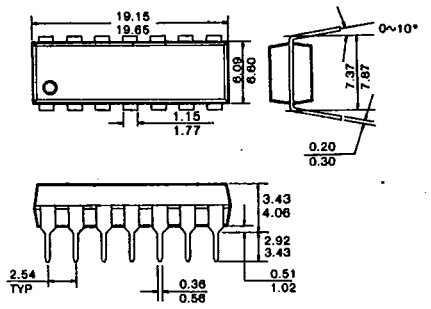
* $C_{PD}$ determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
† For AC switching test circuits and timing waveforms see section 2.
†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

## PACKAGE DIMENSIONS

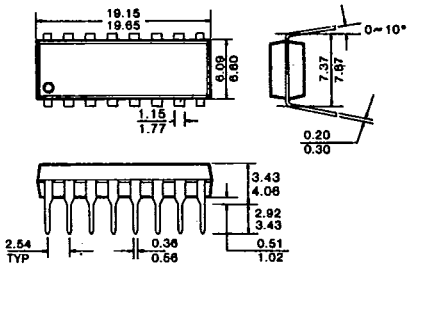
T-90-20

### 1. PLASTIC PACKAGES

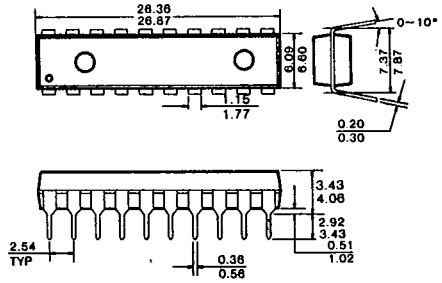
**14-Pin Plastic DIP** **Units: mm**



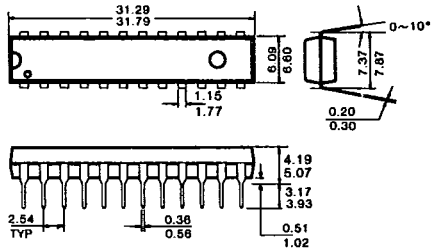

**16-Pin Plastic DIP** **Units: mm**




**20-Pin Plastic DIP** **Units: mm**




**24-Pin Plastic DIP** **Units: mm**

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## PACKAGE DIMENSIONS

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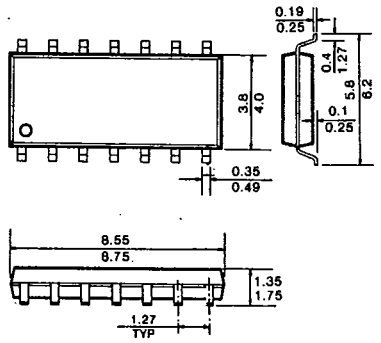
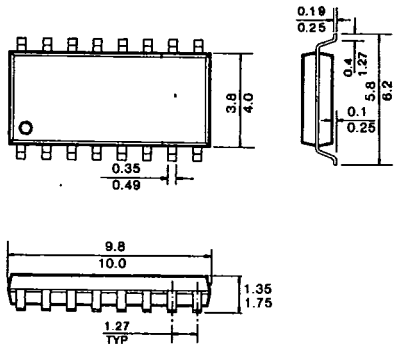
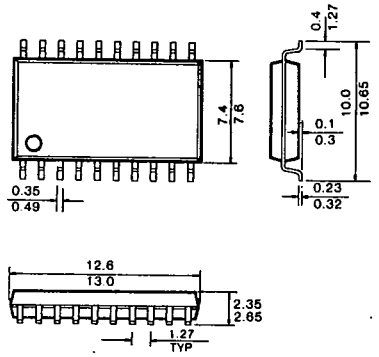
**14-Pin SOP** Unit: mm



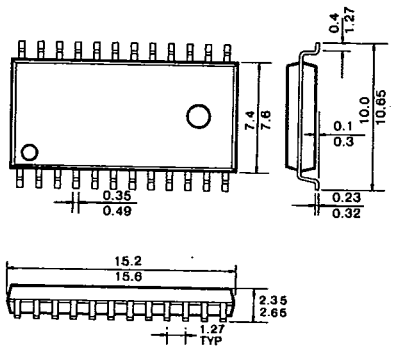

**16-Pin SOP** Unit: mm




**20-Pin SOP** Unit: mm




**24-Pin SOP** Unit: mm

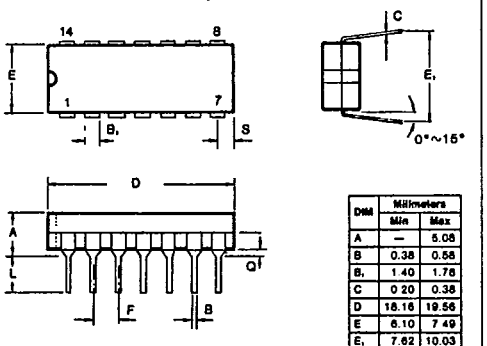


## PACKAGE DIMENSIONS

T-90-20

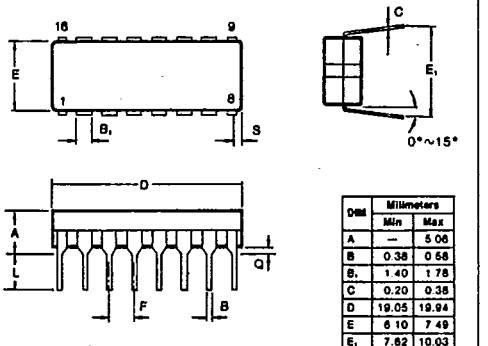
### 2. CERAMIC PACKAGES

**14-Pin Ceramic DIP Units: mm**



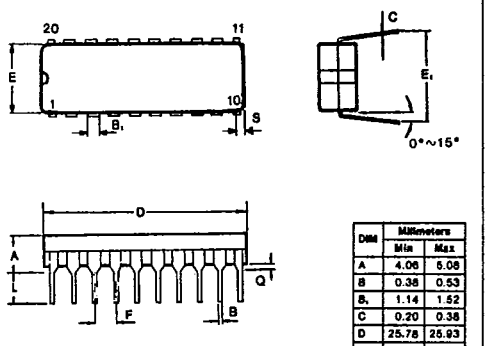

| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | — | 5.08 |
| B | 0.38 | 0.58 |
| B1 | 1.40 | 1.78 |
| C | 0.20 | 0.38 |
| D | 18.16 | 19.56 |
| E | 6.10 | 7.49 |
| E1 | 7.62 | 10.03 |
| F | 2.54 | |
| L | 3.18 | 4.19 |
| Q | 0.51 | 1.02 |
| S | 1.91 | 2.29 |

**16-Pin Ceramic DIP Units: mm**



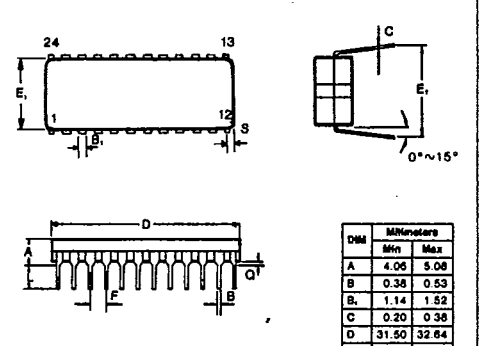

| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | — | 5.08 |
| B | 0.38 | 0.58 |
| B1 | 1.40 | 1.78 |
| C | 0.20 | 0.38 |
| D | 19.05 | 19.94 |
| E | 6.10 | 7.49 |
| E1 | 7.62 | 10.03 |
| F | 2.54 | |
| L | 3.18 | 4.19 |
| Q | 0.51 | 1.02 |
| S | 0.51 | 1.14 |

**20-Pin Ceramic DIP Units: mm**




| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 4.06 | 5.08 |
| B | 0.38 | 0.53 |
| B1 | 1.14 | 1.52 |
| C | 0.20 | 0.38 |
| D | 25.78 | 25.93 |
| E | 6.10 | 6.60 |
| E1 | 7.77 | 7.98 |
| F | 2.54 | |
| L | 3.73 | 4.01 |
| Q | 0.38 | 0.89 |
| S | 0.51 | 1.14 |

**24-Pin Ceramic DIP Units: mm**




| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 4.06 | 5.08 |
| B | 0.38 | 0.53 |
| B1 | 1.14 | 1.52 |
| C | 0.20 | 0.38 |
| D | 31.50 | 32.64 |
| E | 7.24 | 7.75 |
| E1 | 7.77 | 7.98 |
| F | 2.54 | |
| L | 3.73 | 4.01 |
| Q | 0.508 | 1.778 |
| S | 1.65 | 1.93 |

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