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ECL Products	

10125
Gate

Quad ECL-to-TTL Translator

FEATURES

- **Typical propagation delay: 3.5ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10125 is a Quad ECL-to-TTL Translator for interfacing data between two different logic systems. It also provides a separate Reference Bias Voltage output (V_{BB}) to be used in case of single-ended input busing. Input and output levels are, respectively, ECL 10K and TTL Schottky. This device features a peak common-mode rejection voltage of ± 1V.

The 10125 outputs are designed to go to a Low logic level whenever both inputs are left open.

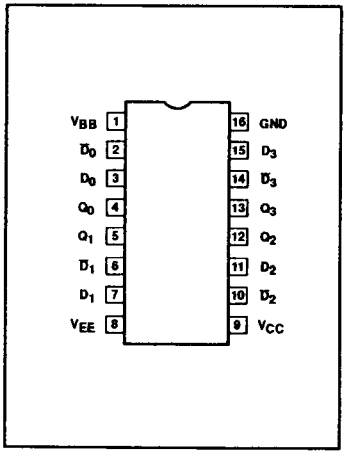
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10125N
16–Pin Ceramic DIP	10125F
16–Pin SO	10125D

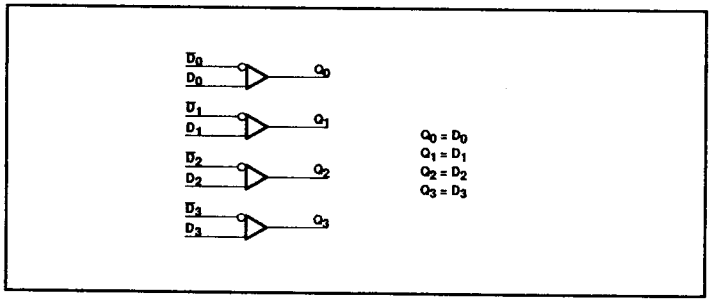
PIN DESCRIPTION

PINS	DESCRIPTION
$D_0 - D_3$, $\overline{D}_0 - \overline{D}_3$	Data Inputs (ECL 10K)
V_{BB}	Reference Bias Voltage Output (ECL 10K)
$Q_0 - Q_3$	Data Outputs (Schottky TTL)

PIN CONFIGURATION



LOGIC DIAGRAM



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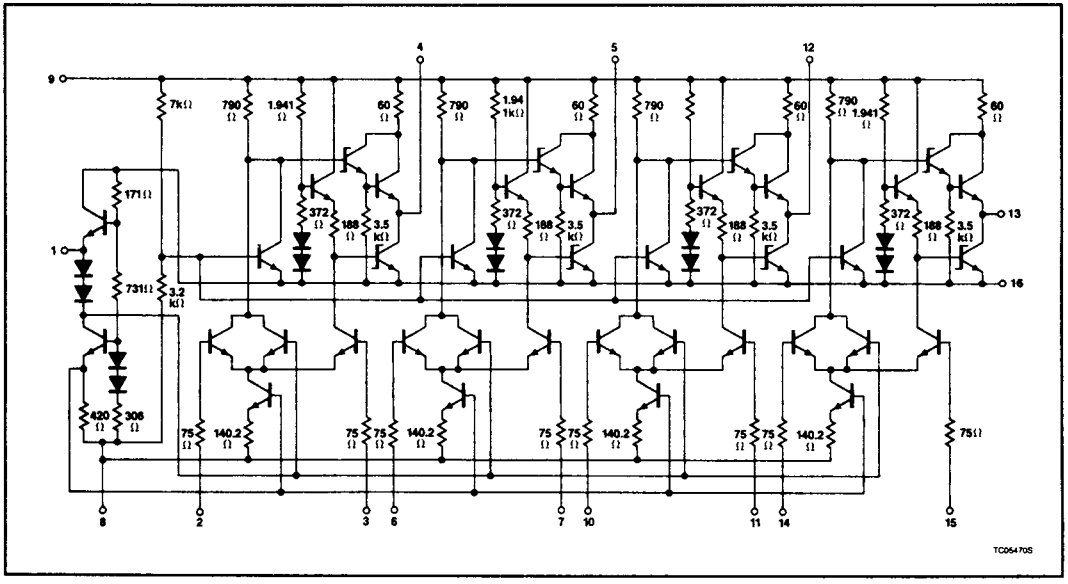
SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage (negative)		–8.0	V
V_{CC}	Supply voltage (positive)		+7.0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		+0.5 to V_{EE}	V
V_{OUT}	Voltage applied to output in High–State		–0.5 to +V_{CC}	V
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
GND	Device ground (common)		0	0	0	V
V_{CC}	Supply voltage (positive)			+5.0		V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C	1.8		–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC OPERATING CONDITIONS FOR COMMON–MODE REJECTION TEST

GND = ground, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{IHH}	V_{IHMAX} +1.0V	T_A = –30°C			+110	mV
		T_A = +25°C			+190	mV
		T_A = +85°C			+300	mV
V_{IHL}	V_{IHMAX} –1.0V	T_A = –30°C			–1890	mV
		T_A = +25°C			–1810	mV
		T_A = +85°C			–1700	mV
V_{ILH}	V_{ILMIN} +1.0V	T_A = –30°C	–890			mV
		T_A = +25°C	–850			mV
		T_A = +85°C	–825			mV
V_{ILL}	V_{ILMIN} –1.0V	T_A = –30°C	–2890			mV
		T_A = +25°C	–2850			mV
		T_A = +85°C	–2825			mV

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

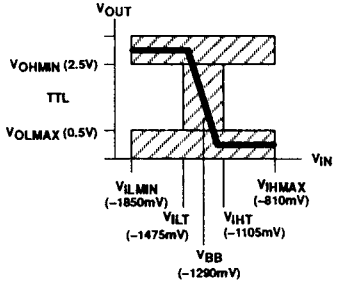
GND = ground, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V, T_A = –30°C to +85°C unless otherwise specified[1,4]

SYMBOL	PARAMETER	TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage	Apply V_{IHMAX} to all non–inverting inputs with V_{BB} applied to all inverting inputs. Force –2.0mA on measureed output.[5]		2.5			V
V_{OL}	Low level output voltage	Apply V_{ILMIN} to all non–inverting inputs with V_{BB} applied to all inverting inputs. Force 20mA on measureed output.[5]				0.5	V
V_{OH}	High level output voltage for CMR test	Apply V_{IHH} to D_n and V_{ILH} to $\overline{D}_n$ inputs. Apply V_{IHL} to D_n and V_{ILL} to $\overline{D}_n$ inputs. Force –2.0mA on measured output.		2.5			V
V_{OL}	Low level output voltage for CMR test	Apply V_{IHH} to $\overline{D}_n$ and V_{ILH} to D_n inputs. Apply V_{IHL} to $\overline{D}_n$ and V_{ILL} to D_n inputs. Force +20mA on measured output.				0.5	V
V_{OLS1}	Indeterminate input protection test	Apply V_{EE} to all inputs. Force 20mA on measured output.				0.5	V
V_{OLS2}	Indeterminate input protection test	All inputs left floating. Force 20mA on measured output.				0.5	V
V_{BB}	Reference bias voltage	T_A = –30°C	Connect all inverting inputs to	–1420		–1280	mV
		T_A = +25°C	V_{BB} pin during test. All other	–1350	–1290	–1230	mV
		T_A = +85°C	inputs are not connected.	–1295		–1150	mV
I_{IH}	High level input current	T_A = –30°C	Apply V_{IHMAX} to each input under			180	µA
		T_A = +25°C	test, one at a time, with V_{ILMIN}			115	µA
		T_A = +85°C	applied to all other inputs.			115	µA
$-I_{CBO}$	Input leakage current	T_A = –30°C	Apply V_{EE} to each inverting input under test, one at			1.5	µA
		T_A = +25°C	at time, with V_{ILMIN} applied to all other inverting			1.0	µA
		T_A = +85°C	inputs and V_{BB} applied to all non–inverting inputs.[5]			1.0	µA
$-I_{EE}$	V_{EE} supply current	T_A = –30°C	Apply V_{BB} to all $\overline{D}_n$ inputs and V_{ILMIN} to all D_n inputs.			44	mA
		T_A = +25°C			30	40	mA
		T_A = +85°C				44	mA
$-I_{OS}$	Short circuit current[4]	T_A = –30°C	Apply V_{ILMIN} to all $\overline{D}_n$ input with V_{BB} applied	40		100	mA
		T_A = +25°C	to all D_n inputs. Test each output one at a time, with all other outputs unloaded.	40		100	mA
		T_A = +85°C	Force 0V (GND) on measured output.[4]	40		100	mA
I_{CCH}	Supply current output High	Apply V_{ILMIN} to all $\overline{D}_n$ inputs with V_{BB} applied to D_n inputs.				52	mA
I_{CCL}	Supply current output Low	Apply V_{IHMAX} to all $\overline{D}_n$ inputs with V_{BB} applied to D_n inputs.				39	mA
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation	T_A = +25°C			0.148		V/V

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high–speed test apparatus and/or sample–and–hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. Refer to DC Test Circuit.

TRANSFER CHARACTERISTICS



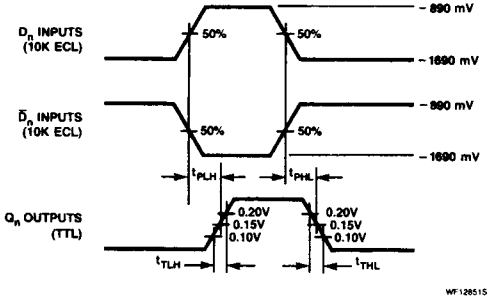
NOTES:
V_{IHMAX} = Maximum HIGH level input voltage (the most positive V_{IH}).
V_{IHT} = HIGH level input threshold voltage.
V_{ILT} = LOW level input threshold voltage.
V_{ILMIN} = Minimum LOW level input voltage (the most negative V_{IL}).
V_{OHMIN} = Minimum HIGH level output voltage (the most negative V_{OH}) under the specified input and loading condition.
V_{OLMAX} = Maximum LOW level output voltage (the most positive V_{OL}) under the specified input and loading conditions.
V_{BB} = Reference Bias Voltage. The internally generated reference voltage which is used to set the input and output threshold level.

AC ELECTRICAL CHARACTERISTICS GND = 0V, V_{CC} = +5.0V ± 0.010V, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = –30°C		T_A = +25°C			T_A = +85°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	1.00 1.00	6.00 6.00	1.00 1.00	4.50 4.50	6.00 6.00	1.00 1.00	6.00 6.00	ns ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%		0.50 0.50	3.30 3.30	0.50 0.50		3.30 3.30	0.50 0.50	3.30 3.30	ns ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

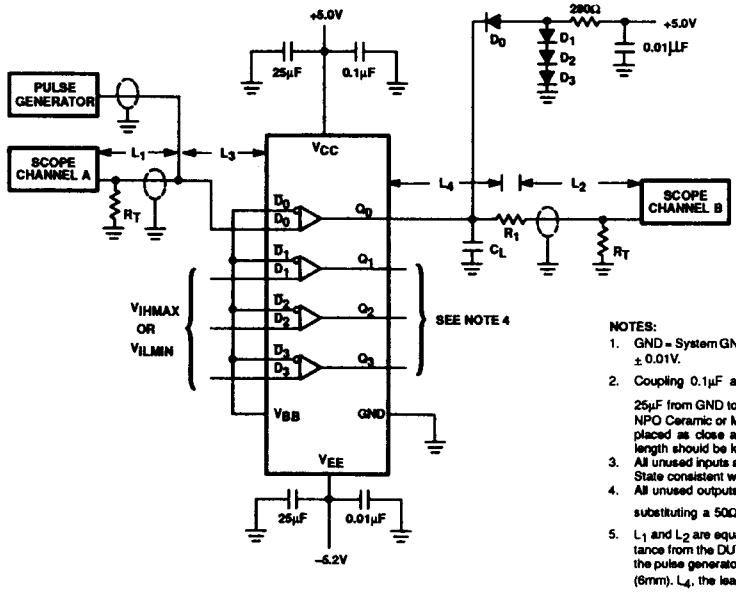
AC WAVEFORMS



NOTE:
The output waveform in Waveform 1 is shown with the actual output voltages of the AC Test Circuit which are attenuated by a factor of 10 as a result of the voltage divider formed by the 450Ω resistor and R_T.

Waveform 1. Propagation Delay and Transition Times

AC TEST CIRCUIT



NOTES:

1. GND = System GND (0V), V_{CC} = +5.0V ±0.010V, V_{EE} = -5.2V ± 0.01V.
2. Coupling 0.1μF and 25μF from GND to V_{CC}, 0.01μF and 25μF from GND to V_{EE} (0.01 and 0.1μF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either High- or Low-State consistent with the Logic function required.
4. All unused outputs are loaded identically to output under test, substituting a 50Ω termination for the scope.
5. L_1 and L_2 are equal length, 50Ω impedance lines. L_3, the distance from the DUT input pin to the junction of the cables from the pulse generator and the scope, should not exceed 1/4 inch (6mm). L_4, the lead length from the DUT output pin to R_1 and D_1, should not exceed 1/4 inch.
6. R_T = 50Ω termination internal to scope. R_1 = 450Ω.
7. C_L = 25pf including fixture and stray capacitance (not including scope cable capacitance).
8. Any unterminated stubs connected anywhere along the transmission line between the Pulse Generator and the DUT or between the DUT and the Scope should not exceed 1/4 inch (6mm) in length (refer to section AC setup procedure).
9. D_1 through D_4 are High Frequency (low capacitance) switching diodes.

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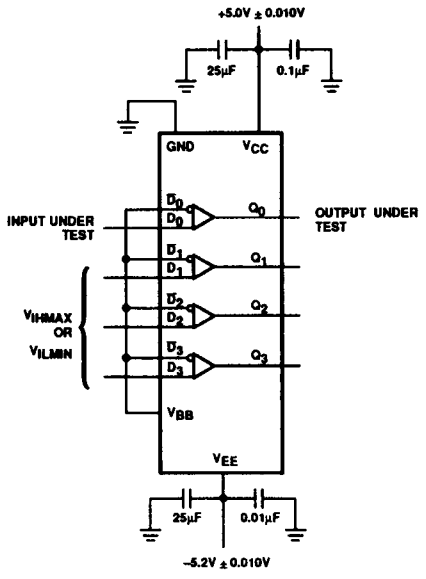
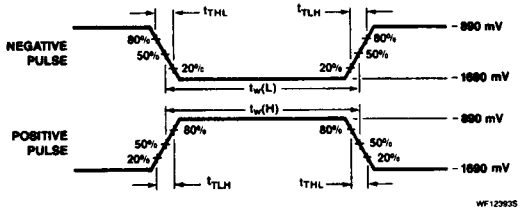
DC TEST CIRCUIT



NOTES:
1. GND = System GND (0V), V_{CC} = +5.0V ±0.010V, V_{EE} = −5.2V ± 0.01V.
2. Coupling 0.1µF and 25µF from GND to V_{CC}, 0.01µF and 25µF from GND to V_{EE} (0.01 and 0.1µF capacitors should be NPO Ceramic or MLC type). Decoupling capacitors should be placed as close as physically possible to the DUT and lead length should be kept to less than 1/4 inch (6mm).
3. All unused inputs should be connected to either High– or Low–State consistent with the Logic function required.
4. All unused outputs are open.

INPUT PULSE DEFINITION



INPUT PULSE REQUIREMENTS
GND = 0V, V_{CC} = +5.0V ± 0.010V, V_{EE} = -5.2V ± 0.010V, V_T = GND (0V)

Family	Amplitude	Rep Rate	Pulse Width	t_{TLH}	t_{THL}
10K ECL	800mVp-p	1MHz	500ns	2.0 ± 0.2ns	2.0 ± 0.2ns