SP8792 200MHz ÷ 80/81
SP8793 200MHz ÷ 40/41

The SP8792A and SP8793A are low power programmable +80/81 and +40/41 counters which operate over the full Military temperature range. They divide by 80(40) when the control input is in the high state and by 81(41) when in the low state.

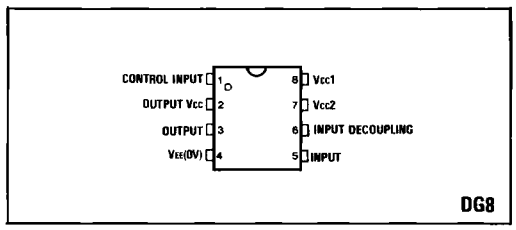


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: +5.2V
- Power Consumption: 26mW typical
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V pins 7 & 8 linked
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8792 A DG
SP8792 AB DG
SP8792 AC DG
SP8793 A DG
SP8793 AB DG
SP8793 AC DG

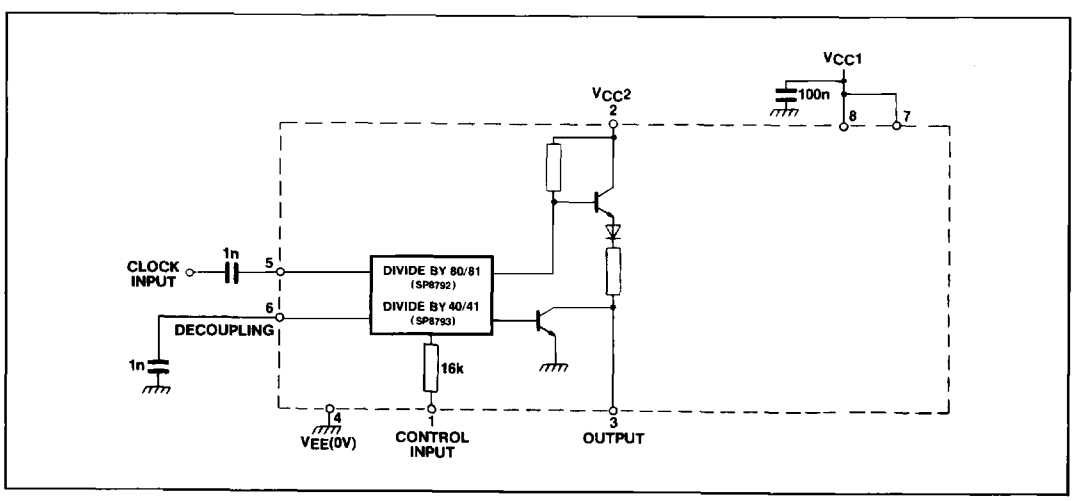


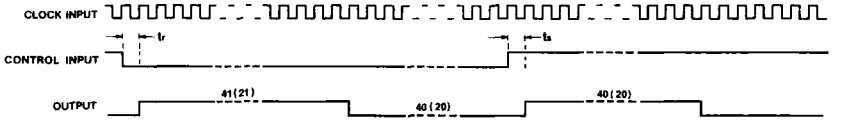
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =200 - 400mV p-p	
		150		MHz	Input =200 - 800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input =400mV p-p	
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC}= 4.95V I_{OH}= -100μA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set-up time	t_s	14		ns	25° C	Note 3
Release time	t_r	20		ns	25° C	Note 3
Clock to output propagation time	t_p		45	ns	25° C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

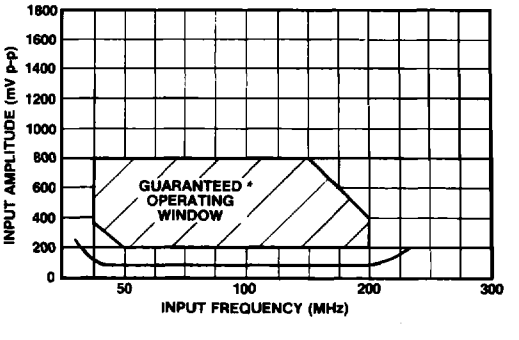


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792A	SP8793A
0	81	41
1	80	40

Fig.4 Input sensitivity (SP8792/3A)

NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L → H transition of the control input and the next L→H clock pulse transition to ensure that the ÷80(40) mode is selected.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷81(41) mode is selected.



OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6 to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k or greater resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pin 2, 7, and 8 should be connected together to give a fan-out = 1. Alternatively, the open collector output may be used with a pull-up resistor.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the circuit will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8792/3 to be used at supply voltages up to 9.5V is NOT available for use in the A Grade device: the SP8792A and SP8793A are ONLY available for operation from 5.2V supply, and therefore pins 7 and 8 should always be externally connected together.

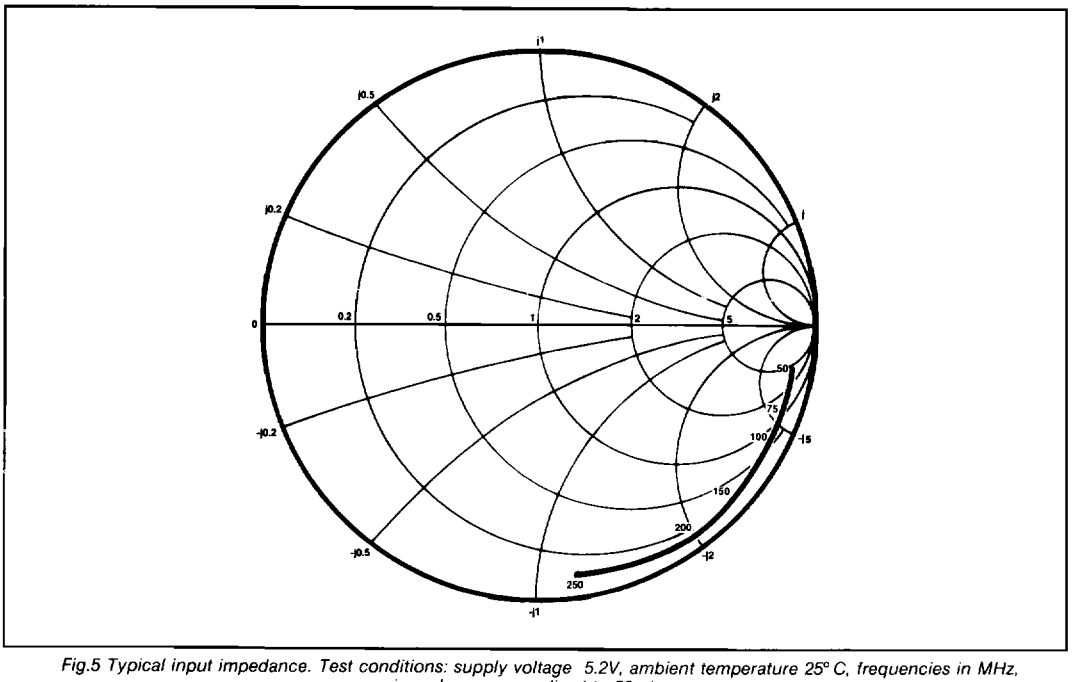


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

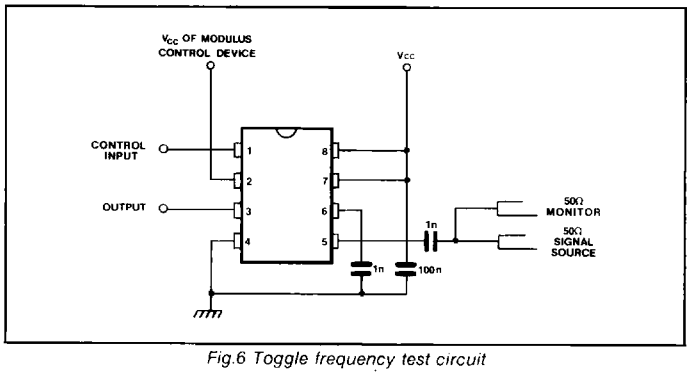


Fig.6 Toggle frequency test circuit