Signetics

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FAST Products	

FAST 74F777

Triple Bidirectional Latched Bus Transceiver

Triple Bidirectional Latched Bus Transceiver (3-State + Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F777	7ns	45mA

FEATURES

- **Latching Transceiver**
- **High drive open collector output current with minimum output swing**
- **Compatible with Test Mode (TM) Bus specification**
- **Controlled output ramp**
- **Multiple package options**

DESCRIPTION

The 74F777 is a triple bidirectional latched Bus transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristic impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with open collector B and 3-state A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC}.

ORDERING INFORMATION

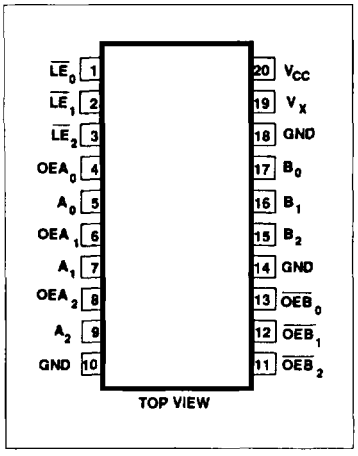
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP (300mil)	N74F777N
20-Pin PLCC	N74F777A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

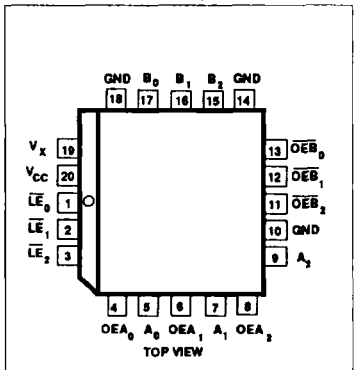
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	PNP latched inputs	3.5/0.117	70µA/70µA
B_0 - B_2	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA_0 - OEA_2	A Output Enable inputs (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$ - $\overline{OEB}_2$	B Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{LE}_0$ - $\overline{LE}_2$	Latch Enable inputs (active Low)	1.0/0.033	20µA/20µA
A_0 - A_2	3-State outputs	150/40	3mA/24mA
B_0 - B_2	Open Collector outputs	OC*/166.7	OC*/100mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

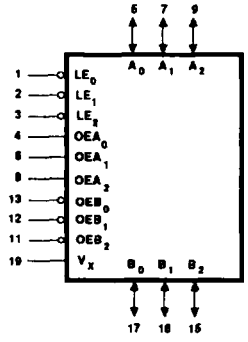
PIN CONFIGURATION



PIN CONFIGURATION PLCC

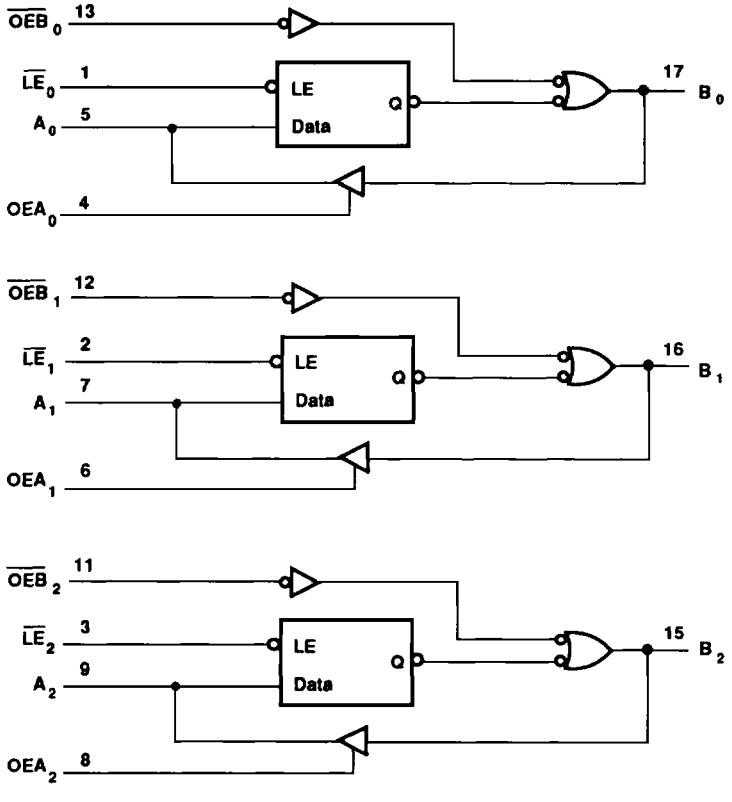


LOGIC SYMBOL



V_{CC} = Pin 20 V_X = Pin 19
GND = Pin 10,14, 18

LOGIC DIAGRAM



V_{CC} = Pin 20 V_X = Pin 19
GND = Pin 10, 14, 18

FUNCTION TABLE

INPUTS					LATCH	OUTPUTS		OPERATING MODE
A_n	B_n*	$\overline{LE}_n$	OEA_n	$\overline{OEB}_n$	STATE	A_n	B_n	
H	X	L	L	L	H	Z	H**	A 3-state, Data from A to B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	H(2)	H	Z(2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	H(2)	L	Z(2)	
–	–	H	H	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	H	Z	Z	B and A 3-state
L	X	L	L	H	L	Z	Z	
X	X	H	L	H	Q_n	Z	Z	
–	H	L	H	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	L	L	Z	
–	H	H	H	H	Q_n	H	Z	
–	L	H	H	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.
H** = Goes to level of pullup voltage.
NOTE = Each latch is independent. The latches may be run in any combination of modes.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	-0.5 to +7.0	V
		$A_0 - A_2$, $B_0 - B_2$	-0.5 to 5.5	
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$A_0 - A_2$	48	mA
		$B_0 - B_2$	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $B_0 - B_2$	2.0			V
		$B_0 - B_2$	1.6			
V_{IL}	Low-level input voltage	Except $B_0 - B_2$			0.8	V
		$B_0 - B_2$			1.43	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$A_0 - A_2$			-3	mA
I_{OL}	Low-level output current	$A_0 - A_2$			24	mA
		$B_0 - B_2$			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High level output current	B_0 - B_2	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_2	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_2[4]	V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
			V_{IH} = MIN	I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_2	V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = 100mA			1.15	V
			V_{IH} = MIN	I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_2	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_2	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} =MAX, V_I = 7.0V				100	µA
		A_0 - A_2, B_0 - B_2	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_2	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		B_0 - B_2	V_{CC} = MAX, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_2	V_{CC} = MAX, V_O =2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_2	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA_n = $\overline{OEB}_n$ = 2.7V, A_0 - A_2= 2.7V, B_0 - B_2 = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA_n = 2.7V, $\overline{OEB}_n$ =A_0 - A_7 = 2.7V, B_0 - B_2 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_2 only	V_{CC} = MAX, B_n = 1.8V, OEA_n = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			55	80	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			45	67	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.8V and V_{IL}=1.3V.

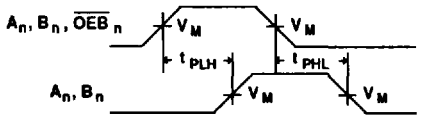
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	8.5 7.5	10.5 9.5	13.0 12.0	8.0 7.5	14.5 12.5	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low $\overline{OEA}_n$ to A_n	Waveform 3,4	8.0 9.0	10.0 11.0	13.0 14.0	7.0 8.0	14.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low $\overline{OEA}_n$ to A_n	Waveform 3,4	1.5 1.5	3.0 3.0	6.0 6.0	1.0 1.0	6.5 6.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	3.0 5.0	4.5 6.5	7.0 9.0	2.5 4.5	8.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_n$ to B_n	Waveform 1	3.5 5.5	5.5 7.5	8.0 10.5	3.0 5.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B_n	Waveform 1	3.0 6.0	5.0 8.0	7.5 10.5	3.0 5.5	8.0 12.0	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	4.0 2.0	4.5 4.5	0.5 0.5	7.0 4.5	ns

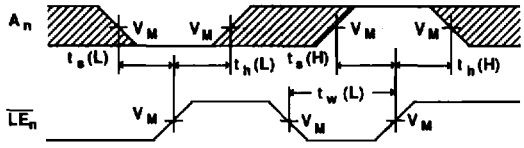
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A_n to $\overline{LE}_n$	Waveform 2	4.0 4.5			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{LE}_n$	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(L)$	$\overline{LE}_n$ Pulse width, Low	Waveform 2	5.5			6.5		ns

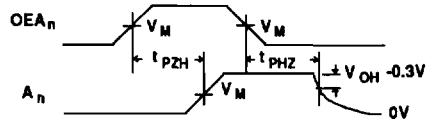
AC WAVEFORMS



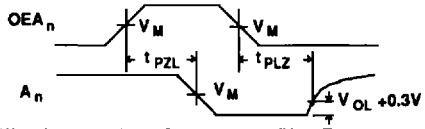
Waveform 1. Propagation Delay For Data To Output And Enable/Disable Time OEB_n To B_n



Waveform 2. Data Setup And Hold Times And LE Pulse Width



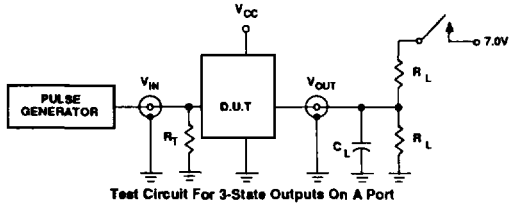
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

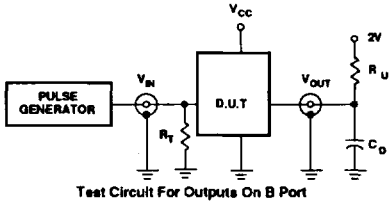
TEST CIRCUIT AND WAVEFORMS



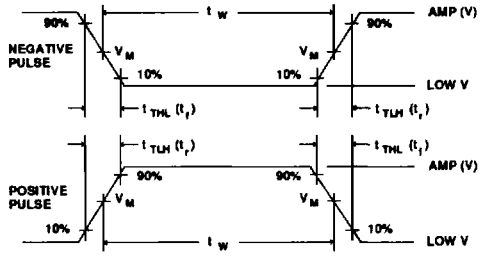
Test Circuit For 3-State Outputs On A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port



V_M = 1.5V

Input Pulse Definition

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.