ADE-203-499 (Z)

HB66C6464BA Series

64k × 64-bit Synchronous Fast Static RAM Module with TAG, Burst Counter and Pipelined Data Output

HITACHI

Preliminary
Rev. 0.0
December 29, 1995

Description

The HB66C6464BA has been developed as an optimized cache memory solution for 8 Bytes processor application. The HB66C6464BA is a 64K x 64 bits fast static RAM module with 32K x 8 Tag, mounted 4 pieces of 1Mbit synchronous SRAM (HM62C3232FP) sealed in LQFP package and a piece of 256Kbit SRAM (UM61256FS equivalent) sealed in SOJ package. An outline of the HB66C6464BA is 160 pins socket type package(Dual read out).

The HB66C6464BA provides common data inputs and outputs. Decoupling capacitors are mounted beside the each SRAM on the its module board.

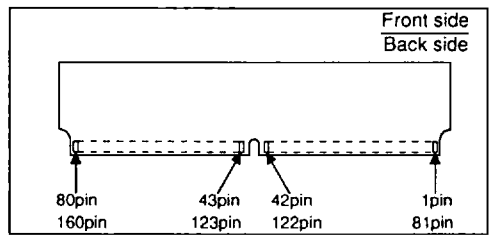
Feature

- 160-pin socket type package (Dual read out)
- Lead pitch : 1.27 mm
- Power supply:
- 3.3V for Data RAM (HM62C3232FP)
- 5.0V for Tag RAM (UM61256FS equivalent)
- Fast clock access time:
- 8/12ns(max)
- Address data pipeline capability
- Internal input registers (address, data, control)
- Internal data output registers
- Internal self-timed write cycle
- /ADSP, /ADSC and /ADV burst control pins (Supports interleaving)
- Asynchronous output enable controlled Three-state outputs
- Individual byte write control and global write
- Common data inputs and data outputs

Ordering Information

Type No.	Access Time	CPU Clock Rate	Package
HB66C6464BA-8	8ns	66MHz	160-pin DIMM Gold Pad
HB66C6464BA-12	12ns	50MHz	

Pin Arrangement



Note: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Pin Arrangement (cont)

Pin No	Signal	Pin No	Signal	Pin No	Signal	Pin No	Signal
1	VSS	41	DQ58	81	VSS	121	DQ59
2	TIO0	42	DQ56	82	TIO1	122	DQ57
3	TIO2	43	VSS	83	TIO7	123	VSS
4	TIO6	44	DQ54	84	TIO5	124	DQ55
5	TIO4	45	DQ52	85	TIO3	125	DQ53
6	NC	46	DQ50	86	NC	126	DQ51
7	VDD3	47	DQ48	87	VDD5	127	DQ49
8	/TWE	48	VSS	88	NC	128	VSS
9	/ADSC	49	DQ46	89	/ADV	129	DQ47
10	VSS	50	DQ44	90	VSS	130	DQ45
11	/CW4	51	DQ42	91	/COE	131	DQ43
12	/CW6	52	VDD3	92	/CW5	132	VDD5
13	/CW0	53	DQ40	93	/CW7	133	DQ41
14	/CW2	54	DQ38	94	/CW1	134	DQ39
15	VDD3	55	DQ36	95	VDD5	135	DQ37
16	/CCE	56	VSS	96	/CW3	136	VSS
17	/GW	57	DQ34	97	NC	137	DQ35
18	/BWE	58	DQ32	98	NC	138	DQ33
19	VSS	59	DQ30	99	VSS	139	DQ31
20	A3	60	VDD3	100	NC	140	VDD5
21	A7	61	DQ28	101	A4	141	DQ29
22	A5	62	DQ26	102	A6	142	DQ27
23	A11	63	DQ24	103	A8	143	DQ25
24	A16	64	VSS	104	A10	144	VSS
25	VDD3	65	DQ22	105	VDD5	145	DQ23
26	A18	66	DQ20	106	A17	146	DQ21
27	VSS	67	DQ18	107	VSS	147	DQ19
28	A12	68	VDD3	108	A9	148	VDD5
29	A13	69	DQ16	109	A14	149	DQ17
30	/ADSP	70	DQ14	110	A15	150	DQ15
31	NC	71	DQ12	111	NC	151	DQ13
32	NC	72	VSS	112	PD0	152	VSS
33	PD1	73	DQ10	113	PD2	153	DQ11
34	PD3	74	DQ8	114	PD4	154	DQ9
35	VSS	75	DQ6	115	VSS	155	DQ7
36	CLK1	76	VDD3	116	CLK0	156	VDD5
37	VSS	77	DQ4	117	VSS	157	DQ5
38	DQ62	78	DQ2	118	DQ63	158	DQ3
39	VDD3	79	DQ0	119	VDD5	159	DQ1
40	DQ60	80	VSS	120	DQ61	160	VSS

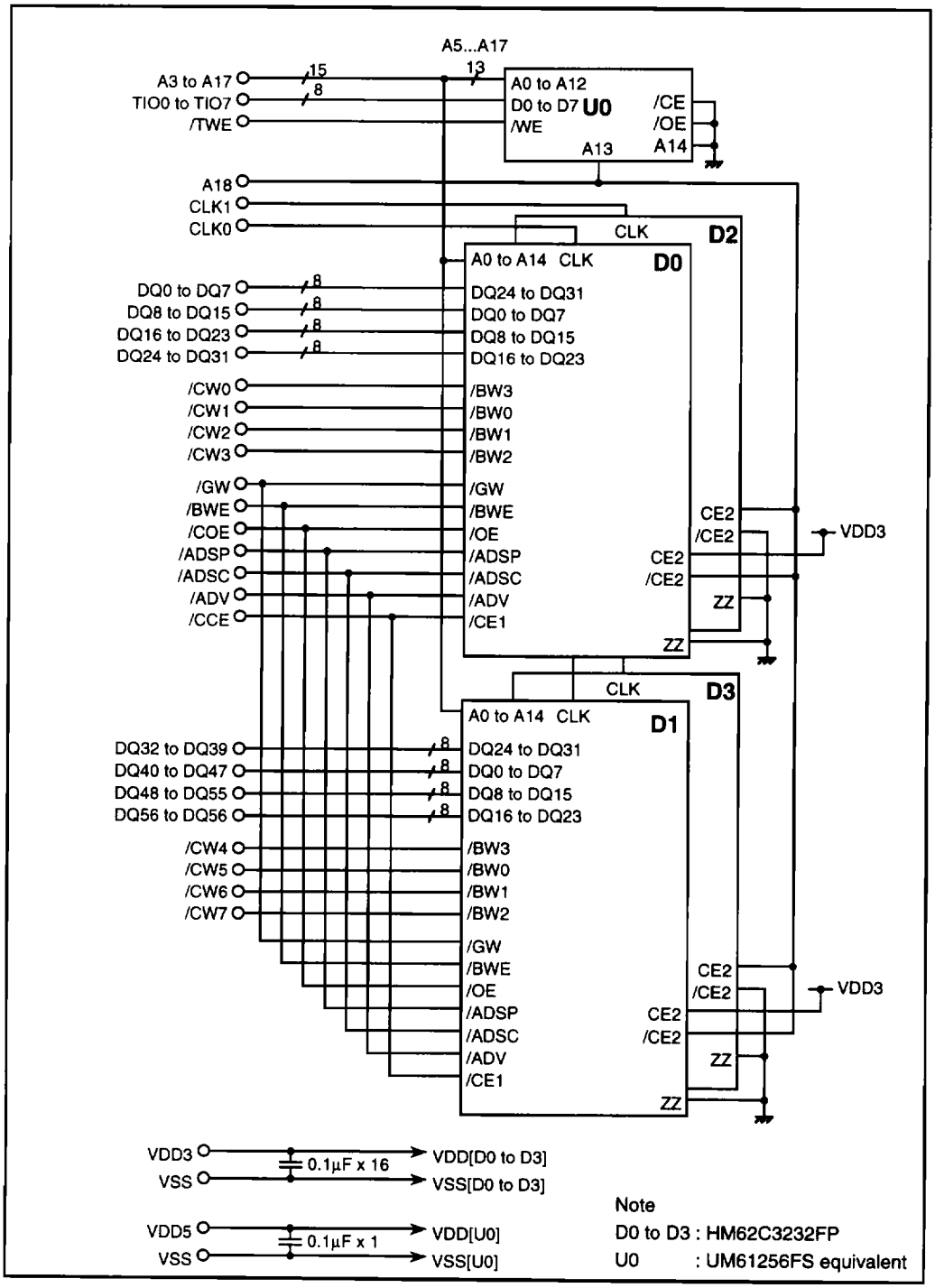
Pin Description

DIMM Pin Number(s)	Symbol	Type	Function
20, 21, 22, 23, 24, 26, 28, 29,101, 102, 103, 104, 106, 108, 109, 110	A3 to A18	Input	Address inputs
11, 12, 13, 14, 92, 93, 94, 96	/CW0, /CW1 /CW2, /CW3 /CW4, /CW5 /CW6, /CW7	Input	Byte write enables /CW0 controls DQ0 - DQ7 /CW1 controls DQ8 - DQ15 /CW2 controls DQ16 - DQ23 /CW3 controls DQ24 - DQ31 /CW4 controls DQ32 - DQ39 /CW5 controls DQ40 - DQ47 /CW6 controls DQ48 - DQ55 /CW7 controls DQ56 - DQ63
17	/GW	Input	Global write
18	/BWE	Input	Byte write enable
36, 116	CLK0, CLK1	Input	Clock
16	/CCE	Input	Cache enable
91	/COE	Input	Cache output enable
89	/ADV	Input	Address advance
30	/ADSP	Input	Address status processor
9	/ADSC	Input	Address status controller
6, 31, 32, 86, 88, 97, 98, 100, 111	NC	–	No connection
38, 40-42, 44-47, 49-51, 53-55, 57-59, 61-63, 65-67, 69-71, 73-75, 77-79, 118, 120-122, 124-127, 129-131, 133-135, 137-139,141-143, 145-147, 149-151,153-155, 157-159	DQ0 to DQ63	Input/Output	Cache data I/O
2-5, 82-85	TIO0 to TIO7	Input/Output	Tag data I/O
8	/TWE	Input	Tag write enable
7, 15, 25, 39, 52, 60, 68, 76	VDD3	Supply	Power supply for cache (+3.3V)
87, 95, 105, 119, 132, 140, 148, 156	VDD5	Supply	Power supply for tag (+5.0V)
1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160	VSS	Supply	Ground

Presence Detect Pin Arrangement

PD4	PD3	PD2	PD1	PD0
VSS	VSS	NC	VSS	VSS

Block Diagram



Synchronous Truth Table

Operation	Address	/CCE	/ADSP	/ADSC	/ADV	/Write	/COE	CLK	DQ
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

Note:
1. H means logic HIGH, L means logic LOW. X means H or L. /Write = L means any one or more byte write enable signals (/CW0 to /CW7) and /BWE are LOW or /GW is LOW.
2. /CW0 enables write to Byte0 (DQ0 to DQ7). /CW1 enables write to Byte1 (DQ8 to DQ15). /CW2 enables write to Byte2 (DQ16 to DQ23). /CW3 enables write to Byte3 (DQ24 to DQ31). /CW4 enables write to Byte4 (DQ32 to DQ39). /CW5 enables write to Byte5 (DQ40 to DQ47). /CW6 enables write to Byte6 (DQ48 to DQ55). /CW7 enables write to Byte7 (DQ56 to DQ63).
3. All inputs except /COE must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation. /COE must be HIGH before the input data required setup time and hold HIGH throughout the input data hold time.
6. /ADSP = LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and /BWE LOW or /GW LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

Asynchronous Truth Table for Cache

Operation	/COE	Cache I/O Status
Cache Read	L	Data out
Cache Read	H	High-Z
Cache Write	X	High-Z, Data in
Deselect	X	High-Z

Note: H means logic HIGH. L means logic LOW. X means H or L.

Asynchronous Truth Table for Tag

Operation	/TWE	Tag I/O Status
Tag Read	H	Data out
Tag Write	L	High-Z, Data in
Deselect	X	High-Z

Note: H means logic HIGH. L means logic LOW. X means H or L.

Partial Truth Table for Cache Write

Operation	/GW	/BWE	/CW0	/CW1 to /CW7
Cache Read	H	H	X	X
Cache Read	H	L	H	H
Cache Write Byte 0	H	L	L	H
Cache Write all bytes	H	L	L	L
Cache Write all bytes	L	X	X	X

Note: H means logic HIGH. L means logic LOW. X means H or L.

Interleaved Burst Sequence Table

Items	A17 to A5	Sequence 1 (A4, A3)	Sequence 2 (A4, A3)	Sequence 3 (A4, A3)	Sequence 4 (A4,A3)
External address	A17 to A5	0 0	0 1	1 0	1 1
1st internal address	A17 to A5	0 1	0 0	1 1	1 0
2nd internal address	A17 to A5	1 0	1 1	0 0	0 1
3rd internal address	A17 to A5	1 1	1 0	0 1	0 0

Note: Each Sequence wraps around to its initial state upon completion.

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit	Note
Supply Voltage		V_{DD3}	-0.5 to +4.6	V	
		V_{DD5}	-0.5 to +7.0	V	
Voltage on any pins relative to V_{SS} (Except V_{DD})	(DQ0 to DQ63)	V_T	-0.5 to V_{DD3}+0.5	V	
	(TIO0 to TIO7, /TWE)	V_T	-0.5 to +7.0	V	1
	(Others)	V_T	-0.5 to +6.0	V	
Power dissipation		P_T	3.0	W	
Operating temperature		Topr	0 to +70	°C	
Storage temperature range (with bias)		Tstg (bias)	-10 to +85	°C	
Storage temperature range		Tstg	-55 to +125	°C	

Note: 1. VT must not exceed VDD5 +0.5V.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Note
Supply voltage (Operating voltage range)		V_{DD3}	3.1	3.6	V	
		V_{DD5}	4.5	5.5	V	
Supply voltage to V_{SS}		V_{SS}	0.0	0.0	V	
Input high voltage	(DQ0 to DQ63)	V_{IH}	2.0	V_{DD3}+0.3	V	
	(TIO0 to TIO7, /TWE)	V_{IH}	2.2	V_{DD5}+0.5	V	
	(Others)	V_{IH}	2.2	5.5	V	
Input low voltage	(TIO0 to TIO7, /TWE)	V_{IL}	-0.5	0.8	V	1
	(Others)	V_{IL}	-0.3	0.8	V	2

Notes: 1. -1.5V for undershoot pulse width ≤ 10ns, once per cycle.
2. -2.0V for undershoot pulse width ≤ tcyc min/2.

DC Characteristics

(Ta = 0 to +70°C, V_{DD3} = 3.3V +0.3V/ -0.2V, V_{DD5} = 5.0V ± 5%, unless otherwise noted)

Parameter		Symbol	Min	Max	Unit	Test conditions
Input leakage current	(TIO0 to TIO7, /TWE)	I_{LI}	—	±5.0	µA	V_{IN} = V_{SS} to V_{DD}, V_{IN}<V_{DD}+0.5V
	(DQ0 to DQ63)	I_{LI}	—	±2.0	µA	V_{IN} = V_{SS} to V_{DD}
	(Others)	I_{LI}	—	±5.0	µA	V_{IN} = V_{SS} to 5.5V, V_{IN}<V_{DD}+0.5V
Output leakage current	(TIO0 to TIO7, /TWE)	I_{LO}	—	±5.0	µA	/COE, /ECS1= V_{IH}, Vout = V_{SS} to V_{DD}, V_{OUT}<V_{DD}+0.5V
	(DQ0 to DQ63)	I_{LO}	—	±2.0	µA	/COE, /ECS1= V_{IH}, Vout = V_{SS} to V_{DD}
	(Others)	I_{LO}	—	±5.0	µA	/COE, /ECS1= V_{IH}, Vout = V_{SS} to V_{DD}, V_{OUT}<V_{DD}+0.5V
Supply current	(V_{DD3})	I_{DD}	—	330	mA	A bank selected
	(V_{DD5})	I_{DD}	—	170	mA	Iout = 0mA, all inputs = V_{IH} or V_{IL} cycle time = t_{cyc} min.
Standby current	(V_{DD3})	I_{SB}	—	100	mA	Banks deselected
	(V_{DD5})	I_{SB}	—	60	mA	all inputs = fixed and all inputs ≥ V_{DD} - 0.2V or ≤ 0.2V cycle time = t_{cyc} min.
Output low voltage		V_{OL}	—	0.4	V	I_{OL} = 8mA
Output high voltage		V_{OH}	2.4	—	V	I_{OH} = -4mA

Capacitance (Ta = 25°C, f = 1.0MHz)

Parameter		Symbol	Max.	Unit
Input capacitance	(Address)	C_{IN}	40	pF
	(/ADSP, /ADSC,/CCE, /COE, /ADV, CLK, /LBO)	C_{IN}	40	pF
	(CW0 to CW7)	C_{IN}	20	pF
	(/TWE)	C_{IN}	15	pF
Input/Output capacitance	(DQ0 to DQ63)	$C_{I/O}$	25	pF
	(TIO0 to TIO7)	$C_{I/O}$	15	pF

Note: This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = 0 to +70°C, V_{DD3} = 3.3V+0.3V/-0.2V, V_{DD5} = 5.0V±5%, V_{SS} = 0V, unless otherwise noted)

Cache Cycle

Parameter	Symbol standard	Symbol alternate	HB66C6464BA -8 Min	-8 Max	-12 Min	-12 Max	Unit	Notes
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	ns	
Clock Access Time	t_{KHQV}	t_{ACK}	—	8	—	12	ns	
Output Enable to Output valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	4
Clock High to Output Active	t_{KHQX1}	t_{CLZ}	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{COH}	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQZ}	t_{OLZ}	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	ns	1
Clock High to Q High-Z	t_{KHQZ}	t_{CHZ}	—	6	—	6	ns	1
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	6	—	ns	
Setup Times :			2.5	—	3.0	—	ns	2, 3
Address	t_{AVKH}	t_{SA}						
Address Status	t_{ADSVKH}	t_{SADS}						
Input Data	t_{DVKH}	t_{SD}						
Write	t_{WVKH}	t_{SW}						
Address Advance	t_{ADVVKH}	t_{SADV}						
Chip Enable	t_{EVKH}	t_{SCE}						
Hold Times :			0.5	—	0.5	—	ns	2, 3
Address	t_{KHAX}	t_{HA}						
Address Status	t_{KHADSX}	t_{HADS}						
Input Data	t_{KHDX}	t_{HD}						
Write	t_{KHWX}	t_{HW}						
Address Advance	t_{KHADVX}	t_{HADV}						
Chip Enable	t_{KHEX}	t_{HCE}						

Notes: 1. Transition is measured ±200mV from steady-state voltage with load of Figure B. This parameter is sampled.
2. A READ cycle is defined by byte write enables all HIGH or /ADSP LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and /ADSP HIGH for the required setup and hold times.
3. This is a synchronous device. All address must meet the specified setup and hold times for all rising edges of CLK when either /ADSP or /ADSC is LOW and chip enabled. All other Synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock(CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK(when either /ADSP or /ADSC is LOW) to remain enabled.
4. /COE is a "H or L" when a byte write enable is sampled LOW.

Test Conditions

- Input Timing Measurement Reference level: 1.4V
- Input Pulse Levels: 0 to 2.8V
- Input Rise and Fall Time: 2ns
- Output Timing Reference Level: 1.4V
- Output Load: See Fig. A unless otherwise noted

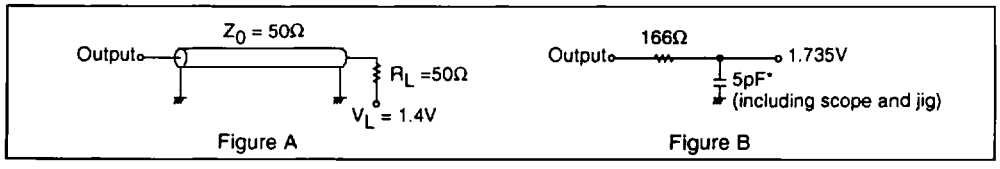


Figure A Figure B

AC Characteristics (cont)

(Ta = 0 to +70°C, V_{DD3} = 3.3V+0.3V/-0.2V, V_{DD5} = 5.0V±5%, V_{SS} = 0V, unless otherwise noted)

Tag Cycle

		HB66C6464BA					
		-8		-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	t_{RC}	15	—	20	—	ns	
Address Access Time	t_{AA}	—	15	—	20	ns	
Output Hold from Address Change	t_{OH}	3	—	3	—	ns	
Write Cycle Time	t_{WC}	15	—	20	—	ns	
Address Valid to End-of-Write	t_{AW}	14	—	15	—	ns	
Write Pulse Width	t_{WP}	14	—	15	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data to Write Time Overlap	t_{DW}	10	—	10	—	ns	
Data Hold from Write Time	t_{DH}	0	—	0	—	ns	

Test Conditions

- Input Timing Measurement Reference Level: 1.5V
- Input Pulse Levels: 0 to 3.0V
- Input Rise and Fall Time: 5ns
- Output Timing Reference Level: 1.5V
- Output Load: See Figures A and B

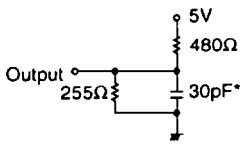


Figure A
Output Load

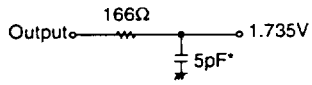
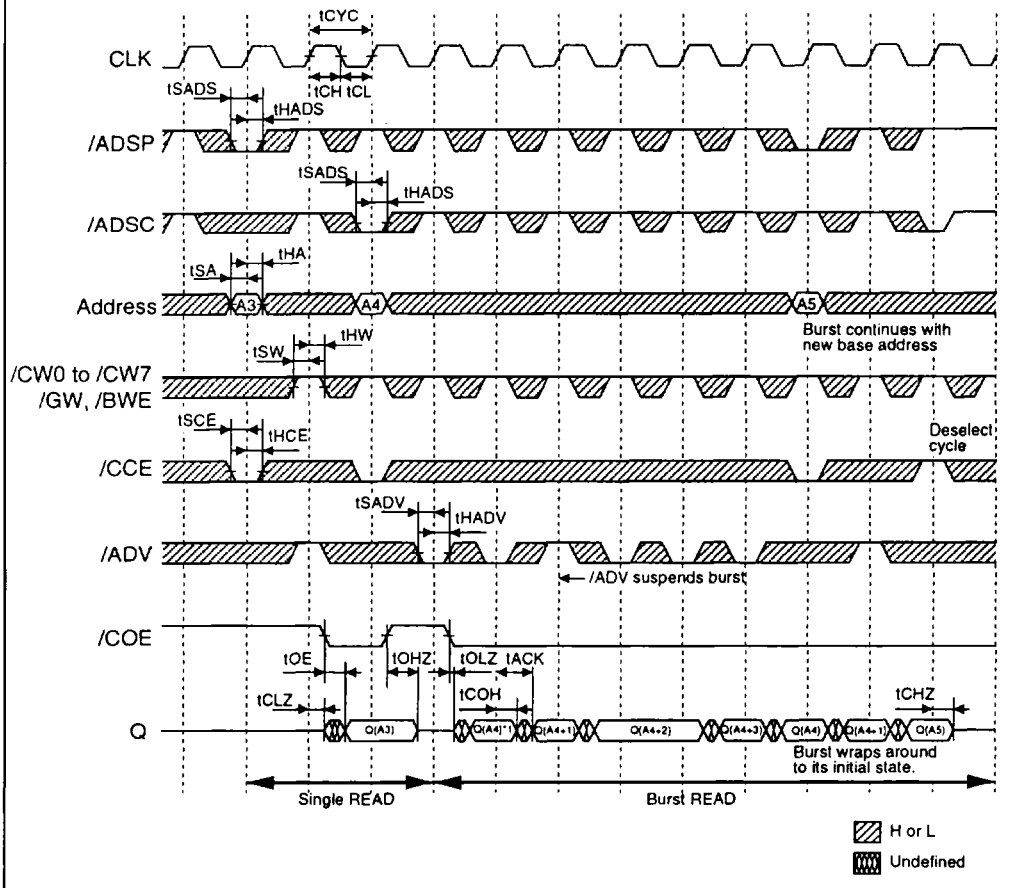


Figure B
Output Load for tLZC,tHZC

*including scope and jig

Timing Waveforms

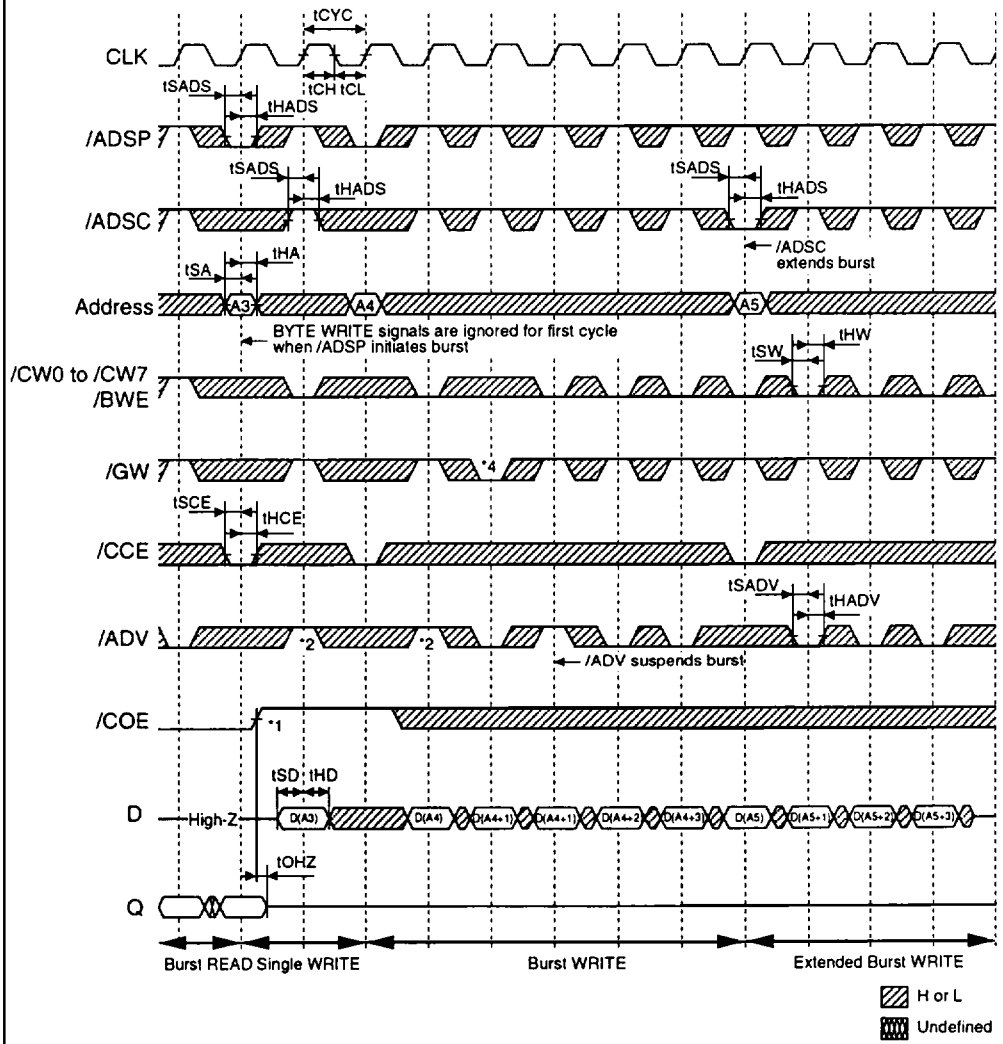
Example of Cache Read Timing



Notes: 1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from next internal burst address following A4.

Timing Waveforms (cont)

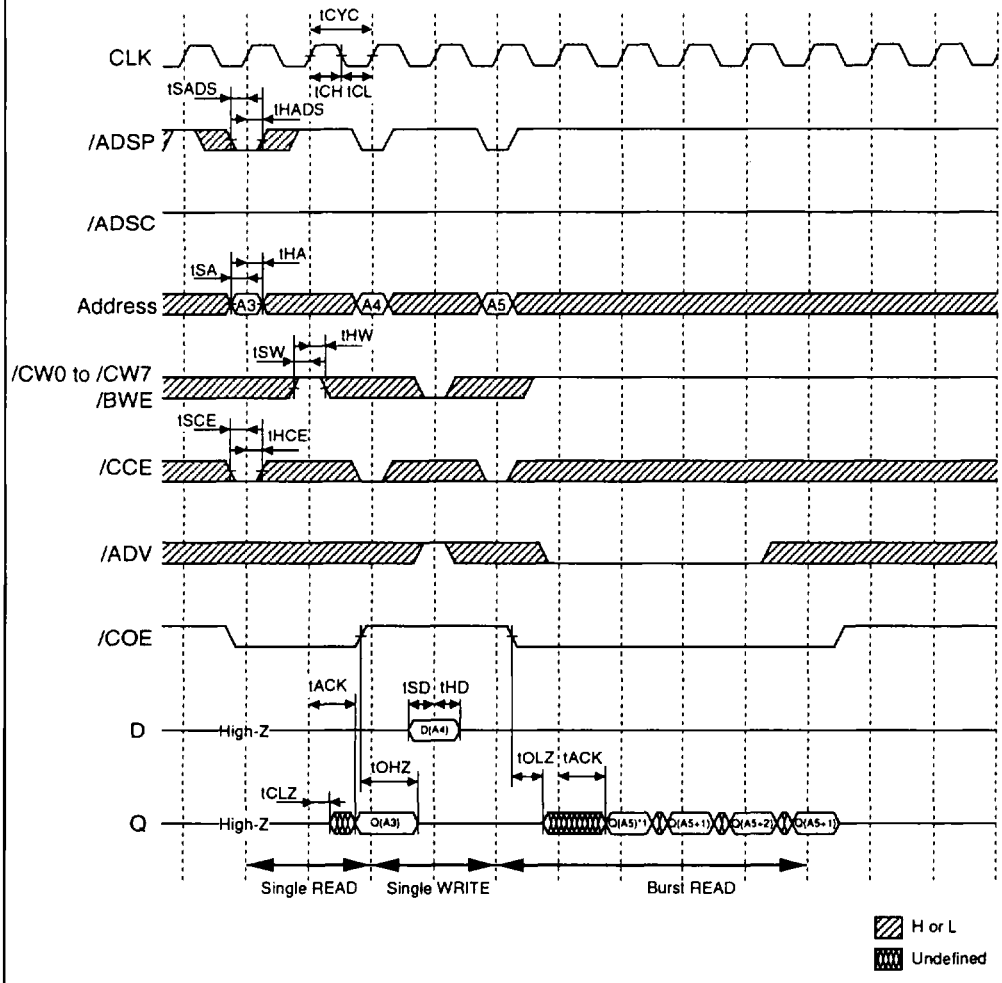
Example of Cache Write Timing



Notes: 1. /COE must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
2. /ADV must be HIGH to permit a WRITE to the loaded address.
3. Full width WRITE can be initiated by /GW is LOW or /GW is HIGH and /BWE, /CW0 to /CW7 are LOW.

Timing Waveforms (cont)

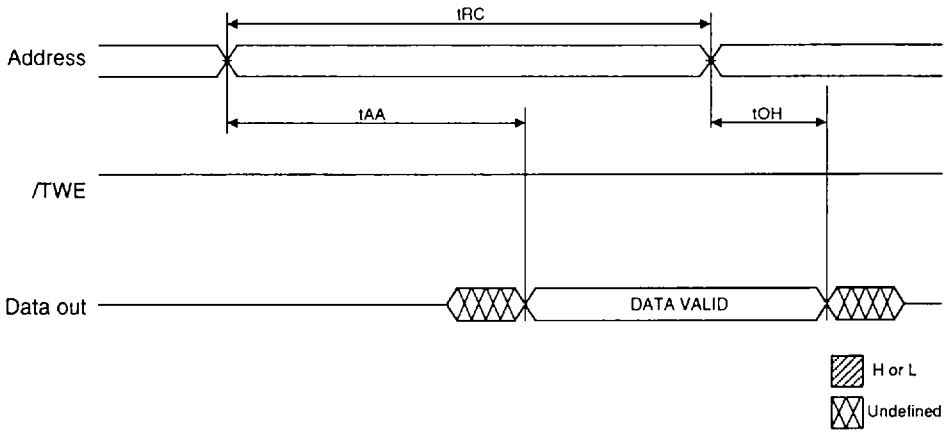
Example of Cache Read/Write Timing



Notes: 1. Q(A5) refers to output from address A5. Q(A5+1) refers to output from next internal burst address following A5.
2. /GW is HIGH.

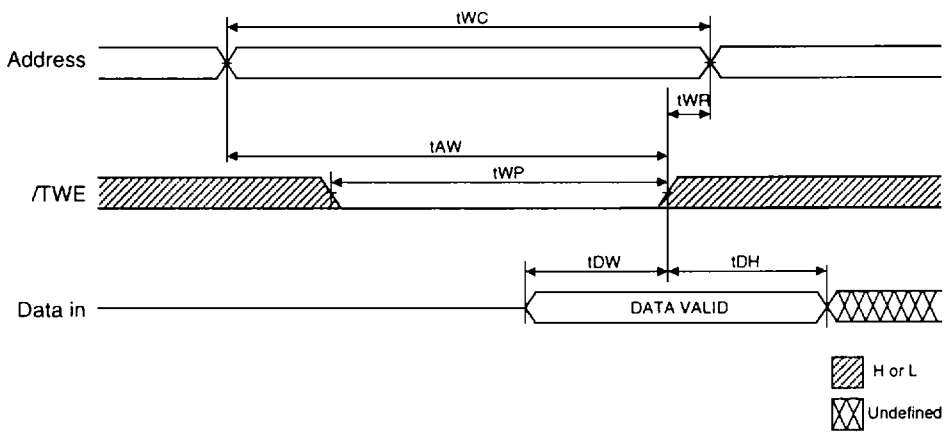
Timing Waveforms (cont)

Example of Tag Read Timing



Note: 1. /TWE is HIGH for Read cycle.

Example of Tag Write Timing



Notes: 1. /TWE must be inactive during all address transitions.
2. A Write occurs during a LOW /TWE.
3. t_{WR} is measured from the /TWE going HIGH to the end of the write cycle.