

MAXIM

12-Bit, 20Mps, TTL-Output ADC

MAX1171

General Description

The MAX1171 analog-to-digital converter (ADC) is a 12-bit monolithic ADC capable of sample rates greater than 20Mps. An on-board input buffer and track/hold function ensure excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes development problems.

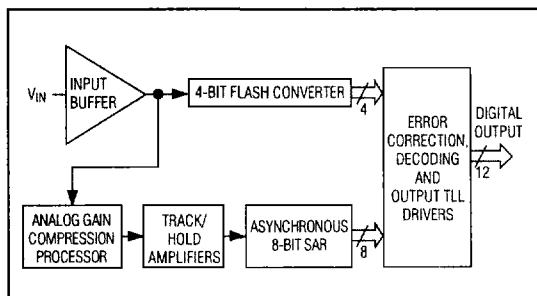
Logic inputs and outputs are TTL compatible. An over-range output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is a very low 1.1W with power-supply voltages of +5.0V and -5.2V. The MAX1171 also provides a wide input voltage range of $\pm 2.0V$.

The MAX1171 is available in a 32-lead ceramic side-brazed package and a 44-lead surface-mount CERQUAD package.

Applications

Radar Receivers
Professional Video
Instrumentation
Imaging
Digital Communications
Digital Spectrum Analyzers

Functional Diagram



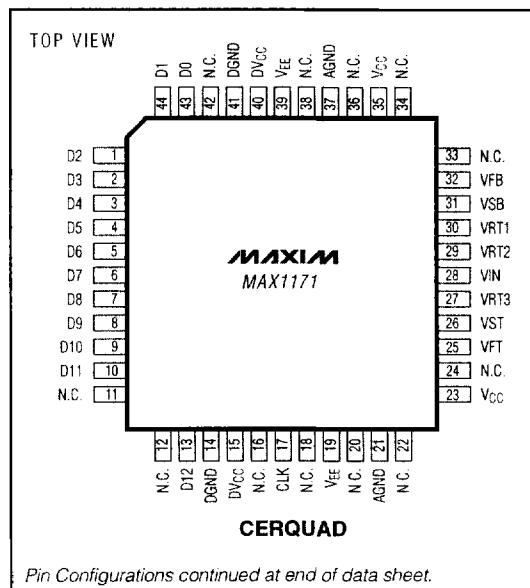
Features

- ◆ Monolithic, 12-Bit, 20Mps Converter
- ◆ On-Chip Track/Hold
- ◆ $\pm 2.0V$ Analog Input Range
- ◆ 66dB SNR at 1MHz Input
- ◆ Low Power: 1.1W
- ◆ 5pF Input Capacitance
- ◆ TTL-Compatible Outputs

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1171CDJ	0°C to +70°C	32 Ceramic SB
MAX1171CBH	0°C to +70°C	44 CERQUAD

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

VCC	+6V	Digital Outputs	0mA to -30mA
VEE	-6V	Operating Temperature Range	0°C to +70°C
Analog Input	$V_{FB} \leq V_{IN} \leq V_{FT}$	Junction Temperature (T _j)	+175°C
VFB, VFT	-3.0V, +3.0V	Storage Temperature Range	-65°C to +150°C
Reference Ladder Current	12mA	Lead Temperature (soldering, 10sec)	+300°C
CLK IN	VCC		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +5.0V, VEE = -5.2V, DVCC = +5.0V, VIN = ±2.0V, VSB = -2.0V, VST = +2.0V, fCLK = 20MHz, 50% clock duty cycle, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			12			Bits
DC ACCURACY (TA = +25°C)						
Integral Nonlinearity	± full scale	IV		±2.0		LSB
Differential Nonlinearity	250kHz sample rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
ANALOG INPUT						
Input Voltage Range		VI		±2.0		V
Input Bias Current	TA = +25°C	I		30	60	µA
Input Resistance	VIN = 0V, TA = +25°C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3dB small signal	V		120		MHz
Positive Full-Scale Error		V		±5.0		LSB
Negative Full-Scale Error		V		±5.0		LSB
REFERENCE INPUT						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
TIMING CHARACTERISTICS						
Maximum Conversion Rate		VI	20			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	TA = +25°C	V		14	18	ns
Aperture Delay Time	TA = +25°C	V		1		ns
Aperture Jitter Time	TA = +25°C	V		5		ps-RMS

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, V_{SB} = -2.0V, V_{ST} = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Effective Number of Bits	f _{IN} = 500kHz			10.2		Bits
	f _{IN} = 1MHz			10.0		
	f _{IN} = 3.58MHz			9.5		
Signal-to-Noise Ratio (without Harmonics)	f _{IN} = 500kHz	T _A = +25°C	I	64	67	dB
		T _A = T _{MIN} to T _{MAX}	IV	58	61	
	f _{IN} = 1MHz	T _A = +25°C	I	64	66	
		T _A = T _{MIN} to T _{MAX}	IV	58	60	
	f _{IN} = 3.58MHz	T _A = +25°C	I	62	64	
		T _A = T _{MIN} to T _{MAX}	IV	58	60	
Harmonic Distortion	f _{IN} = 500kHz	T _A = +25°C	I	63	66	dB
		T _A = T _{MIN} to T _{MAX}	IV	59	62	
	f _{IN} = 1MHz	T _A = +25°C	I	63	65	
		T _A = T _{MIN} to T _{MAX}	IV	59	61	
	f _{IN} = 3.58MHz	T _A = +25°C	I	59	61	
		T _A = T _{MIN} to T _{MAX}	IV	57	59	
Signal-to-Noise and Distortion	f _{IN} = 500kHz	T _A = +25°C	I	60	63	dB
		T _A = T _{MIN} to T _{MAX}	IV	55	58	
	f _{IN} = 1MHz	T _A = +25°C	I	60	62	
		T _A = T _{MIN} to T _{MAX}	IV	55	57	
	f _{IN} = 3.58MHz	T _A = +25°C	I	57	59	
		T _A = T _{MIN} to T _{MAX}	IV	54	56	
Spurious-Free Dynamic Range	f _{IN} = 1MHz, T _A = +25°C	V		74		dBc
Differential Phase	f _{IN} = 3.58MHz and 4.35MHz, T _A = +25°C	V		0.2		Degrees
Differential Gain	f _{IN} = 3.58MHz and 4.35MHz, T _A = +25°C	V		0.7		%
DIGITAL INPUTS						
Logic "1" Voltage		V	2.4		4.0	V
Logic "0" Voltage		V			0.8	V
Maximum Input Current Low	T _A = +25°C	I	0	5	20	μA
Maximum Input Current High	T _A = +25°C	I	0	5	20	μA
Pulse Width Low (CLK)		IV	20			ns
Pulse Width High (CLK)		IV	20		300	ns
DIGITAL OUTPUTS						
Logic "1" Voltage	T _A = +25°C	I	2.4			V
Logic "0" Voltage	T _A = +25°C	I			0.6	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +5.0V$, $V_{EE} = -5.2V$, $DV_{CC} = +5.0V$, $V_{IN} = \pm 2.0V$, $V_{SB} = -2.0V$, $V_{ST} = +2.0V$, $f_{CLK} = 20MHz$, 50% clock duty cycle, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
POWER-SUPPLY REQUIREMENTS						
Voltages	V_{CC}	IV	4.75	5.0	5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	
Currents	I_{CC} , $T_A = +25^\circ C$	I		135	150	mA
	$D I_{CC}$, $T_A = T_{MIN}$ to T_{MAX}	IV		40	55	
	$-I_{EE}$, $T_A = +25^\circ C$	I		45	70	
Power Dissipation		VI		1.1	1.3	W
Power-Supply Rejection	$5V \pm 0.25V$, $-5.2V \pm 0.25V$	V		1.0		LSB

Note 1: Typical thermal impedances (unsoldered, in free air):

32 Ceramic SB: $\theta_{JA} = 50^\circ C/W$

44 CERQUAD: $\theta_{JA} = 78^\circ C/W$, θ_{JA} at 1m/s airflow = $58^\circ C/W$, $\theta_{JC} = 3.3^\circ C/W$

Use forced-air cooling or heatsinking to maintain $T_j \leq 150^\circ C$.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL TEST PROCEDURE

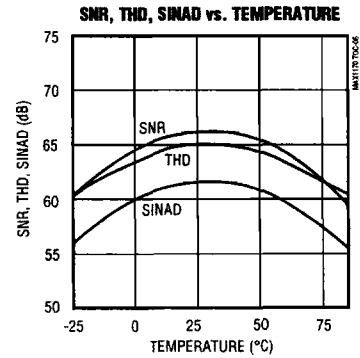
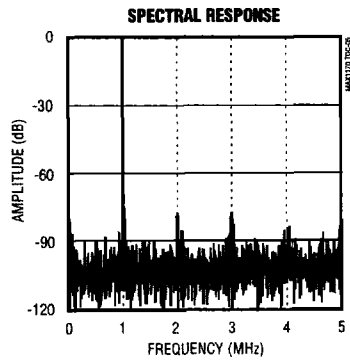
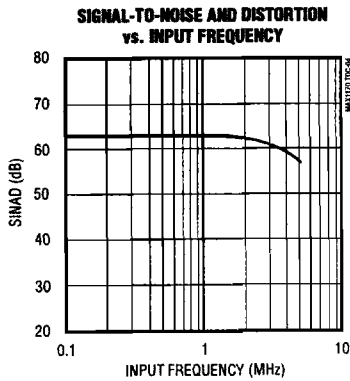
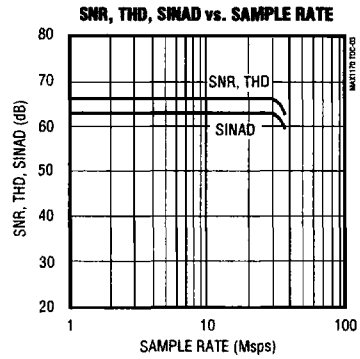
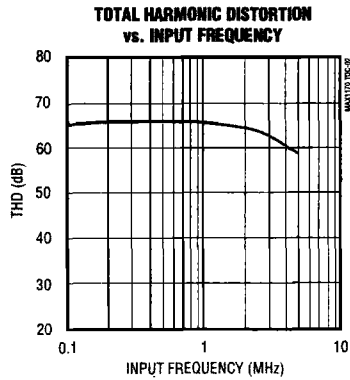
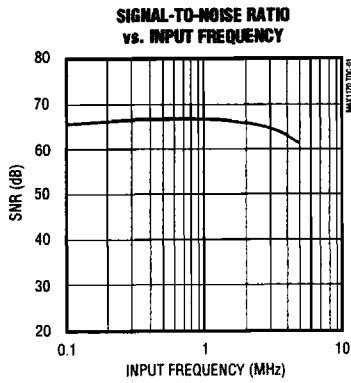
I	100% production tested at the specified temperature.
II	100% production tested at $T_A = +25^\circ C$, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at $T_A = +25^\circ C$. Parameter is guaranteed over specified temperature range.

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Typical Operating Characteristics

($f_s = 20\text{Mps}$, $f_{IN} = 1\text{MHz}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

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Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 15	14, 41	DGND	Digital Ground
2-13	43, 44, 1-10	D0-D11	TTL Outputs (D0 = LSB)
14	13	D12	TTL Output Overage Bit
16, 32	15, 40	DVCC	Digital +5.0V Supply (TTL Outputs)
17	17	CLK	TLL Clock Input
18, 31	19, 39	VEE	-5.2V Supply
19, 30	21, 37	AGND	Analog Ground
20, 29	23, 35	VCC	+5.0V Supply
21	25	VFT	Force for Top of Reference Ladder
22	26	VST	Sense for Top of Reference Ladder
23	27	VRT3	Voltage Reference Tap 3
24	28	VIN	Analog Input, 2.0V typical
25	29	VRT2	Voltage Reference Tap 2
26	30	VRT1	Voltage Reference Tap 1
27	31	VSB	Sense for Bottom of Reference Ladder
28	32	VFB	Force for Bottom of Reference Ladder
—	11, 12, 16, 18, 20, 22, 24, 33, 34, 36, 38, 42	N.C.	No Connection

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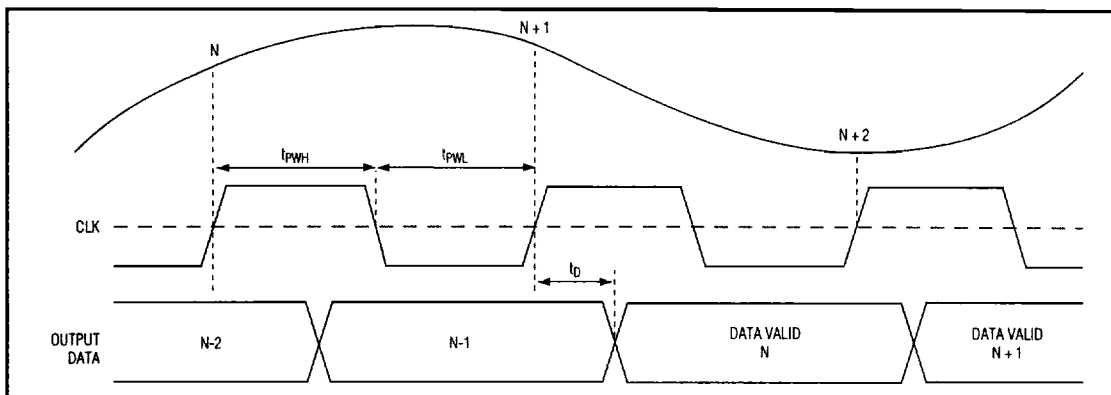


Figure 1a. Timing Diagram

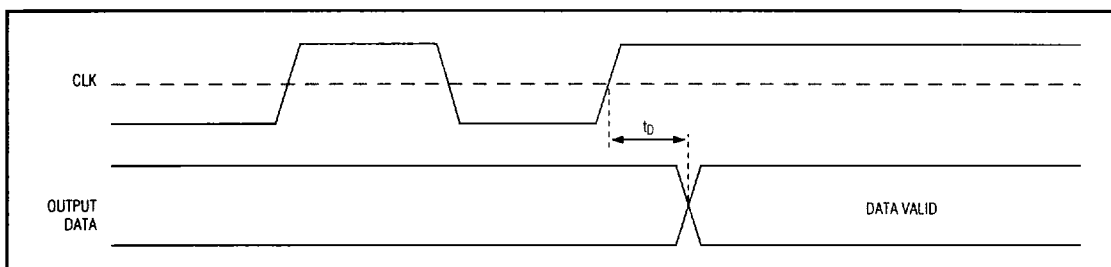


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_D	CLK to Data Valid Prop Delay		14	18	ns
t_{PWH}	CLK High Pulse Width	20		300	ns
t_{PWL}	CLK Low Pulse Width	20			ns

Detailed Description

The MAX1171 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1171 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1171 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog VCC and digital DVCC. A ferrite bead in series with each supply line reduces the transient noise injected into the analog VCC. These beads should be connected as close to the device as possible. The connection between the beads and the MAX1171 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1 μ F for VEE and VCC, and 0.01 μ F for DVCC (chip capacitors are preferred).

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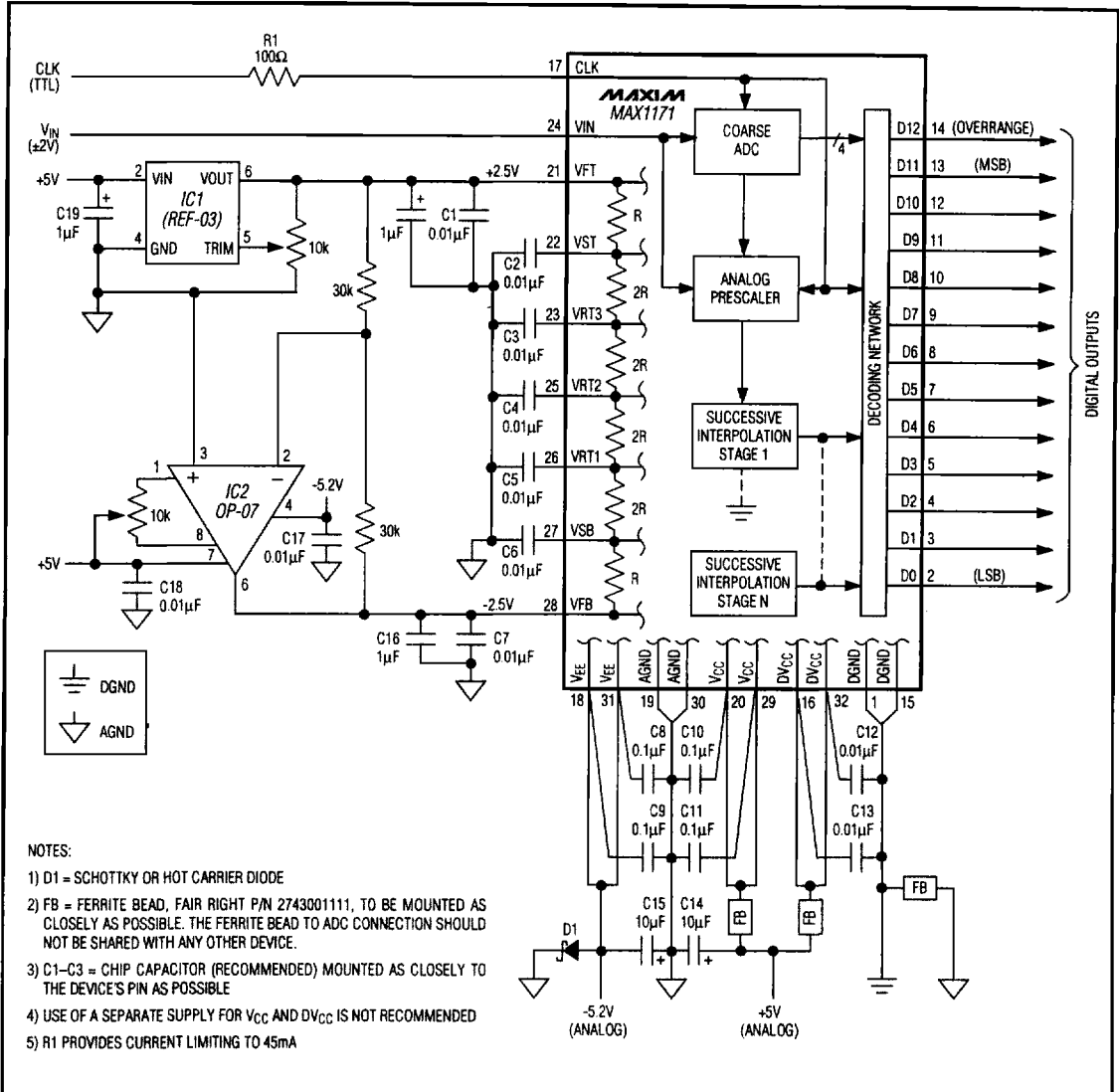


Figure 2. Typical Interface Circuit

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AGND and DGND are the two grounds available on the MAX1171. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DVCC return path (40mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and VEE is required. The use of separate power supplies between VCC and DVCC is not recommended due to potential power-supply sequencing latchup conditions. Use of the recommended interface circuit shown in Figure 2 will provide optimum device performance for the MAX1171.

Voltage Reference

The MAX1171 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5V typical), V_{FB} (-2.5V typical) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800Ω. The +2.5V voltage source for reference V_{FT} must be current limited to 20mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3.

In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0V), V_{RT2} is the mid-point of the ladder (0.0V typical), and V_{SB} is the sense for the bottom of the reference ladder (-2.0V). V_{RT1} and V_{RT3} are quarter-point ladder taps (+1.0V and -1.0V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full-scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5V and -2.5V typical, respectively). V_{ST} and V_{SB} can be used to monitor the actual full-scale input voltage of the device. V_{RT1}, V_{RT2}, and V_{RT3} should not be driven to the expected ideal values, as is commonly done with standard flash converters. A decoupling capacitor of 0.01μF connected to AGND from each tap is recommended to minimize high-frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input

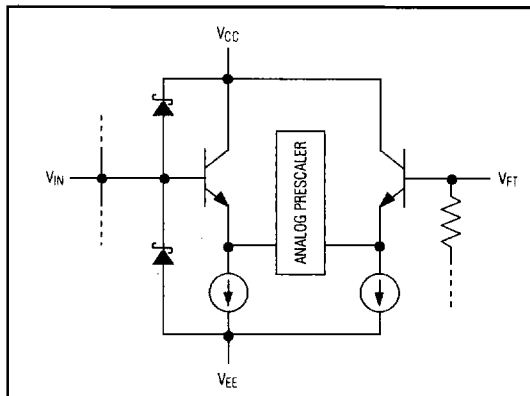


Figure 3. Analog Equivalent Input Circuit

range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the MAX1171 is laser trimmed to optimize performance with ±2.5V references, its accuracy will degrade if operated beyond a ±2% range.

An example of a recommended reference driver circuit is shown in Figure 2. IC1 is REF-03, the +2.5V reference with a tolerance of 0.6% or ±0.015V. The 10kΩ potentiometer supports an adjustable range of 150mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. Adjust R1 and R4 such that V_{ST} and V_{SB} are exactly +2.0V and -2.0V, respectively.

The following errors are defined:

$$\begin{aligned} +FS \text{ error} &= \text{top of ladder offset voltage} \\ &= \Delta(+FS - V_{ST}) \\ -FS \text{ error} &= \text{bottom of ladder offset voltage} \\ &= \Delta(-FS - V_{SB}) \end{aligned}$$

Where the +FS (full scale) input voltage is defined as the output 1LSB above the transition of 1–10 and 1–11, and the -FS input voltage is defined as the output 1LSB below the transition of 0–00 and 0–01.

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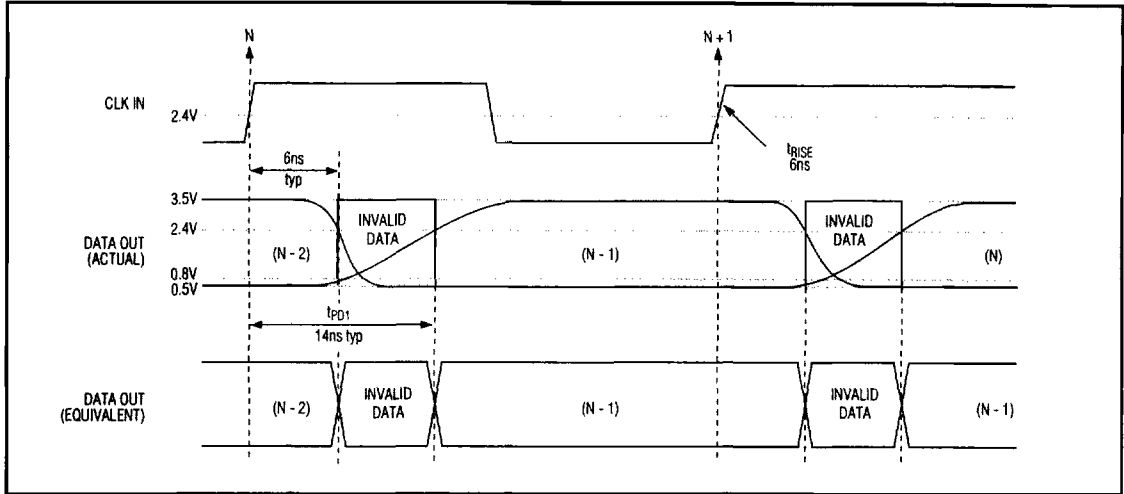


Figure 4. Digital Output Characteristics

Analog Input

V_{IN} is the analog input. The full-scale input range will be 80% of the reference voltage or $\pm 2V$ with V_{FB} = -2.5V and V_{FT} = +2.5V.

The drive requirements for the analog inputs are minimal compared to those of conventional flash converters, due to the MAX1171's extremely low 5pF input capacitance and high 300k Ω input impedance. For example, for an input signal of $\pm 2V$ p-p with an input frequency of 10MHz, the peak output current required for the driving circuit is only 628 μ A.

Clock Input

The MAX1171 is driven from a single-ended TTL input (CLK). For optimal noise performance, the clock input slew rate should be a minimum of 6ns. Because of this, the use of fast logic is recommended. The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40% to 60%. However, in any case, the clock pulse width (t_{PWH}) must be kept at 300ns maximum to ensure proper operation of the internal track/hold amplifier (Figure 1a). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} \leq 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100 Ω resistor (R1, Figure 2) in series to current limit to approximately 45mA.

Digital Outputs

The format of the output data (D0-D11) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one clock cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise times and fall times are not symmetrical. The rise time's typical propagation delay is 14ns, and the typical fall time is 6ns (Figure 4). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
> +2.0V + 1/2LSB	1	11 1111 1111
+2.0V - 1LSB	0	11 1111 1110
0.0V	0	00 0000 0000
-2.0V + 1LSB	0	00 0000 0000
< -2.0V	0	00 0000 0000

(\emptyset indicates the flickering bit between logic 0 and 1).

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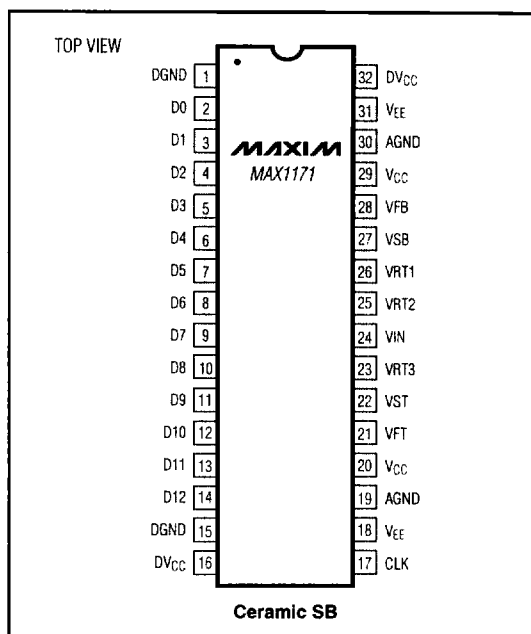
Overrange Output

The overrange output (D12) is an indication that the analog input signal has exceeded the full-scale input voltage by 1LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the MAX1171 in higher resolution systems.

Evaluation Board

The MAX1170 evaluation kit (EV kit) is available to aid designers in demonstrating the full performance of the MAX1171 (or of the MAX1170/MAX1172). This board includes a reference circuit, clock driver circuit, output data latches, and on-board reconstruction of the digital data. A separate EV kit manual describing the operation of this board is available. Contact the factory for price and availability.

Pin Configurations (continued)



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