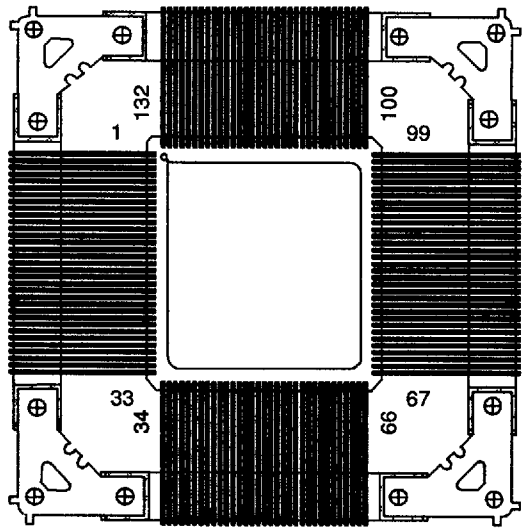
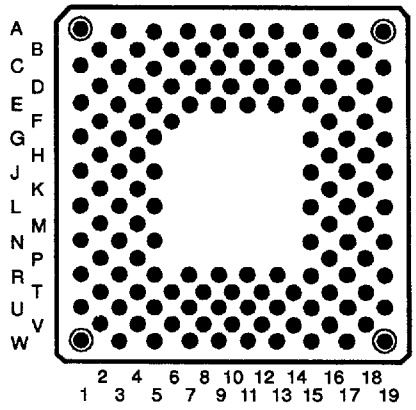
- Military Operating Temperature Range:
  – 55°C to 125°C
- Processed to MIL-STD-883, Class B
- Fast Instruction Cycle Times of 40 ns and 50 ns
- Source-Code Compatible With All 'C1x and 'C2x Devices
- RAM-Based Operation
  - 9K × 16-Bit Single-Cycle On-Chip Program/Data RAM
  - 1056 × 16-Bit Dual-Access On-Chip Data RAM
- 2K × 16-Bit On-Chip Boot ROM
- 224K × 16-Bit Maximum Addressable External Memory Space (64K Program, 64K Data, 64K I/O, and 32K Global)
- 32-Bit Arithmetic Logic Unit (ALU)
  - 32-bit Accumulator (ACC)
  - 32-Bit Accumulator Buffer (ACCB)
- 16-Bit Parallel Logic Unit (PLU)
- 16 × 16-Bit Multiplier, 32-Bit Product
- 11 Context-Switch Registers
- 2 Buffers for Circular Addressing
- Full-Duplex Synchronous Serial Port
- Time-Division Multiplexed Serial Port (TDM)
- Timer With Control and Counter Registers
- 16 Software Programmable Wait-State Generators
- Divide-by-One Clock Option
- JTAG Boundary Scan Logic (IEEE 1149.1)
- Operations Are Fully Static
- Texas Instruments EPIC™ 0.8-μm CMOS Technology
- Packaging
  - 141-Pin Ceramic Grid Array (GFA Suffix)
  - 132-Lead Ceramic Quad Flat Package (HFG Suffix)

HFG PACKAGE
(TOP VIEW)



GFA PACKAGE
(TOP VIEW)



description

The SMJ320C50A digital signal processor (DSP) is a high-performance, 16-bit, fixed-point processor manufactured in 0.8-μm double-level metal CMOS technology. The SMJ320C50A is the first DSP from TI designed as a fully static device. Full-static CMOS design contributes to low power consumption while maintaining high performance, making it ideal for applications such as battery-operated communications systems, satellite systems, and advanced control algorithms.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

A number of enhancements to the basic SMJ320C2x architecture give the 'C50A a minimum 2x performance over the previous generation. A four-deep instruction pipeline, incorporating delayed branching, delayed call to subroutine, and delayed return from subroutine, allows the 'C50A to perform instructions in fewer cycles. The addition of a parallel logic unit (PLU) gives the 'C50A a method of manipulating bits in data memory without using the accumulator and ALU. The 'C50A has additional shifting and scaling capability for proper alignment of multiplicands or storage of values to data memory.

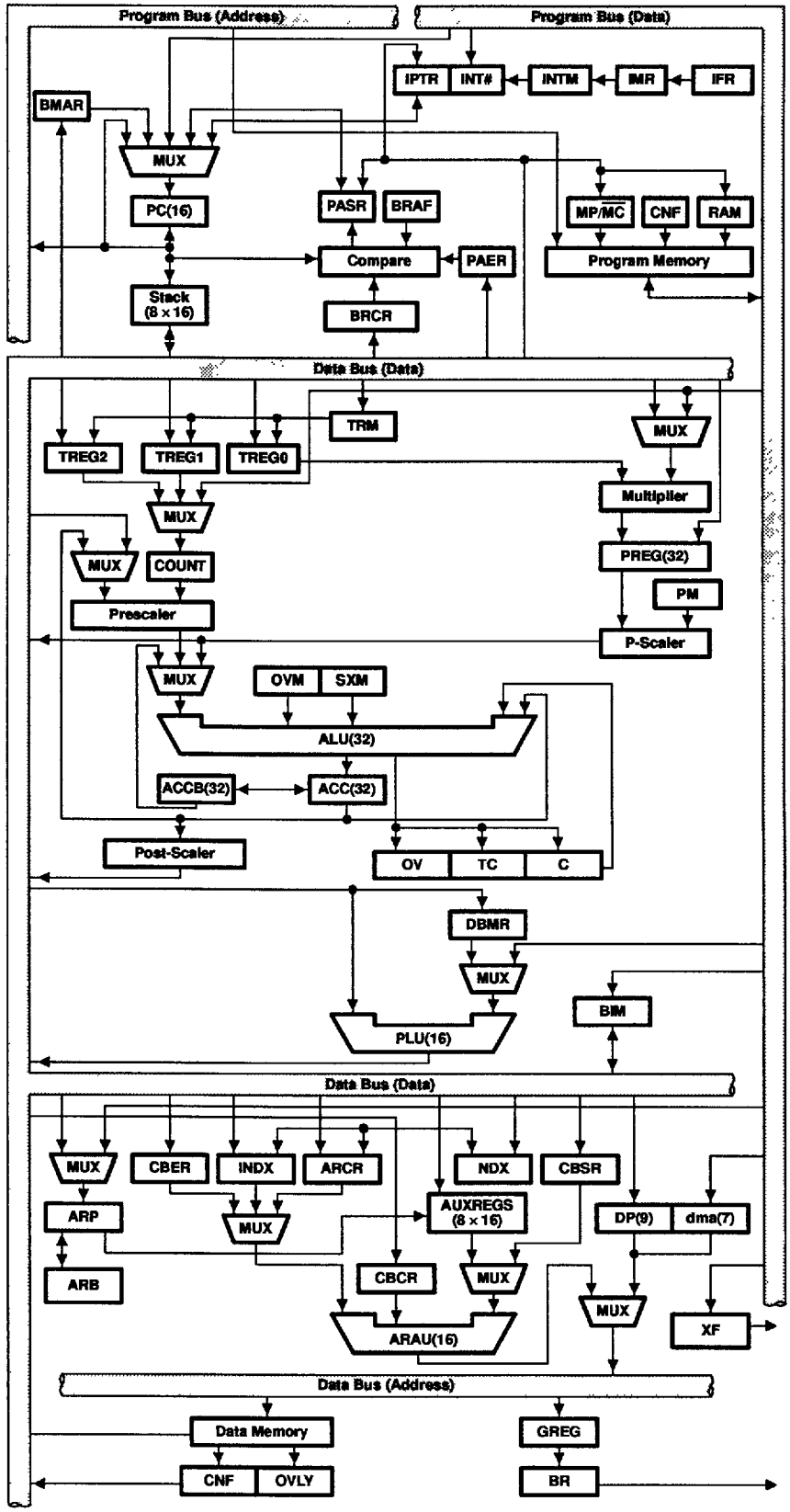
The 'C50A achieves its low power consumption through the IDLE2 instruction. IDLE2 removes the functional clock from the internal hardware of the 'C50A, which puts it into a total-sleep mode that uses only 5 μA. A low logic level on an external interrupt with a duration of at least five clock cycles ends the IDLE2 mode.

The 'C50A is available with two clock speeds. The clock frequencies are 40 MHz, giving a 50-ns cycle time, and 50 MHz, giving a 40-ns cycle time.

AVAILABLE OPTIONS

PART NUMBER	SPEED	SUPPLY VOLTAGE TOLERANCE	PACKAGE
SMJ320C50AGFAM40	50-ns cycle time	±10%	Pin grid array
SMJ320C50AGFAM50	40-ns cycle time	±10%	Pin grid array
SMJ320C50AHFGM40	50-ns cycle time	±10%	Quad flat package
SMJ320C50AHFGM50	40-ns cycle time	±10%	Quad flat package

functional block diagram



PIN ASSIGNMENTS

PIN NO. HFG PKG.	PIN NO. GFA PKG.	PIN NAME	PIN NO. HFG PKG.	PIN NO. GFA PKG.	PIN NAME	PIN NO. HFG PKG.	PIN NO. GFA PKG.	PIN NAME	PIN NO. HFG PKG.	PIN NO. GFA PKG.	PIN NAME
1		NC†	35		NC†	69	P4	V_{SS}	103	T10	V_{SS}
2		NC†	36	H4	V_{SS}	70	T4	V_{SS}	104	T12	V_{SS}
3	D8	V_{SS}	37	K2	V_{SS}	71		NC†	105	C15	TOUT
4	D10	V_{SS}	38	U5	A0 (LSB)	72	R17	$\overline{DS}$	106	B16	TCLKX
5		NC†	39	V4	A1	73	T18	$\overline{IS}$	107	A17	CLKX
6	E3	D7	40	W3	A2	74	U19	$\overline{PS}$	108	C13	TFSR/TADD
7	D2	D6	41	U7	A3	75	N17	R/$\overline{W}$	109	B14	TCLKR
8	C1	D5	42	V6	A4	76	P18	$\overline{STRB}$	110	A15	$\overline{RS}$
9	G3	D4	43	W5	A5	77	R19	$\overline{BR}$	111	C11	READY
10	F2	D3	44	U9	A6	78	L17	CLKIN2	112	B12	$\overline{HOLD}$
11	E1	D2	45	V8	A7	79	M18	X2/CLKIN	113	A13	$\overline{BIO}$
12	J3	D1	46	W7	A8	80	N19	X1	114	R7	V_{DD}
13	H2	D0 (LSB)	47	W9	A9	81	J5	V_{DD}	115	R9	V_{DD}
14	G1	TMS	48	E9	V_{DD}	82	L5	V_{DD}	116	A11	$\overline{IAQ}$
15	C3	V_{DD}	49	E11	V_{DD}	83	L19	TDO	117	A9	$\overline{TRST}$
16	D4	V_{DD}	50	V10	TDI	84	T6	V_{SS}	118	B10	V_{SS}
17	J1	TCK	51	K4	V_{SS}	85	T8	V_{SS}	119	D6	V_{SS}
18	D12	V_{SS}	52	M4	V_{SS}	86	K18	CLKMD2	120	A7	MP/$\overline{MC}$
19	F4	V_{SS}	53		NC†	87	J19	FSX	121	B8	D15 (MSB)
20		NC†	54	W11	CLKMD1	88	G19	TFSX/TFRM	122	C9	D14
21	L1	$\overline{INT1}$	55	W13	A10	89	H18	DX	123	A5	D13
22	N1	$\overline{INT2}$	56	V12	A11	90	J17	TDX	124	B6	D12
23	M2	$\overline{INT3}$	57	U11	A12	91	E19	$\overline{HOLDA}$	125	C7	D11
24	L3	$\overline{INT4}$	58	W15	A13	92	F18	XF	126	A3	D10
25	R1	$\overline{NMI}$	59	V14	A14	93	G17	CLKOUT1	127	B4	D9
26	P2	DR	60	U13	A15	94		NC†	128	C5	D8
27	N3	TDR	61		NC†	95	E17	$\overline{IACK}$	129	A1	V_{DD}
28	T2	FSR	62		NC†	96	N5	V_{DD}	130	B2	V_{DD}
29	R3	CLKR	63	E13	V_{DD}	97	R5	V_{DD}	131		NC†
30	E5	V_{DD}	64	G5	V_{DD}	98		NC†	132		NC†
31	E7	V_{DD}	65	V16	$\overline{RD}$	99		NC†			
32		NC†	66	U15	$\overline{WE}$	100		NC†			
33		NC†	67		NC†	101	B18	EMU0			
34		NC†	68		NC†	102	A19	EMU1/$\overline{OFF}$			

† NC = No connect.

GFA Package additional connections:

V_{DD}: R11, E15, G15, J15, L15, N15, R13, R15, T16, U17, V18, W17, W19

V_{SS}: T14, U1, U3, V2, W1, C17, C19, D14, D16, D18, F16, H16, K16, M16, P16

TEXAS INSTRUMENTS
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Terminal Functions

SIGNAL	TYPE	DESCRIPTION
ADDRESS AND DATA BUSES		
A15 (MSB) A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 (LSB)	I/O/Z	Parallel address bus. Multiplexed to address external data, program memory, or I/O. A0–A15 are in the high-impedance state in hold mode and when $\overline{OFF}$ is active (low). These signals are used as inputs for external DMA access of the on-chip single-access RAM. They become inputs while $\overline{HOLDA}$ is active (low) if $\overline{BR}$ is externally driven low.
D15 (MSB) D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0 (LSB)	I/O/Z	Parallel data bus. Multiplexed to transfer data between the core CPU and external data, program memory, or I/O devices. D0–D15 are in the high-impedance state when not outputting data, when $\overline{RS}$ or $\overline{HOLD}$ is asserted, or when $\overline{OFF}$ is active (low). These signals are also used in external DMA access of the on-chip single-access RAM.
MEMORY CONTROL SIGNALS		
$\overline{DS}$ $\overline{PS}$ $\overline{IS}$	O/Z	Data, program, and I/O space select signals. Always high unless asserted for communicating to a particular external space. $\overline{DS}$, $\overline{PS}$, and $\overline{IS}$ are in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low).
READY	I	Data ready input. Indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY is low), the processor waits one cycle and checks READY again. READY also indicates a bus grant to an external device after a $\overline{BR}$ (bus request) signal.
R/$\overline{W}$	I/O/Z	Read/write. Indicates transfer direction during communication to an external device. Normally in read mode (high) unless asserted for performing a write operation. R/$\overline{W}$ is in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low). Used in external DMA access of the 9K RAM cell. While $\overline{HOLDA}$ and $\overline{IAQ}$ are active (low), this signal is used to indicate the direction of the data bus for DMA reads (high) and writes (low).

NOTE: All input pins that are unused should be connected to V_{DD} or an external pullup resistor. The $\overline{BR}$ pin has an internal pullup for performing DMA to the on-chip RAM. For emulation, $\overline{TRST}$ has an internal pulldown, and TMS, TCK, and TDI have internal pullups. EMU0 and EMU1 require external pullups to support emulation.

Terminal Functions (continued)

SIGNAL	TYPE	DESCRIPTION
		MEMORY CONTROL SIGNALS (CONTINUED)
$\overline{STRB}$	I/O/Z	Strobe. Always high unless asserted to indicate an external bus cycle. $\overline{STRB}$ is in the high-impedance state in the hold mode or when $\overline{OFF}$ is active (low). Used in external DMA access of the on-chip single-access RAM. While $\overline{HOLDA}$ and $\overline{IAQ}$ are active (low), this signal is used to select the memory access.
$\overline{RD}$	O/Z	Read select. Indicates an active external read cycle and can connect directly to the output enable ($\overline{OE}$) of external devices. This signal is active on all external program, data, and I/O reads. $\overline{RD}$ is in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low).
$\overline{WE}$	O/Z	Write enable. The falling edge indicates that the device is driving the external data bus (D15 – D0). Data can be latched by an external device on the rising edge of $\overline{WE}$. This signal is active on all external program, data, and I/O writes. $\overline{WE}$ is in the high-impedance state in hold mode or when $\overline{OFF}$ is active (low).
		MULTIPROCESSING SIGNALS
$\overline{HOLD}$	I	Hold. Asserted to request control of the address, data, and control lines. When acknowledged by the 'C50A, these lines go to the high-impedance state.
$\overline{HOLDA}$	O/Z	Hold acknowledge. Indicates to the external circuitry that the processor is in a hold state and that the address, data, and memory control lines are in the high-impedance state so that they are available to the external circuitry for access of local memory. This signal also goes to the high-impedance state when $\overline{OFF}$ is active (low).
$\overline{BR}$	I/O/Z	Bus request. Asserted during access of external global data memory space. READY is asserted when the global data memory is available for the bus transaction. $\overline{BR}$ can be used to extend the data memory address space by up to 32K words. $\overline{BR}$ goes to the high-impedance state when $\overline{OFF}$ is active low. $\overline{BR}$ is used in external DMA access of the on-chip single-access RAM. While $\overline{HOLDA}$ is active (low), $\overline{BR}$ is externally driven (low) to request access to the on-chip single-access RAM.
$\overline{IAQ}$	O/Z	Instruction acquisition. Asserted (active) when there is an instruction address on the address bus; goes into the high-impedance state when $\overline{OFF}$ is active (low). $\overline{IAQ}$ is also used in external DMA access of the on-chip single-access RAM. While $\overline{HOLDA}$ is active (low), $\overline{IAQ}$ acknowledges the $\overline{BR}$ request for access of the on-chip single-access RAM and stops indicating instruction acquisition.
$\overline{BIO}$	I	Branch control. Samples as the BIO condition. If low, the device executes the conditional instruction. $\overline{BIO}$ must be active during the fetch of the conditional instruction.
XF	O/Z	External flag (latched software-programmable signal). Set high or low by a specific instruction or by loading status register 1 (ST1). Used for signaling other processors in multiprocessor configurations or as a general-purpose output. XF goes to the high-impedance state when $\overline{OFF}$ is active (low) and is set high at reset.
$\overline{IACK}$	O/Z	Interrupt acknowledge. Indicates receipt of an interrupt and that the program counter is fetching the interrupt vector location designated by A15 – A0. $\overline{IACK}$ goes to the high-impedance state when $\overline{OFF}$ is active (low).
		INITIALIZATION, INTERRUPT, AND RESET OPERATIONS
$\overline{INT4}$ $\overline{INT3}$ $\overline{INT2}$ $\overline{INT1}$	I	External interrupts. Prioritized and maskable by the interrupt mask register (IMR) and interrupt mode bit (INTM, bit 9 of status register 0). These signals can be polled and reset via the interrupt flag register.
$\overline{NMI}$	I	Nonmaskable interrupt. External interrupt that cannot be masked via INTM or IMR. When $\overline{NMI}$ is activated, the processor traps to the appropriate vector location.
$\overline{RS}$	I	Reset. Causes the device to terminate execution and forces the program counter to zero. When $\overline{RS}$ is brought to a high level, execution begins at location zero of program memory.
MP/$\overline{MC}$	I	Microprocessor/microcomputer select. If active (low) at reset (microcomputer mode), the signal causes the internal program ROM to be mapped into program memory space. In the microprocessor mode, all program memory is mapped externally. This signal is sampled only during reset, and the mode that is set at reset can be overridden via the software control bit MP/$\overline{MC}$ in the PMST register.

Terminal Functions (continued)

SIGNAL	TYPE	DESCRIPTION
OSCILLATOR/TIMER SIGNALS		
CLKOUT1	O/Z	Master clock (or CLKIN2 frequency). CLKOUT1 cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the rising edges of this signal. This signal goes to the high-impedance state when $\overline{OFF}$ is active (low).
CLKMD1 CLKMD2	I	CLKMD1 CLKMD2 Clock mode 0 0 External clock with divide-by-two option. Input clock provided to X2/CLKIN1. Internal oscillator and PLL disabled. 0 1 Reserved for test purposes 1 0 External divide-by-one option. Input clock provided to CLKIN2. Internal oscillator is disabled and internal PLL is enabled. 1 1 Internal or external divide-by-two option. Input clock provided to X2/CLKIN1. Internal oscillator is enabled and internal PLL is disabled.
X2/CLKIN	I	Input to the internal oscillator from the crystal. If the internal oscillator is not being used, a clock may be input to the device on X2/CLKIN. The internal machine cycle is half this clock rate.
X1	O	Output from the internal oscillator for the crystal. If the internal oscillator is not used, X1 should be left unconnected. This signal does not go to the high-impedance state when $\overline{OFF}$ is active (low).
CLKIN2	I	Divide-by-one input clock for driving the internal machine rate.
TOUT	O	Timer output. TOUT signals a pulse when the on-chip timer counts down past zero. The pulse is a CLKOUT1 cycle wide.
SUPPLY PINS		
V_{DD1} V_{DD2} V_{DD3} V_{DD4}	S	Power supply for data bus
V_{DD5} V_{DD6}	S	Power supply for address bus
V_{DD7} V_{DD8}	S	Power supply for inputs and internal logic
V_{DD9} V_{DD10}	S	Power supply for address bus
V_{DD11} V_{DD12}	S	Power supply for memory control signals
V_{DD13} V_{DD14}	S	Power supply for inputs and internal logic
V_{DD15} V_{DD16}	S	Power supply for memory control signals
V_{SS1} V_{SS2}	S	Ground for memory control signals
V_{SS3} V_{SS4} V_{SS5} V_{SS6}	S	Ground for data bus
V_{SS7} V_{SS8} V_{SS9} V_{SS10}	S	Ground for address bus

Terminal Functions (continued)

SIGNAL	TYPE	DESCRIPTION
SUPPLY PINS (CONTINUED)		
V_{SS11} V_{SS12}	S	Ground for memory control signals
V_{SS13} V_{SS14} V_{SS15} V_{SS16}	S	Ground for inputs and internal logic
SERIAL PORT SIGNALS		
CLKR TCLKR	I	Receive clock. External clock signal for clocking data from DR (data receive) or TDR (TDM data receive) into the RSR (serial port receive shift register). Must be present during serial port transfers. If the serial port is not being used, these signals can be sampled as an input via the IN0 bit of the serial port control (SPC) or TDR serial port control (TSPC) registers.
CLKX TCLKX	I/O/Z	Transmit clock. Clock signal for clocking data from the DR or TDR to the DX (data transmit) or TDX (TDM data transmit pins). CLKX can be an input if the MCM bit in the serial port control register is set to 0. It can also be driven by the device at 1/4 the CLKOUT1 frequency when the MCM bit is set to 1. If the serial port is not being used, this pin can be sampled as an input via the IN1 bit of the SPC or TSPC register. This signal goes into the high-impedance state when $\overline{OFF}$ is active (low).
DR TDR	I	Serial data receive. Serial data is received in the RSR (serial port receive shift register) via DR or TDR.
DX TDX	O/Z	Serial port transmit. Serial data transmitted from XSR (serial port transmit shift register) via DX or TDX. This signal is in the high-impedance state when not transmitting and when $\overline{OFF}$ is active (low).
FSR TFSR/TADD	I I/O/Z	Frame synchronization pulse for receive. The falling edge of FSR or TFSR initiates the data receive process, which begins the clocking of the RSR. TFSR becomes an input/output (TADD) pin when the serial port is operating in the TDM mode (TDM bit = 1). In TDM mode, this pin is used to input/output the address of the port. This signal goes into the high-impedance state when $\overline{OFF}$ is active (low).
FSX TFSX/TFRM	I/O/Z	Frame synchronization pulse for transmit. The falling edge of FSX/TFSX initiates the data transmit process, which begins the clocking of the XSR. Following reset, the default operating condition of FSX/TFSX is an input. This pin may be selected by software to be an output when the TXM bit in the serial control register is set to 1. This signal goes to the high-impedance state when $\overline{OFF}$ is active (low). When operating in TDM mode (TDM bit = 1), TFSX becomes TFRM, the TDM frame synchronization pulse.
TEST SIGNALS		
TCK	I	JTAG test clock. This is normally a free-running clock with a 50% duty cycle. The changes of TAP (test access port) input signals (TMS and TDI) are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI	I	JTAG test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z	JTAG test data output. The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance state except when scanning of data is in progress. This signal also goes to the high-impedance state when $\overline{OFF}$ is active (low).
TMS	I	JTAG test mode select. This serial control input is clocked into the test access port (TAP) controller on the rising edge of TCK.
$\overline{TRST}$	I	JTAG test reset. Asserting this signal gives the JTAG scan system control of the operations of the device. If this signal is not connected or is driven low, the device operates in its functional mode and the JTAG signals are ignored.

Terminal Functions (continued)

SIGNAL	TYPE	DESCRIPTION
		TEST SIGNALS (CONTINUED)
EMU0	I/O/Z	Emulator 0. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for activation of the $\overline{\text{OFF}}$ condition (see EMU1/$\overline{\text{OFF}}$). When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output put via JTAG scan.
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator 1/$\overline{\text{OFF}}$. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as input/output via JTAG scan. When $\overline{\text{TRST}}$ is driven low, EMU1/$\overline{\text{OFF}}$ is configured as $\overline{\text{OFF}}$. When the $\overline{\text{OFF}}$ signal is active (low), all output drivers are in the high-impedance state. $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (not for multiprocessing applications). For the $\overline{\text{OFF}}$ condition, the following conditions apply: • $\overline{\text{TRST}}$ = Low • EMU0 = High • EMU1/$\overline{\text{OFF}}$ = Low
RESERVED†	N/C	Reserved. This pin should be left unconnected.

† Quad flat pack only

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... – 0.3 V to 7 V
Input voltage range ..... – 0.3 V to 7 V
Output voltage range ..... – 0.3 V to 7 V
Maximum operating case temperature ..... 125°C
Minimum operating free-air temperature, T_A ..... – 55°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

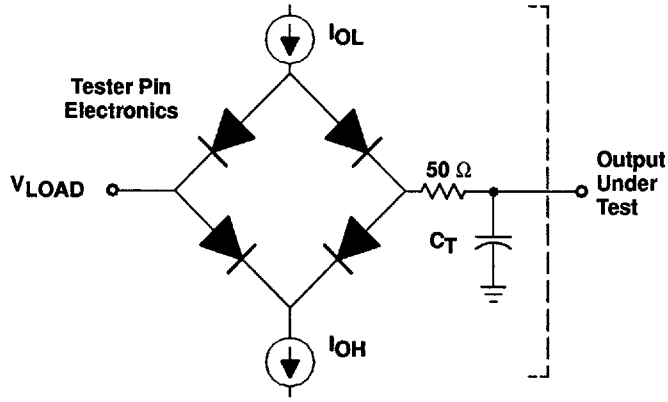
			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	CLKIN, CLKIN2	3.0		V_{DD} + 0.3	V
		CLKX, CLKR, TCLKX, TCLKR	2.5		V_{DD} + 0.3	V
		All others	2.2		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage		– 0.3		0.6	V
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature				125	°C
T_A	Operating free-air temperature		– 55			°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	MIN	TYP§	MAX	UNIT
V_{OH}	High-level output voltage¶	I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage§	I_{OL} = MAX		0.3	0.6	V
I_{OZ}	High-impedance output current (V_{DD} = MAX)	BR	– 400	#	30	µA
		All others	– 30	#	30	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$ (with internal pulldown)	– 30	#	800	µA
		TMS, TCK, TDI (with internal pullups)	– 400	#	30	
		X2/CLKIN	– 50	#	50	
		All other inputs	– 10	#	50	mA
I_{DDC}	Supply current, core CPU	Operating, T_A = 25°C, V_{DD} = 5.25 V, f_x = 40.96 MHz		60		mA
I_{DDP}	Supply current, pins	Operating, T_A = 25°C, V_{DD} = 5.25 V, f_x = 40.96 MHz		40		mA
I_{DD}	Supply current, standby	IDLE instruction, T_A = – 55°C, V_{DD} = 5.5 V, f_x = 50 MHz			30	mA
		IDLE2 instruction, Clocks shut off, T_A = – 55°C, V_{DD} = 5.5 V			7	mA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

‡ For conditions shown as MIN/MAX, use the appropriate value specified under "recommended operating conditions".
§ All typical or nominal values are at V_{DD} = 5 V, T_A = 25°C.
¶ All input and output voltage levels are TTL-compatible. Figure 1 shows the tested load circuit; Figure 2 and Figure 3 show the voltage reference levels.
# These values are not specified pending detailed characterization.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2.0 mA (all outputs)
I_{OH} = 300 μA (all outputs)
V_{LOAD} = 1.5 V
C_T = 80 pF typical load circuit capacitance

Figure 1. Test Load Circuit

signal transition levels

TTL-output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Figure 2 shows the TTL-level outputs.

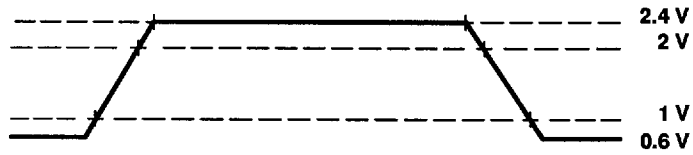


Figure 2. TTL-Level Outputs

TTL-output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is 2 V, and the level at which the output is said to be low is 1 V.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 1 V, and the level at which the output is said to be high is 2 V.

Figure 3 shows the TTL-level inputs.

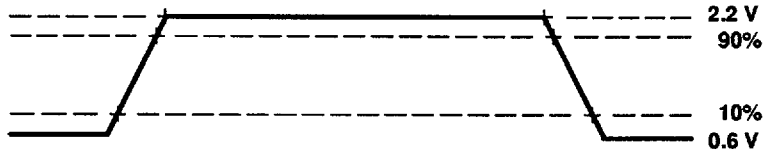


Figure 3. TTL-Level Inputs

TTL-compatible input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 2 V, and the level at which the input is said to be low is 0.8 V.
- For a low to high transisiton on an input signal, the level at which the input is said to be no longer low is 0.8 V, and the level at which the input is said to be high is 2 V.

CLOCK CHARACTERISTICS AND TIMING

The 'C50A can use either its internal oscillator or an external frequency source for a clock. The clock mode is determined by the CLKMD1 and CLKMD2 pins. The following table outlines the selection of the clock mode by these pins.

CLKMD1	CLKMD2	CLOCK SOURCE
1	0	External divide-by-one clock option
0	1	Reserved for test purposes
1	1	External divide-by-two option or internal divide-by-two clock option with an external crystal
0	0	External divide-by-two option with the internal oscillator disabled

internal divide-by-two clock option with external crystal

The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT1 is one-half the crystal's oscillating frequency. The crystal should be in either fundamental or overtone operation and parallel resonant, with an effective series resistance of 30 Ω and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF. Overtone crystals require an additional tuned LC circuit. Figure 4 shows an external crystal (fundamental frequency) connected to the on-chip oscillator.

recommended operating conditions for internal divide-by-two clock option

PARAMETER			MIN	NOM	MAX	UNIT
f_x	Input clock frequency	SMJ320C50A-40	0†		40	MHz
		SMJ320C50A-50‡	0†		50	MHz
C1, C2	Load capacitance			10		pF

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz but is tested at a minimum of 3.3 MHz to meet device test time requirements.

‡ Other timings for the 'C50A-50 device are the same as those for the 'C50A-40 device except where otherwise indicated.

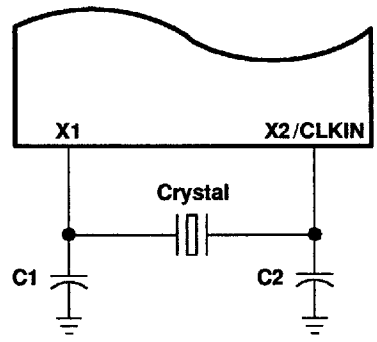


Figure 4. Internal Clock Option

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external divide-by-two clock option

An external frequency source can be used by injecting the frequency directly into X2/CLKIN with X1 left unconnected, CLKMD1 set high, and CLKMD2 set high. The external frequency is divided by two to generate the internal machine cycle. The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

PARAMETER			MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	'320C50-40	50	$2t_{c(CI)}$	†	ns
		'320C50-50‡	40	$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT1 high/low		6	11	20	ns
$t_{f(CO)}$	Fall time, CLKOUT1			5		ns
$t_{r(CO)}$	Rise time, CLKOUT1			5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low		H – 2	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high		H – 2	H	H + 2	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, CLKIN	'320C50A-40	25	†	ns
		'320C50A-50‡	20	†	ns
$t_{f(CI)}$	Fall time, CLKIN§			5	ns
$t_{r(CI)}$	Rise time, CLKIN§			5	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	'320C50A-40	11	†	ns
		'320C50A-50‡	8	†	ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	'320C50A-40	11	†	ns
		'320C50A-50‡	8	†	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz, but is tested at a minimum of 6.7 MHz to meet device test time requirements.
‡ Other timings for the 'C50A-50 device are the same as those for the 'C50A-40 device except where otherwise indicated.
§ Values derived from characterization data and not tested.

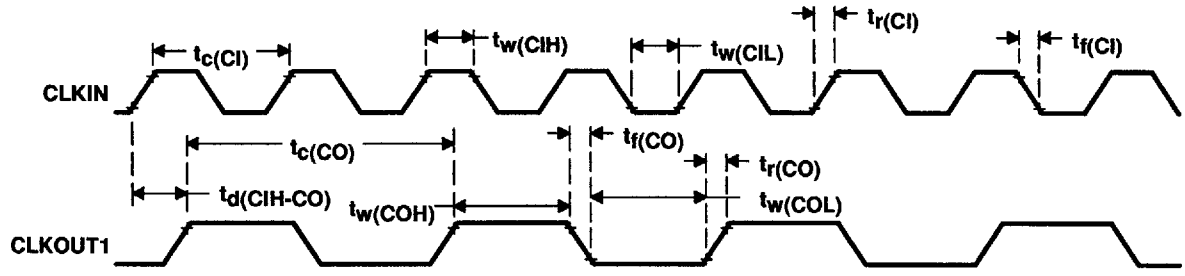

Figure 5. External Divide-by-Two Clock Timing

external divide-by-one clock option

An external frequency source can be used by injecting the frequency directly into CLKIN2 with X1 left unconnected and X2 connected to V_{DD}. This external frequency is divided by one to generate the internal machine cycle. The divide-by-one option is used when CLKMD1 is strapped high and CLKMD2 is strapped low. The external frequency injected must conform to specifications listed in the timing requirements table.

switching characteristics over recommended operating conditions [H = 0.5 $t_{c(CO)}$]

PARAMETER			MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT1	'320C50A-40	50	$t_{c(CI)}$	75†	ns
		'320C50A-50‡	40	$t_{c(CI)}$	75†	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN2 high to CLKOUT1 high		2	9	16	ns
$t_{f(CO)}$	Fall time, CLKOUT1			5		ns
$t_{r(CO)}$	Rise time, CLKOUT1			5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT1 low		H – 2	H	H + 2	ns
$t_{w(COH)}$	Pulse duration, CLKOUT1 high		H – 2	H	H + 2	ns
t_p	Transitory phase – PLL synchronized after CLKIN2 supplied		256§		1000¶	cycles

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, CLKIN2	'320C50A-40	50	75†	ns
		'320C50A-50‡	40	75†	ns
$t_{f(CI)}$	Fall time, CLKIN2¶			5	ns
$t_{r(CI)}$	Rise time, CLKIN2¶			5	ns
$t_{w(CIL)}$	Pulse duration, CLKIN2 low	'320C50A-40	15	60	ns
		'320C50A-50‡	11	64	ns
$t_{w(CIH)}$	Pulse duration, CLKIN2 high	'320C50A-40	15	60	ns
		'320C50A-50‡	11	64	ns

† Clocks can be stopped only while the device executes IDLE2 when using the external divide-by-one clock option. Note that tp (the transitory phase) will occur when restarting clock from IDLE2 in this mode.
‡ Other timings for the 'C50A-50 device are the same as those for the 'C50A-40 device except where indicated otherwise.
§ Values are specified by design and not tested.
¶ Values derived from characterization data and not tested.

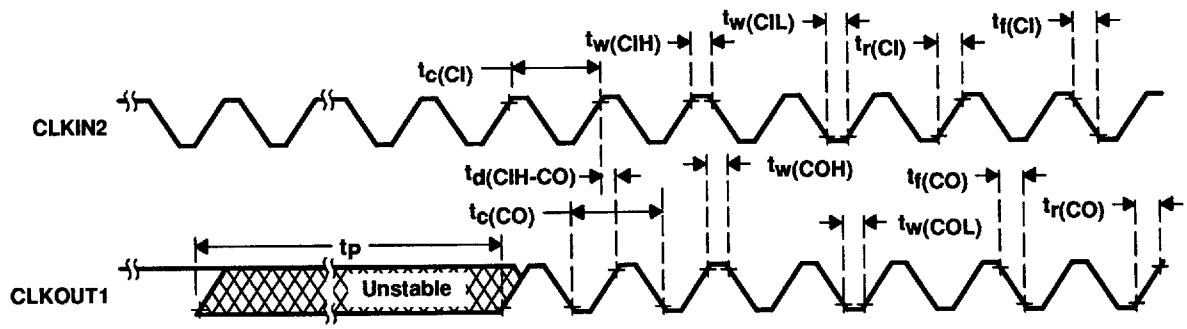

Figure 6. External Divide-by-One Clock Timing

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MEMORY AND PARALLEL I/O INTERFACE READ

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

	PARAMETER	MIN	MAX	UNIT
$t_{su(A)R}$	Setup time, address valid before $\overline{RD}$ low†	H–10‡		ns
$t_{h(A)R}$	Hold time, address valid after $\overline{RD}$ high†	0‡		ns
$t_{w(RL)}$	Pulse duration, $\overline{RD}$ low§¶	H–8		ns
$t_{w(RH)}$	Pulse duration, $\overline{RD}$ high§¶	H–8		ns
$t_{d(RW)}$	Delay time, $\overline{RD}$ high to $\overline{WE}$ low	2H–5		ns

† A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address.
‡ See Figure 8 for address bus timing variation with load capacitance.
§ $\overline{STRB}$ and $\overline{RD}$ timing is – 3/+5 ns from CLKOUT1 timing on read cycles, following the first cycle after reset, which is always a 7 wait-state cycle.
¶ Values derived from characterization data and are not tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$]

			MIN	MAX	UNIT
$t_{a(A)}$	Access time, read data valid from address valid	'320C50A-40		2H–15‡	ns
		'320C50A-50#		2H–15‡	ns
$t_{a(R)}$	Access time, read data valid after $\overline{RD}$ low			H–10	ns
$t_{su(D)R}$	Setup time, read data valid before $\overline{RD}$ high		10		ns
$t_{h(D)R}$	Hold time, read data valid after $\overline{RD}$ high		0		ns

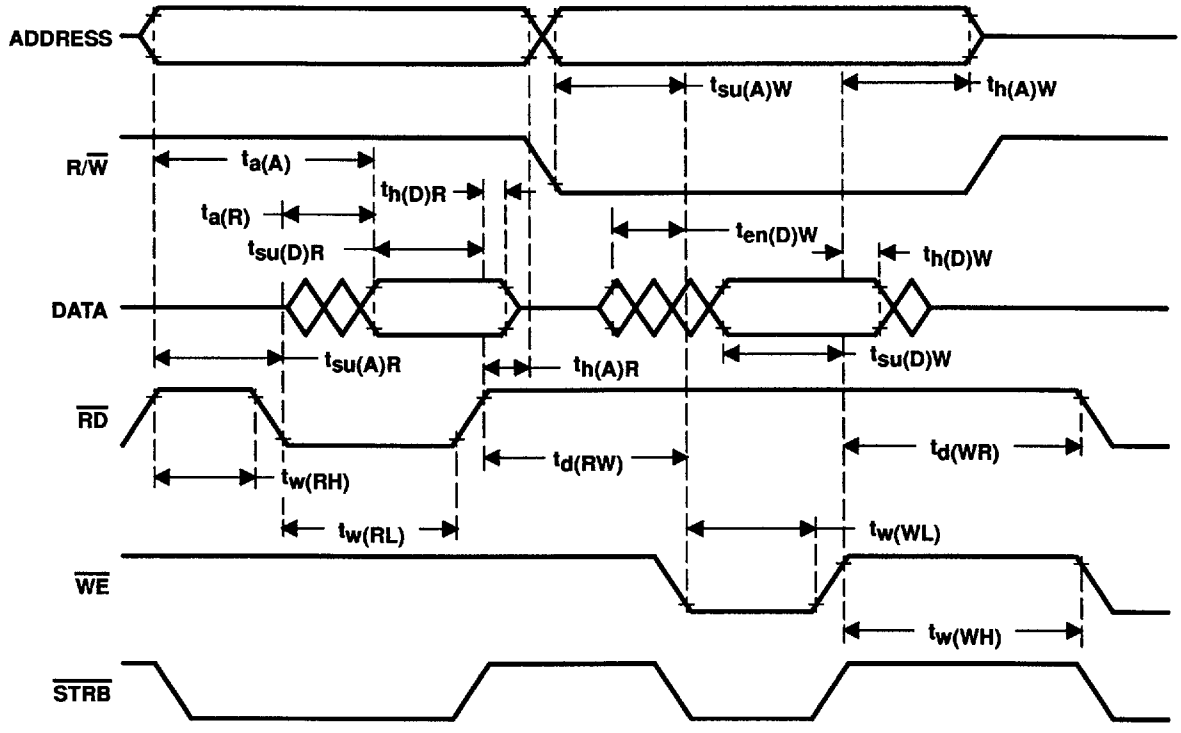
‡ See Figure 8 for address bus timing variation with load capacitance.
# Other timings for 'C50A-50 device are the same as for the 'C50A-40 device except where indicated otherwise.

MEMORY AND PARALLEL I/O INTERFACE WRITE

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

	PARAMETER	MIN	MAX	UNIT
$t_{su(A)W}$	Setup time, address valid before $\overline{WE}$ low†	H – 5‡		ns
$t_{h(A)W}$	Hold time, address valid after $\overline{WE}$ high†	H – 10‡		ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low§	2H – 8		ns
$t_{w(WH)}$	Pulse duration, $\overline{WE}$ high§	2H – 8		ns
$t_{d(WR)}$	Delay time, $\overline{WE}$ high to $\overline{RD}$ low	3H – 10		ns
$t_{su(D)W}$	Setup time, write data valid before $\overline{WE}$ high§	2H – 20	2H¶#	ns
$t_{h(D)W}$	Hold time, write data valid after $\overline{WE}$ high§	H – 5	H+10¶	ns
$t_{en(D)W}$	Enable time, $\overline{WE}$ to data bus driven	-5¶		ns

† A15–A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address.
‡ See Figure 8 for address bus timing variation with load capacitance.
§ $\overline{STRB}$ and $\overline{WE}$ edges are 0 – 4 ns from CLKOUT1 edges on writes. Rising and falling edges of these signals track each other; tolerance of resulting pulse durations is ± 2 ns, not ± 4 ns.
¶ Values derived from characterization data and are not tested.
# This value holds true for zero or one wait state only.



NOTE A: All timings are for 0 wait states. However, external writes always require two cycles to prevent external bus conflicts. The above diagram illustrates a one-cycle read and a two-cycle write and is not drawn to scale. All external writes immediately preceded by an external read or immediately followed by an external read require three machine cycles.

Figure 7. Memory and Parallel I/O Interface Read and Write Timing

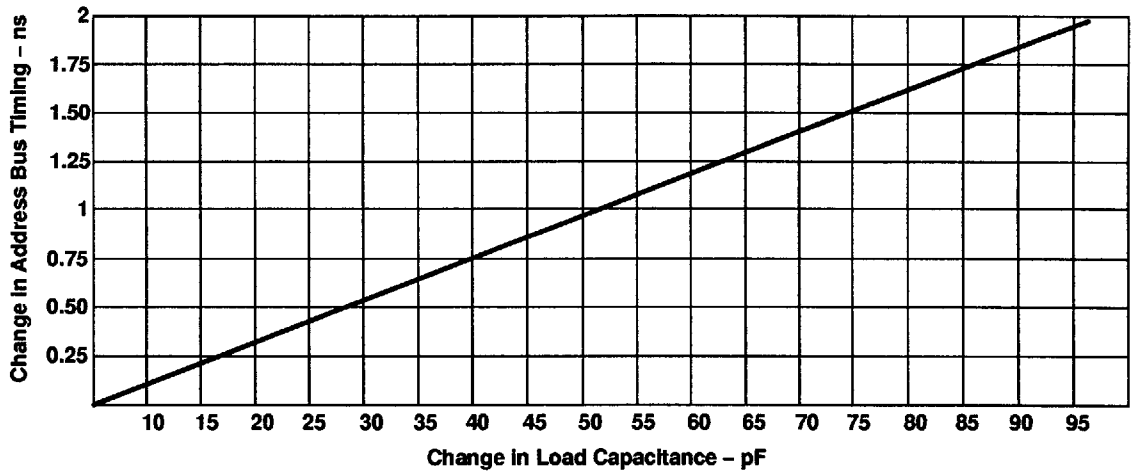


Figure 8. Address Bus Timing Variation With Load Capacitance

READY TIMING FOR EXTERNALLY GENERATED WAIT STATES

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
$t_{su(R-CO)}$	Setup time, READY before CLKOUT1 rises	10		ns
$t_{h(CO-R)}$	Hold time, READY after CLKOUT1 rises	0		ns
$t_{su(R)R}$	Setup time, READY before $\overline{RD}$ falls	15		ns
$t_{h(R)R}$	Hold time, READY after $\overline{RD}$ falls	5		ns
$t_{v(R)W}$	Valid time, READY after $\overline{WE}$ falls	H – 15		ns
$t_{h(R)W}$	Hold time, READY after $\overline{WE}$ falls	H + 5		ns

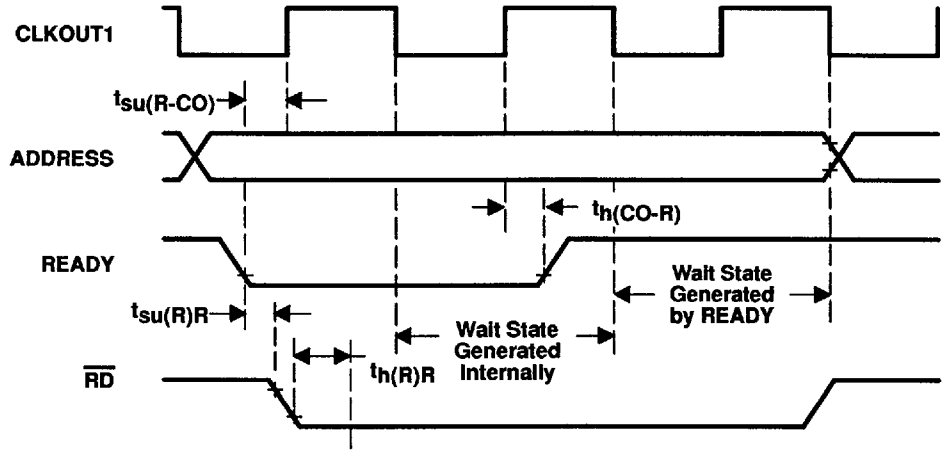


Figure 9. Ready Timing for Externally Generated Wait States During an External Read Cycle

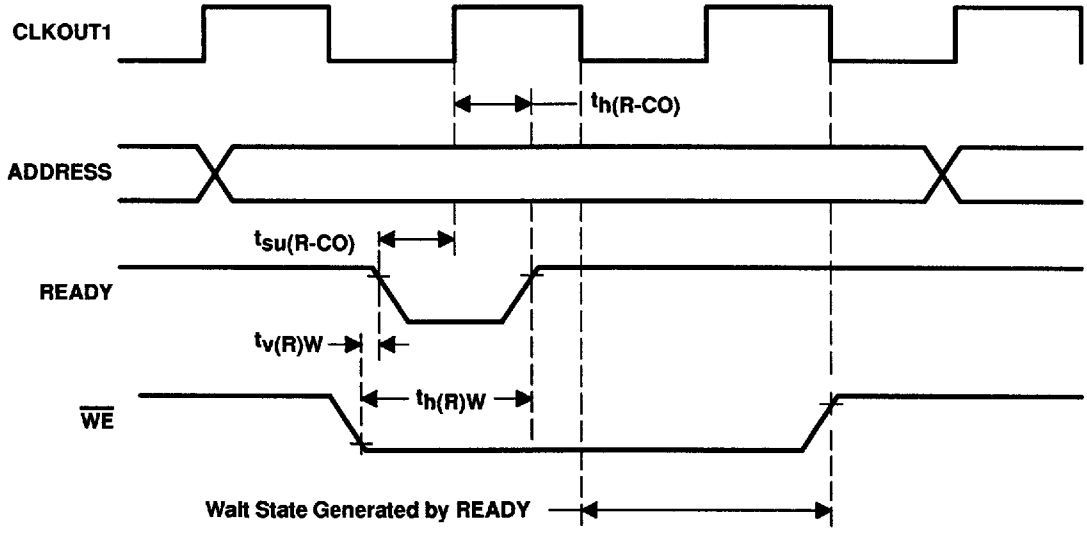


Figure 10. Ready Timing for Externally Generated Wait States During an External Write Cycle

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RESET, INTERRUPT, AND $\overline{BIO}$

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = $0.5t_{c(CO)}$]

	PARAMETER	MIN	MAX	UNIT
$t_{su(IN)}$	Setup time, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$, before CLKOUT1 low †	15		ns
$t_{h(IN)}$	Hold time, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$, after CLKOUT1 low †	0		ns
$t_{w(INL)s}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ low, synchronous	4H+15‡		ns
$t_{w(INH)s}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ high, synchronous	2H+15‡¶		ns
$t_{w(INL)a}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ low, asynchronous §	6H+15‡		ns
$t_{w(INH)a}$	Pulse duration, $\overline{INT1}$–$\overline{INT4}$, $\overline{NMI}$ high, asynchronous §	4H+15‡		ns
$t_{su(R)}$	Setup time, $\overline{RS}$ before X2/CLKIN low	10		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low	20H		ns
$t_{d(EX)}$	Delay time, $\overline{RS}$ high to reset vector fetch	34H		ns
$t_{w(BI)s}$	Pulse duration, $\overline{BIO}$ low, synchronous	15		ns
$t_{w(BI)a}$	Pulse duration, $\overline{BIO}$ low, asynchronous §	H+15		ns
$t_{su(BI)}$	Setup time, $\overline{BIO}$ before CLKOUT1 low	15		ns
$t_{h(BI)}$	Hold time, $\overline{BIO}$ after CLKOUT1 low	0		ns

† These parameters must be met to use the synchronous timings. Both reset and the interrupts can operate asynchronously. The pulse durations require an extra half-cycle to assure internal synchronization.
‡ If in IDLE2, add 4H to these timings.
§ Values derived from characterization data and are not tested.
¶ Values are specified by design and not tested.

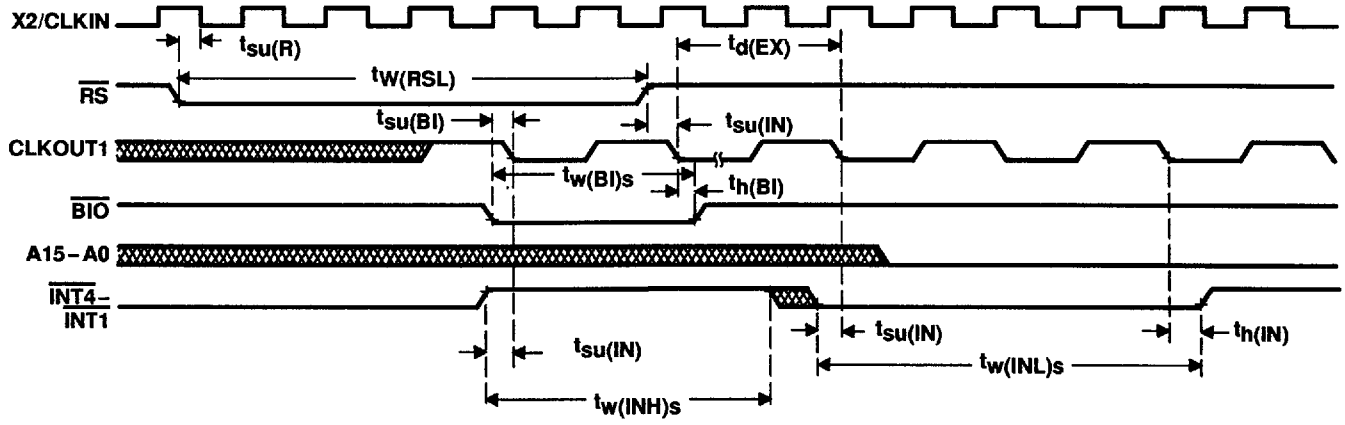


Figure 11. Reset, Interrupt, and $\overline{BIO}$ Timings

INSTRUCTION ACQUISITION ($\overline{IAQ}$), INTERRUPT ACKNOWLEDGE ($\overline{IACK}$), EXTERNAL FLAG (XF), AND TOUT

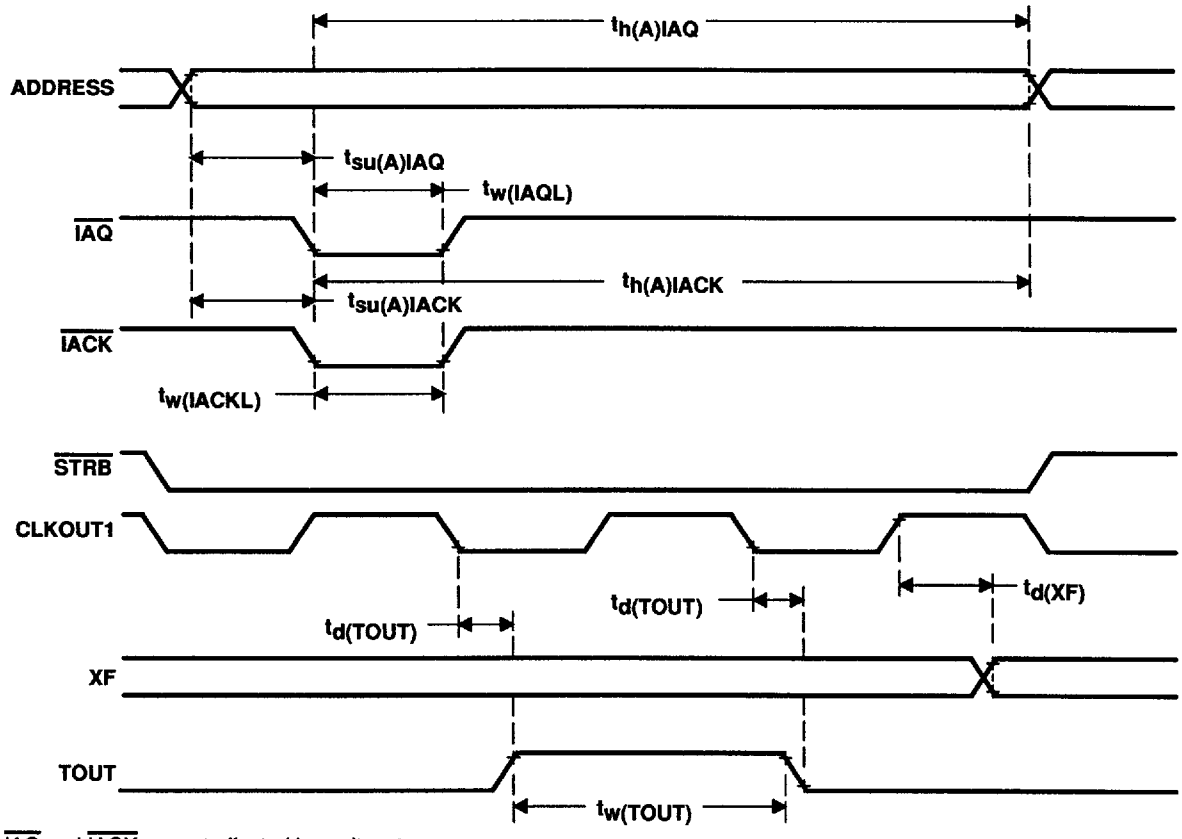
switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

	PARAMETER	MIN	MAX	UNIT
$t_{su(A)IAQ}$	Setup time, address valid before $\overline{IAQ}$ low†	H–14‡		ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ low	H–8‡		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	H–10‡		ns
$t_{d(TOUT)}$	Delay time, CLKOUT1 falling to TOUT	–6	6	ns
$t_{su(A)IACK}$	Setup time, address valid before $\overline{IACK}$ low§	H–14‡		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high §	H–8‡		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	H–10‡		ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H–12		ns
$t_{d(XF)}$	Delay time, XF valid after CLKOUT1	0	12	ns

† $\overline{IAQ}$ goes low during an instruction acquisition. It goes low only on the first cycle of the read when wait states are used. The falling edge should be used to latch the valid address. The AVIS bit in the PMST register must be set to zero for the address to be valid when the instruction being addressed resides in on-chip memory.

‡ Valid only if the external address reflects the current instruction activity (that is, code is executing on chip with no external bus cycles and AVIS is on, or code is executing off-chip).

§ $\overline{IACK}$ goes low during the fetch of the first word of the interrupt vector. It goes low only on the first cycle of the read when wait states are used. Address pins A1 – A4 can be decoded at the falling edge to identify the interrupt being acknowledged. The AVIS bit in the PMST register must be set to zero for the address to be valid when the vectors reside in on-chip memory.



NOTE: $\overline{IAQ}$ and $\overline{IACK}$ are not affected by wait states.

Figure 12. $\overline{IAQ}$, $\overline{IACK}$, and XF Timings Example With Two External Wait States

EXTERNAL DMA

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Note 2)

	PARAMETER	MIN	MAX	UNIT
$t_{d(H-HA)}$	Delay time, $\overline{HOLD}$ low to $\overline{HOLDA}$ low	4H	‡	ns
$t_{d(HH-HA)}$	Delay time, $\overline{HOLD}$ high before $\overline{HOLDA}$ high	2H		ns
$t_{dis(M-HA)}$	Disable time, address in the high-impedance state before $\overline{HOLDA}$ low§	H–15†		ns
$t_{en(HA-M)}$	Enable time, $\overline{HOLDA}$ high to address driven	H–5†		ns
$t_{d(B-I)}$	Delay time, $\overline{XBR}$ low to $\overline{IAQ}$ low	4H†	6H†	ns
$t_{d(BH-I)}$	Delay time, $\overline{XBR}$ high to $\overline{IAQ}$ high	2H†	4H†	ns
$t_{d(D)XR}$	Delay time, read data valid after $\overline{XSTRB}$ low		40	ns
$t_{h(D)XR}$	Hold time, read data after $\overline{XSTRB}$ high	0		ns
$t_{en(I-D)}$	Enable time, $\overline{IAQ}$ low to read data driven¶	0†	2H†	ns
$t_{dis(W)}$	Disable time, XR/$\overline{W}$ low to data in the high-impedance state	0†	15†	ns
$t_{dis(I-D)}$	Disable time, $\overline{IAQ}$ high to data in the high-impedance state		H†	ns
$t_{en(D)RW}$	Enable time, data from XR/$\overline{W}$ going high		4†	ns

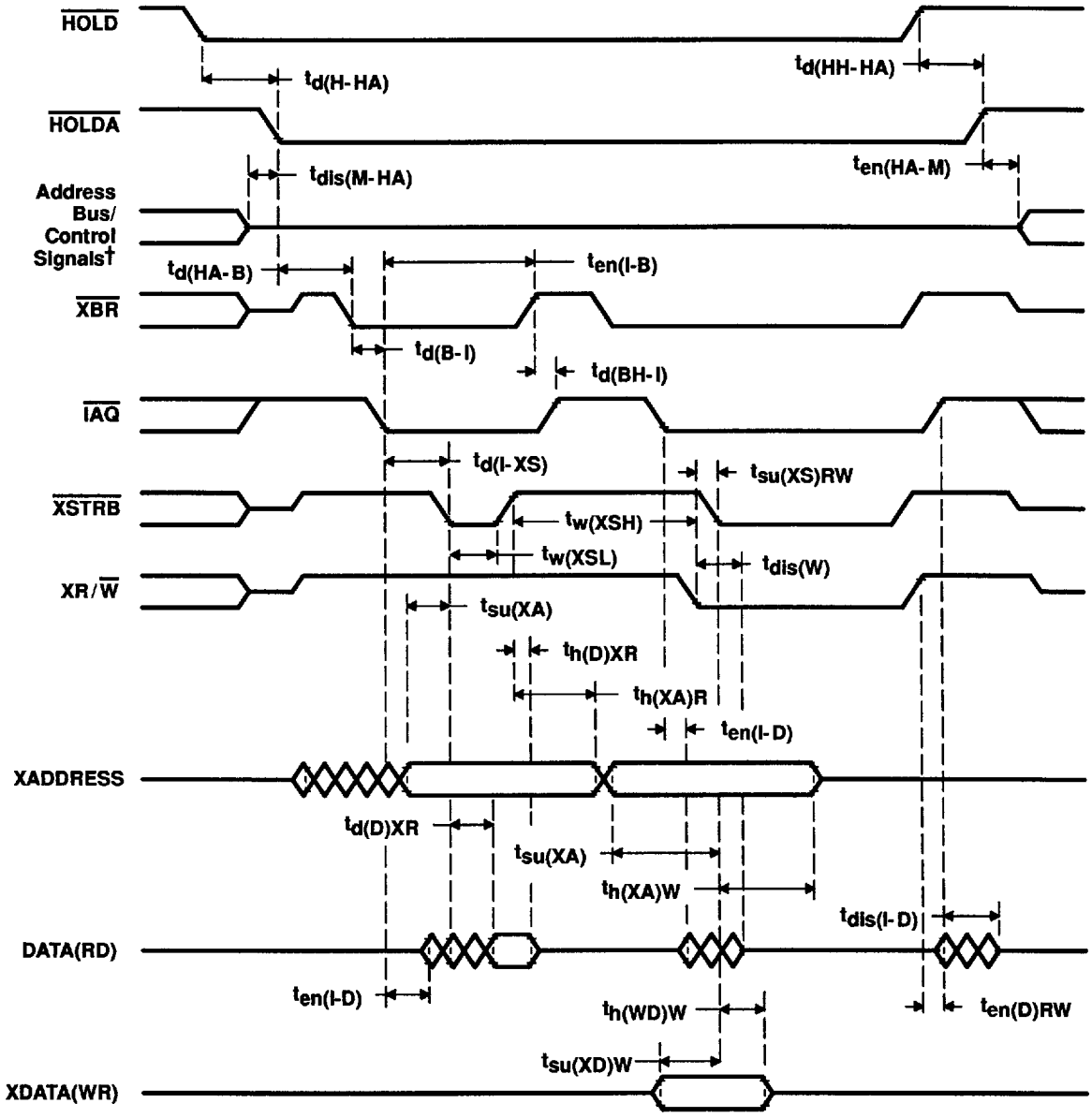
† Values derived from characterization data and are not tested.
‡ $\overline{HOLD}$ is not acknowledged until current external access request is complete.
§ This parameter includes all memory control lines.
¶ This parameter refers to the delay between the time the condition ($\overline{IAQ}$ = 0 and XR/$\overline{W}$ = 1) is satisfied and the time that the SMJ320C50A data lines become valid.
NOTE 2: X preceding a name refers to the external drive of the signal.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
$t_{d(HA-B)}$	Delay time, $\overline{HOLDA}$ low to $\overline{XBR}$ low#	0#		ns
$t_{d(I-XS)}$	Delay time, $\overline{IAQ}$ low to $\overline{XSTRB}$ low#	0#		ns
$t_{su(XA)}$	Setup time, Xaddress valid before $\overline{XSTRB}$ low	15		ns
$t_{su(XD)W}$	Setup time, Xdata valid before $\overline{XSTRB}$ low	15		ns
$t_{h(WD)W}$	Hold time, Xdata hold after $\overline{XSTRB}$ low	15		ns
$t_{h(XA)W}$	Hold time, write Xaddress hold after $\overline{XSTRB}$ low	15		ns
$t_{w(XSL)}$	Pulse duration, $\overline{XSTRB}$ low	45		ns
$t_{w(XSH)}$	Pulse duration, $\overline{XSTRB}$ high	45		ns
$t_{su(XS)RW}$	Setup time, R/$\overline{W}$ valid before $\overline{XSTRB}$ low	20		ns
$t_{h(XA)R}$	Hold time, read Xaddress after $\overline{XSTRB}$ high	0		ns

$\overline{XBR}$, XR/$\overline{W}$, and $\overline{XSTRB}$ lines should be pulled up with a 10-kΩ resistor to assure that they are in an inactive (high) state during the transition period between the SMJ320C50A driving them and the external circuit driving them.
NOTE 2. X preceding a name refers to the external drive of the signal.

EXTERNAL DMA



† A15 – A0, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, and $\overline{BR}$ timings are all included in timings referenced as address bus/control signals.

Figure 13. External DMA Timing

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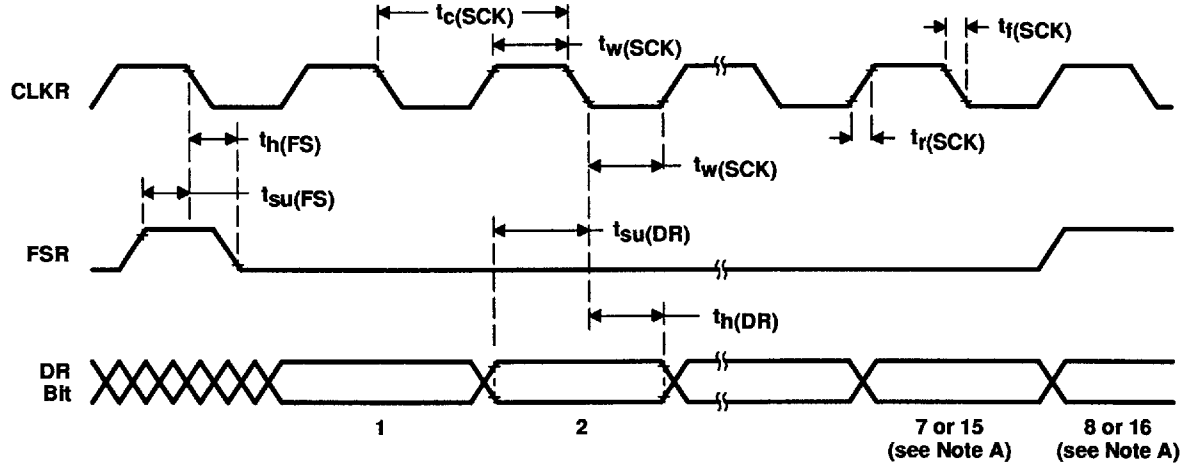
SERIAL-PORT RECEIVE

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = $0.5t_{c(CO)}$]

	PARAMETER	MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8‡	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8‡	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H		ns
$t_{su(FS)}$	Setup time, FSR before CLKR falling edge	10		ns
$t_{h(FS)}$	Hold time, FSR after CLKR falling edge	10		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	10		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	10		ns

† The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
‡ Values derived from characterization data and are not tested.



NOTE A: Depending on whether information is sent in an 8-bit or 16-bit packet.

Figure 14. Serial-Port Receive Timing

SERIAL-PORT TRANSMIT, EXTERNAL CLOCKS AND EXTERNAL FRAMES

switching characteristics over recommended operating conditions (see Note 3)

	PARAMETER	MIN	MAX	UNIT
$t_{d(DX)}$	Delay time, DX valid after CLKX rising		25	ns
$t_{dis(DX)}$	Disable time, DX valid after CLKX rising		40†	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising	−6		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = $0.5t_{c(CO)}$] (see Note 3)

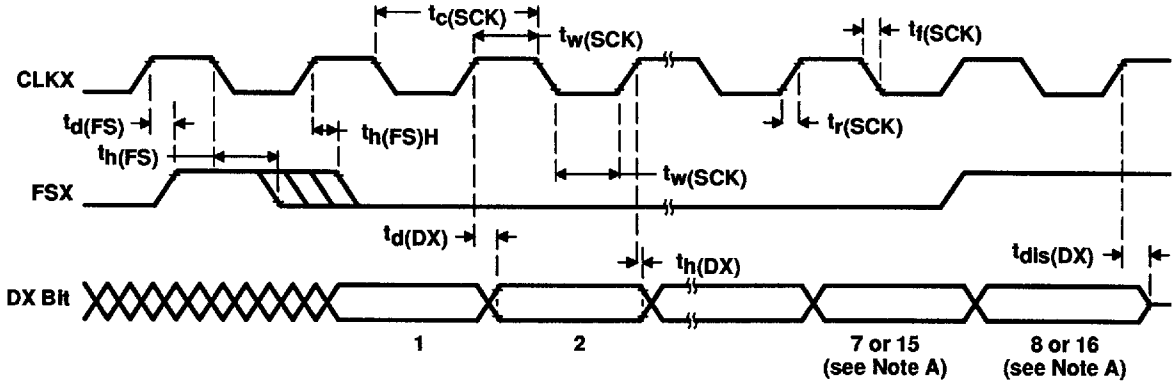
		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	‡	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8†	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8†	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H		ns
$t_{d(FS)}$	Delay time, FSX after CLKX rising edge		2H−8	ns
$t_{h(FS)}$	Hold time, FSX after CLKX falling edge	10		ns
$t_{h(FS)H}$	Hold time, FSX after CLKX rising edge		2H−8†§	ns

† Values derived from characterization data and are not tested.

‡ The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ If the FSX pulse does not meet this specification, the first bit of serial data will be driven on the DX pin until the falling edge of FSX. After the falling edge of FSX, data will be shifted out on the DX pin. The transmit-buffer-empty interrupt will be generated when the $t_{h(FS)}$ and $t_{h(FS)H}$ specification is met.

NOTE 3: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.



NOTE A: Depending on whether information is sent in an 8-bit or 16-bit packet.

Figure 15. Serial-Port Transmit Timing of External Clocks and External Frames

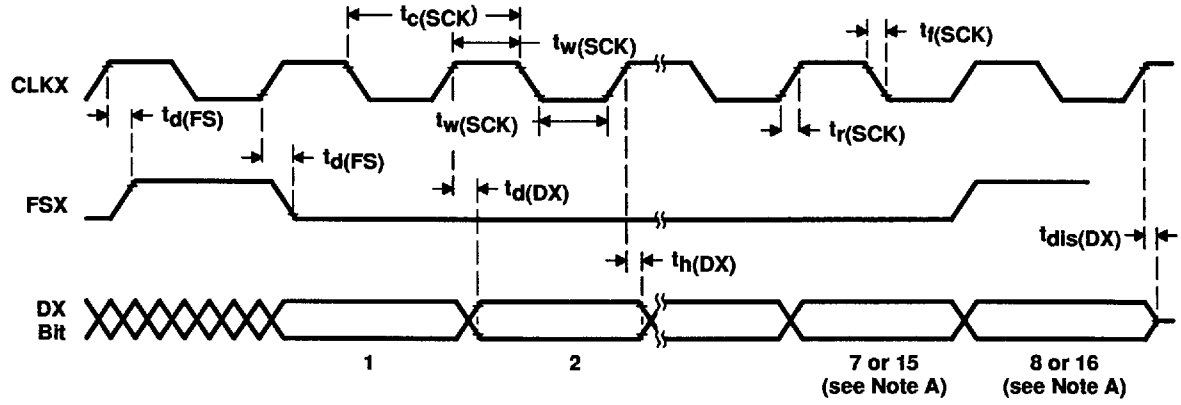
SERIAL-PORT TRANSMIT, INTERNAL CLOCKS AND INTERNAL FRAMES

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$] (see Note 3)

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{d(FS)}$	Delay time, CLKX rising to FSX			25	ns
$t_{d(DX)}$	Delay time, CLKX rising to DX			25	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX			40†	ns
$t_{c(SCK)}$	Cycle time, serial-port clock		8H		ns
$t_{f(SCK)}$	Fall time, serial-port clock		5		ns
$t_{r(SCK)}$	Rise time, serial-port clock		5		ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	4H - 20			ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising	- 6			ns

† Values derived from characterization and not tested.

NOTE 3: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX are always defined depending on the source of FSX, and CLKX timings are always dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.



NOTE A: Depending on whether information is sent in an 8-bit or 16-bit packet.

Figure 16. Serial-Port Transmit Timing of Internal Clocks and Internal Frames

SERIAL-PORT RECEIVE IN TDM MODE

timing requirements over recommended ranges of supply voltage and operating free-air temperature [H = 0.5$t_{c(CO)}$]

		MIN	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	†	ns
$t_{f(SCK)}$	Fall time, serial-port clock		8‡	ns
$t_{r(SCK)}$	Rise time, serial-port clock		8‡	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H		ns
$t_{su(LB)}$	Setup time, TDAT/TADD before TCLK rising	30		ns
$t_{h(LB)}$	Hold time, TDAT/TADD after TCLK rising	-5		ns
$t_{su(SB)}$	Setup time, TDAT/TADD before TCLK rising§	25		ns
$t_{h(SB)}$	Hold time, TDAT/TADD after TCLK rising§	0		ns
$t_{su(FS)}$	Setup time, TRFM before TCLK rising edge¶	10		ns
$t_{h(FS)}$	Hold time, TRFM after TCLK rising edge¶	10		ns

† The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.
‡ Values derived from characterization data and are not tested.
§ These parameters apply only to the first bits in the serial bit string.
¶ TFRM timing and waveforms shown in Figure 17 are for external TFRM. TFRM can also be configured as internal. The TFRM internal case is illustrated in the transmit timing diagram in Figure 18.

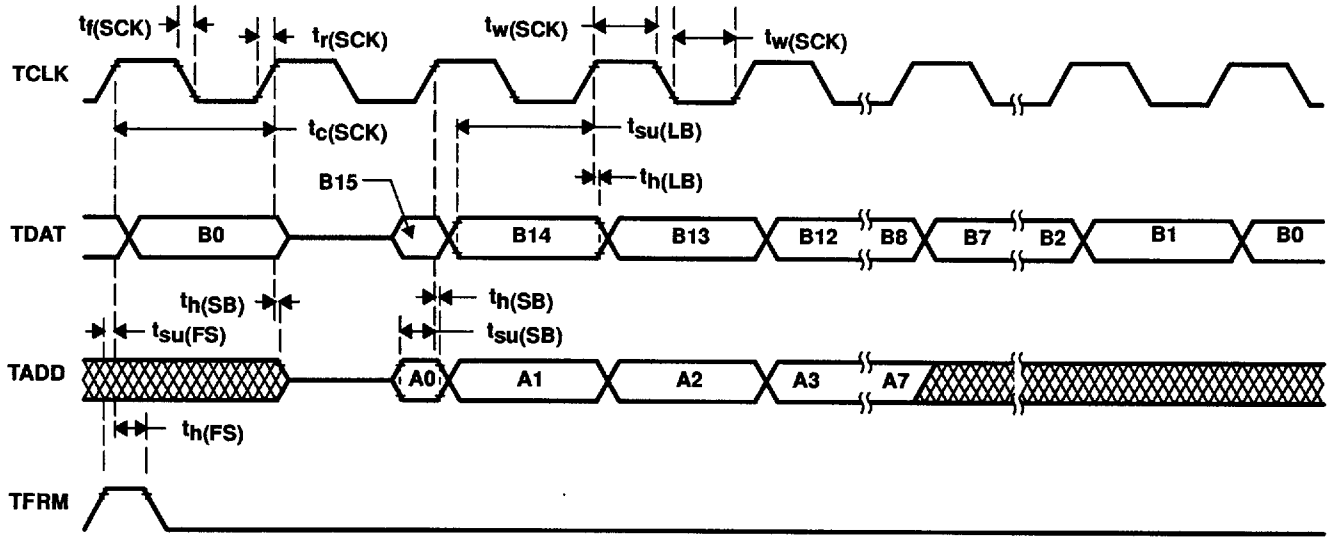


Figure 17. Serial-Port Receive Timing in TDM Mode

SERIAL-PORT TRANSMIT IN TDM MODE

switching characteristics over recommended operating conditions [H = 0.5$t_{c(CO)}$]

	PARAMETER	MIN	MAX	UNIT
$t_{h(AD)}$	Hold time, TDAT/TADD valid after TCLK rising	−2		ns
$t_{d(FS)}$	Delay time, TFRM valid after TCLK rising†	H	3H+10	ns
$t_{d(AD)}$	Delay time, TCLK to valid TDAT/TADD		25	ns

† TFRM timing and waveforms shown in Figure 18 are for internal TFRM. TFRM can also be configured as external, and the TFRM external case is illustrated in the receive timing diagram in Figure 17.

timing requirements over recommended ranges of supply voltage and operating free-air temperature [(H = 0.5$t_{c(CO)}$]

		MIN	TYP	MAX	UNIT
$t_{c(SCK)}$	Cycle time, serial-port clock	5.2H	8H‡	§	ns
$t_{f(SCK)}$	Fall time, serial-port clock			8¶	ns
$t_{r(SCK)}$	Rise time, serial-port clock			8¶	ns
$t_{w(SCK)}$	Pulse duration, serial-port clock low/high	2.1H			ns

‡ When SCK is generated internally.

§ The serial-port design is fully static and therefore can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

¶ Values derived from characterization data and are not tested.

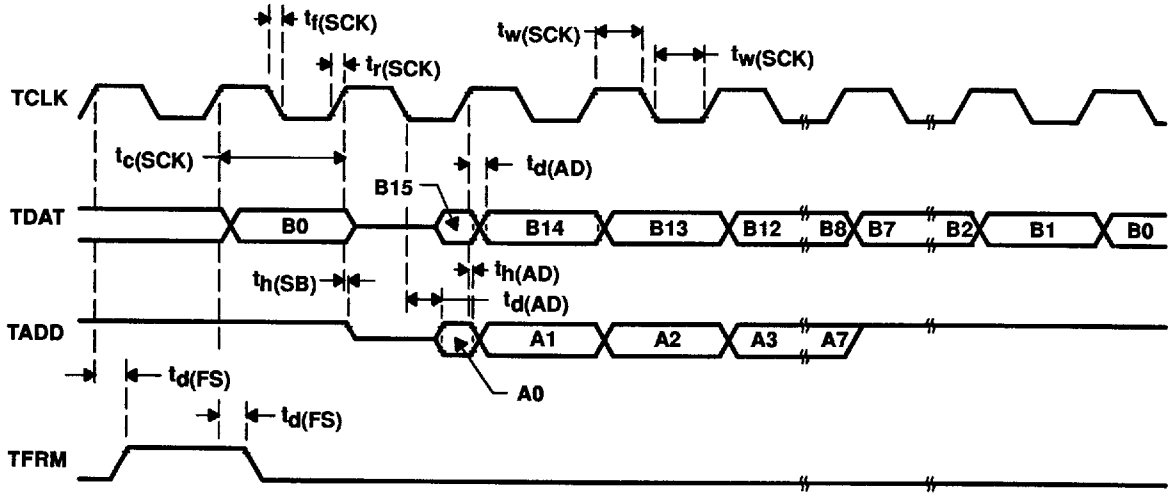
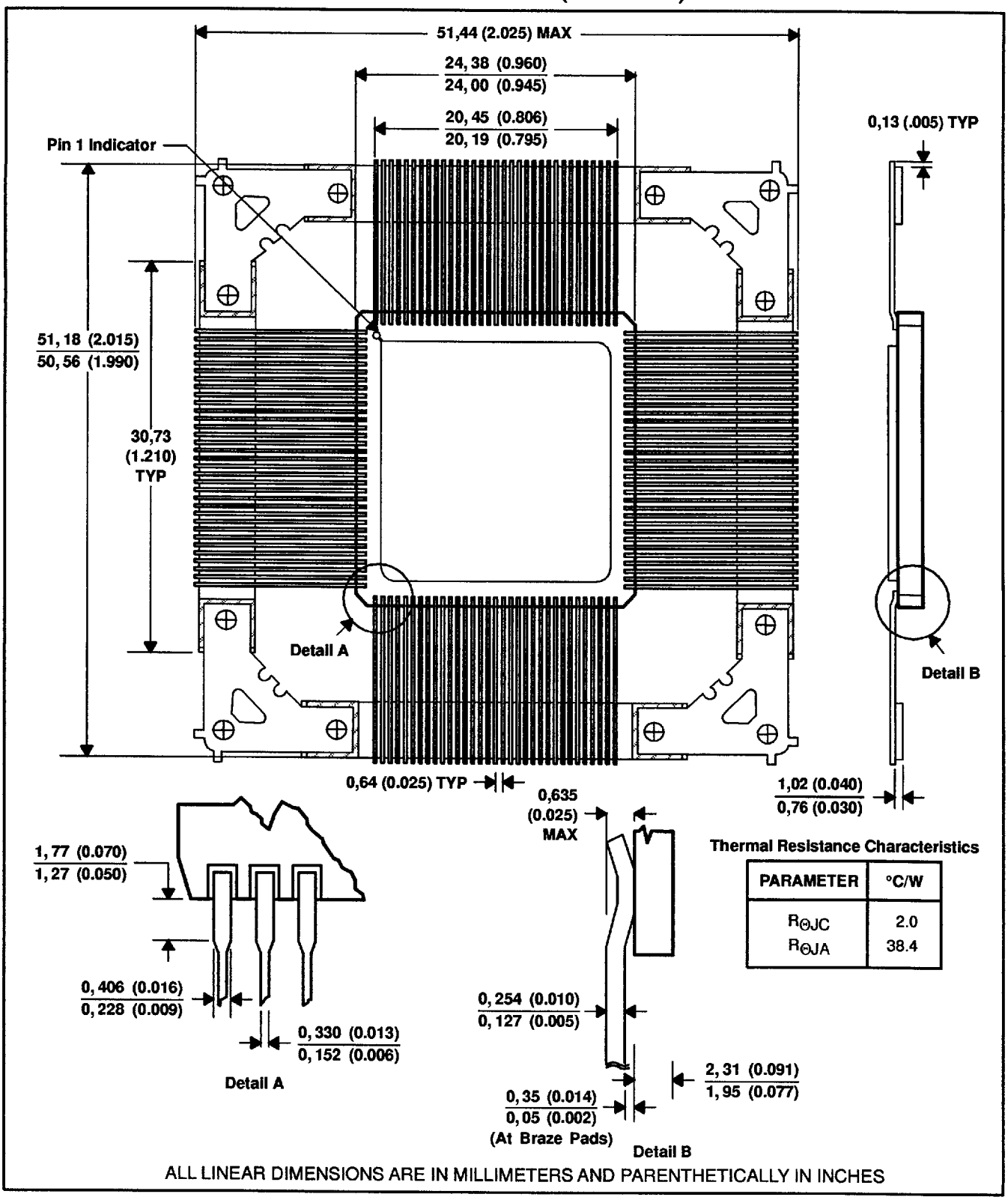


Figure 18. Serial-Port Transmit Timing in TDM Mode

MECHANICAL DATA

SMJ320C50 132-lead non-conductive ceramic tie bar (HFG suffix)



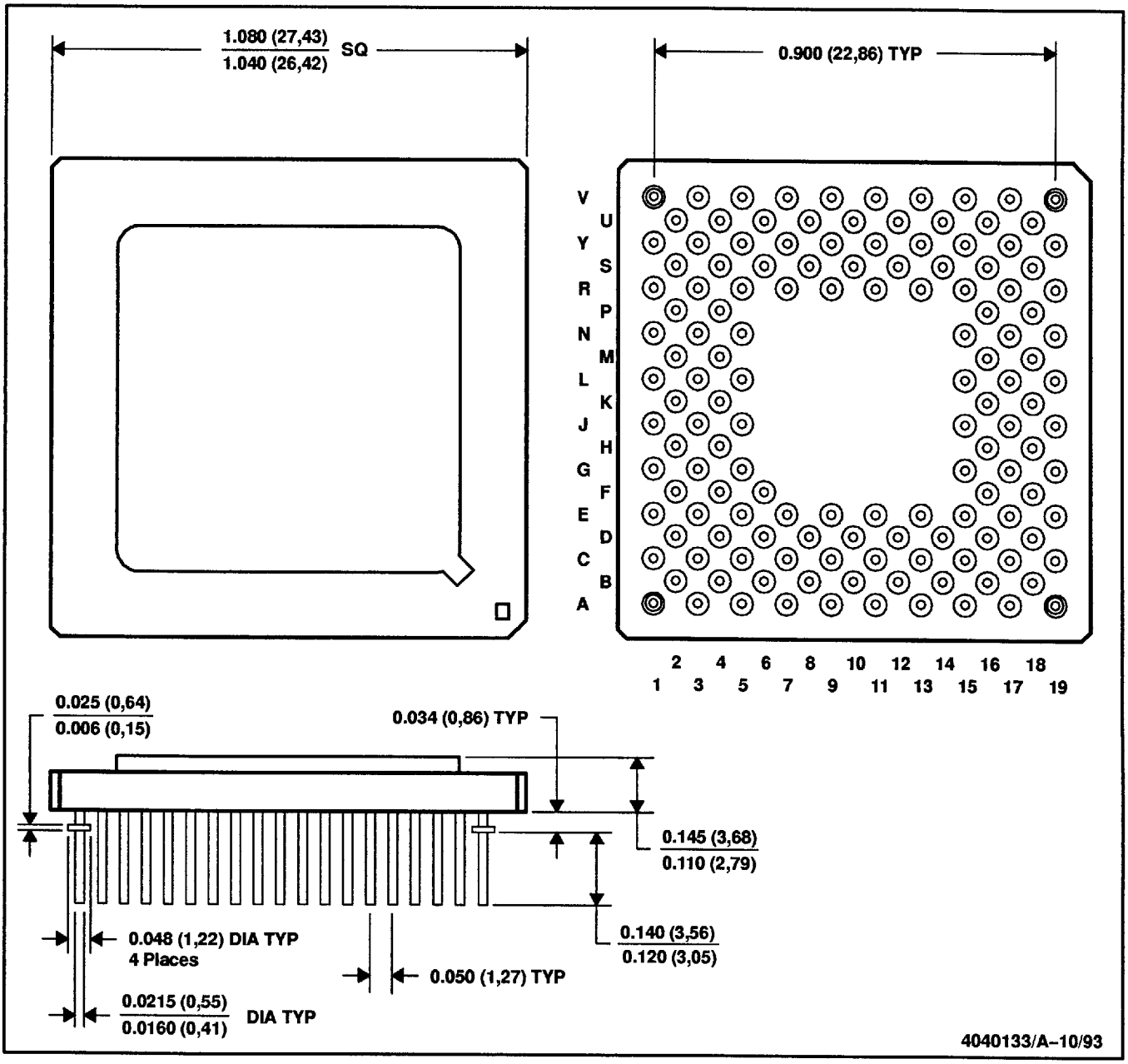
Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JC}$	2.0
$R_{\Theta JA}$	38.4

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

MECHANICAL DATA

GFA/S-CPGA1-P141 **SMJ320C31 CERAMIC PIN GRID ARRAY, CAVITY UP**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\Theta JC}$	1.0
$R_{\Theta JA}$	39.0

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