ASIC built-in analog front-end
BU9785KS

This is an ASIC chip with a built-in D/A, for modems that conform to V.34.
Customized to meet your requirements, this chip enables flexible D/A and D/A control and use of analog and digital lock interface.

●Applications
FAX/Data modem for PCs

●Features
1) A/D and D/A use a 16-bit 2nd-order Σ Δ converter.
2) Over-sampling A/D and D/A at 2,304kHz.
3) A/D has analog amplifier and pre-filter built in pre-stage ; D/A has smoothing filter and analog amplifier built in post-stage.
4) Sampling frequency range can be changed between 7,200Hz to 9,600 × 8/7Hz, when master frequency (MILK) is 2.304MHz.
5) An S/N ratio of 80dB can be achieved, at a sampling frequency of 11,000Hz and an analog power supply of 5V.
6) Built-in standard voltage generation circuit.
7) Analog interface with 1 differential input and 1 differential output.
8) 15,000 gate and 75 I/O pins built in.

●Absolute maximum. ratings (Ta=25℃)

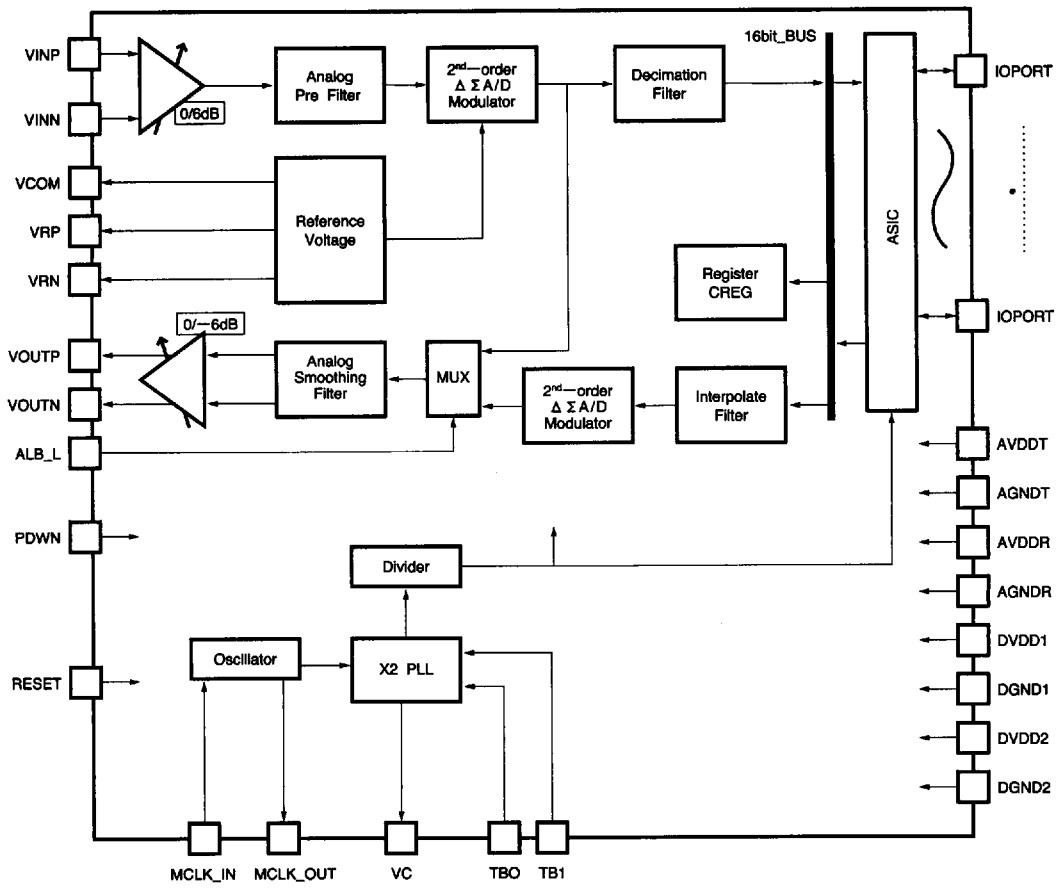
Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	0.3~7.0	V
Pin applied voltage	V_{IN}	GND−0.3~V_{DD}+0.3*	V
Power dissipation	Pd	500	mW
Storage temperature	Tstg	−55~125	℃

* Reduced by 5.0 mW for each increase in Ta of 1℃ over 25℃.
Note) Does not represent guaranteed performance

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	AVDD	4.75~5.25	V
	DVDD	3.15~3.45	
	LVDD	3.15~3.45	
Oscillation frequency	FCK	2.304	MHz
Operating temperature	Ta	0~70	℃

●Block diagram



●Pin descriptions

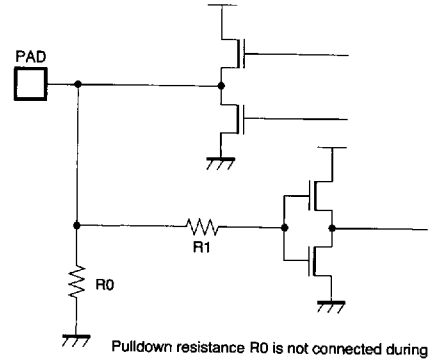
Pin No.	Signal Name	Function	Type
1	IOPORT00	ASIC I/O pin	LIO
2	IOPORT01		LIO
3	IOPORT02		LIO
4	IOPORT03		LIO
5	IOPORT04		LIO
6	IOPORT05		LIO
7	IOPORT06		LIO
8	IOPORT07		LIO
9	IOPORT08		LIO
10	IOPORT09		LIO
11	IOPORT10		LIO
12	IOPORT11		LIO
13	IOPORT12		LIO
14	IOPORT13		LIO
15	IOPORT14		LIO
16	IOPORT15		LIO
17	IOPORT16		LIO
18	IOPORT17		LIO
19	IOPORT18		LIO
20	IOPORT19		LIO
21	IOPORT20		LIO
22	IOPORT21		LIO
23	IOPORT22		LIO
24	IOPORT23		LIO
25	IOPORT24		LIO
26	IOPORT25		LIO
27	IOPORT26		LIO
28	IOPORT27		LIO
29	IOPORT28		LIO
30	VRP	Positive standard voltage output	BUFF
31	VRN	Negative standard voltage output	BUFF
32	VCOM	Standard voltage output	BUFF
33	nc		—
34	VINP	Differential amp positive input	INAMP
35	VINN	Differential amp negative input	
36	nc		—
37	nc		—
38	AVDDR	Power supply for analogue use (5.0V)	—
39	AVSSR	Receive GND for analogue use	—
40	VC	Externally attached condenser pin for PLL use	PLL
41	Nc		—
42	nc		—

Pin No.	Signal Name	Function	Type
43	nc		—
44	nc		—
45	AVDDT	Analog source power supply (5.0V)	—
46	AVSST	Analog source GND	—
47	nc		LIO
48	VOUTP	Output differential amplifier forward output	OUTAMP
49	VOUTN	Output differential amplifier reverse output	
50	DVSS2	Digital filter power supply (3.3V)	—
51	DVDD2	Digital filter GND	—
52	IOPORT28	ASIC logic I/O pins	LIO
53	IOPORT29		LIO
54	IOPORT30		LIO
55	IOPORT31		LIO
56	IOPORT32		LIO
57	IOPORT33		LIO
58	IOPORT34		LIO
59	IOPORT35		LIO
60	IOPORT36		LIO
61	IOPORT37		LIO
62	IOPORT38		LIO
63	IOPORT39		LIO
64	IOPORT40		LIO
65	IOPORT41		LIO
66	IOPORT42		LIO
67	IOPORT43		LIO
68	IOPORT44		LIO
69	IOPORT45		LIO
70	IOPORT46		LIO
71	IOPORT47		LIO
72	IOPORT48		LIO
73	IOPORT49		LIO
74	IOPORT50		LIO
75	IOPORT51		LIO
76	IOPORT52	ASIC I/O pins	LIO
77	IOPORT53		LIO
78	IOPORT54		LIO
79	IOPORT55		LIO
80	IOPORT56		LIO
81	IOPORT57		LIO
82	IOPORT58		LIO
83	IOPORT59		LIO
84	IOPORT60		LIO

Pin No.	Signal Name	Function	Type
85	IOPORT61	ASIC I/O pin	LIO
86	IOPORT62		LIO
87	IOPORT63		LIO
88	IOPORT64		LIO
89	DVDD1	Digital power supply for ASIC use (3.3V)	—
90	IOPORT65	ASIC I/O pin	LIO
91	DVSS1	Digital GND for ASIC use	—
92	IOPORT66	ASIC I/O pin	LIO
93	IOPORT67		LIO
94	IOPORT68		LIO
95	IOPORT69		LIO
96	IOPORT70		LIO
97	IOPORT71		LIO
98	IOPORT72		LIO
99	MCLK_IN	Crystal or master clock input	XTAL
100	MCLK_OUT	Crystal output	

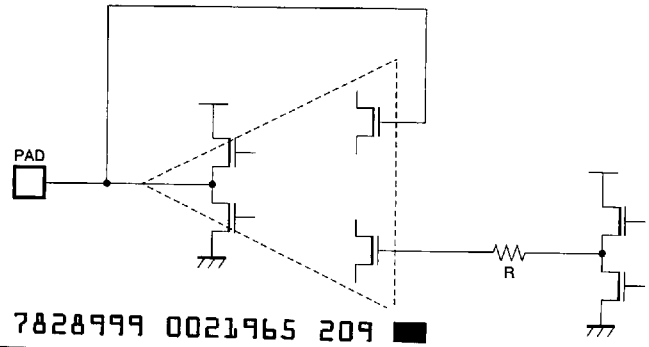
●Input/output circuit

Type : LIO

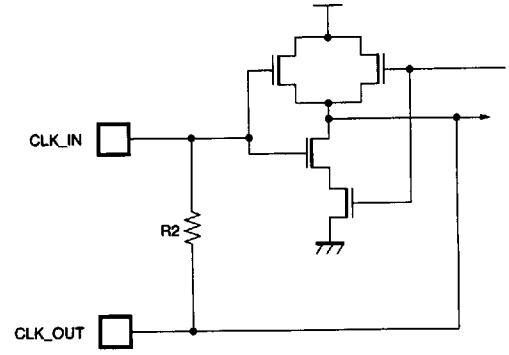


Pulldown resistance R0 is not connected during output.

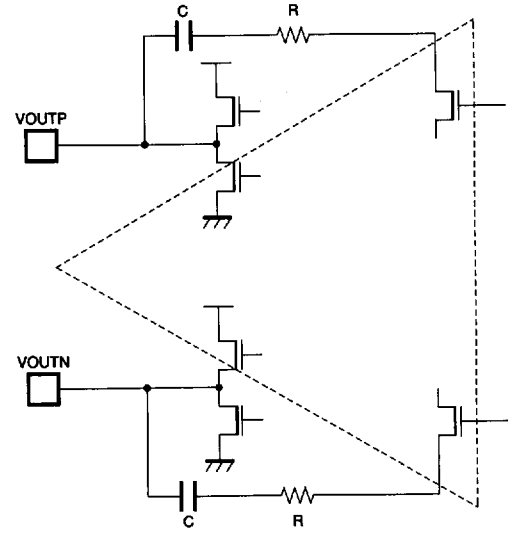
Type : BUFF



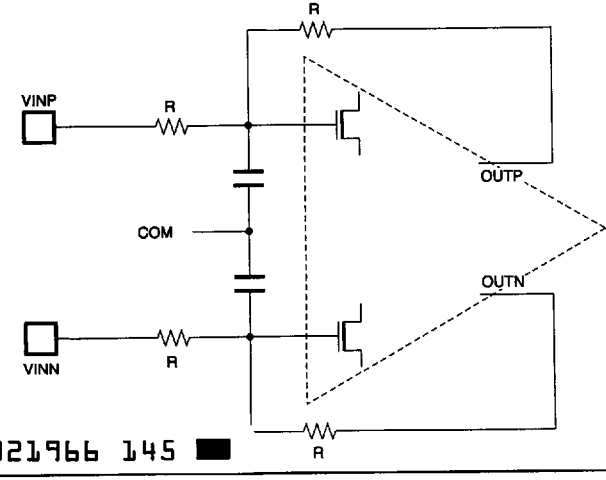
Type : XTAL



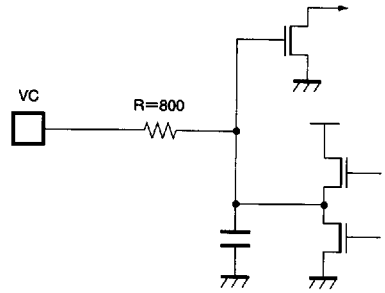
Type : OUTAMP



Type : INAMP



Type : PLL



●Electrical characteristics (unless otherwise specified : Ta=25℃, AV_{DD}=5.0V, DV_{DD}=3.3V)

DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current	I_{DD}	—	20	40	mA	MCLK=2.304MHz
	I_{DD_I}	—	0.1	0.2	mA	Power Down mode
<Digital interface>						
Input voltage (high)	V_{IH}	—	—	0.5	V	
Input voltage (low)	V_{IL}	2.8	—	—	V	
Input current (high)	I_{IH}	—	0	10	mA	VIN=DVDD
Input current (low)	I_{IL}	−10	0	—	mA	VIN=DGND
Output voltage (high)	V_{OH}	2.8	—	—	V	I load=1mA
Output voltage (low)	V_{OL}	—	—	0.5	V	I load=−1mA
Input capacitance	CN	—	5	10	pF	
<Analogue interface>						
Reference voltage output	VREF	−5%	2.5	+5%	V	Measure pin=VCOM
	VREFP	—	3.45	—	V	Measure pin=VRP
	VREFN	—	0.95	—	V	Measure pin=VRN
Reference voltage temperature conversion	TCO	—	200	—	ppm/℃	
Maximum differential input voltage	VDIFI	2XVREF			Vpp	
Input DC offset voltage	VOFFI	−100	0	100	mV	
Maximum differential output voltage	VDIFO	2XVREF			Vpp	
Output DC offset voltage	VOFFO	−100	0	100	mV	
Input resistance VINN VINP	RIN	100	—	—	kΩ	Measure pin=VINP, VINN
Output resistance VOUTN VOUTP	ROUT	—	—	20	Ω	Measure pin=VOUTP, VOUTN
Load resistance VOUTN VOUTP	RL	10	—	—	kΩ	Measure pin=VOUTP, VOUTN
Load capacitance VOUTN VOUTP	CL	—	—	20	pF	Measure pin=VOUTP, VOUTN

AC characteristics

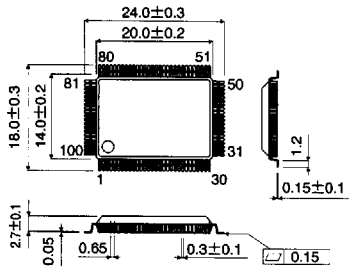
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<Master clock>						
Master clock input	MCLK	—	2.304	—	MHz	
Clock jitter	JIT	—	—	200	pS	
Duty	DUTY	45	50	55	%	
<Serial interface>						
Clock interval	twCK	—	868	—	nSec	
L clock bandwidth	twlCK	—	424	—	nSec	
H clock bandwidth	twhCK	—	424	—	nSec	
FS setup time	tfssu	100	—	—	nSec	
FS hold time	tsfh	100	—	—	nSec	
DIN setup time	tdisu	50	—	—	nSec	
DIN hold time	tdih	0	—	—	nSec	
DOUT effective time	tdov	—	—	20	nSec	
HCO & HCI setup time	thcsu	20	—	—	nSec	

Transmit/Receive Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<Transmission channel>						
Absolute gain	GABS	−0.5	0	0.5	dB	
Bandwidth ripple	RIPPL	—	±0.2	—	dB	
Total harmonic distortion	THD	—	−89	—	dB	
Dynamic range	DR	—	91	—	dB	
Power supply rejection ratio	PSSR	—	−50	—	dB	f=1kHz, Vac=200mVpp
Crosstalk	CTxRx	—	−90	—	dB	from Receive
<Reception channel>						
Absolute gain	GABS	−0.5	0	0.5	dB	
Bandwidth ripple	RIPPL	—	±0.2	—	dB	
Total harmonic distortion	THD	—	−89	—	dB	
Dynamic range	DR	—	91	—	dB	
Power supply rejection ratio	PSSR	—	−50	—	dB	f=1kHz, Vac=200mVpp
Crosstalk	CTxRx	—	−90	—	dB	from Transmit

Note: MCLK = 2.304MHz Oversampling ratio = 256
The measurement bandwidth is from DC to 0.425 X sampling cycles.

●External dimensions (Units: mm)



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