LATTICE

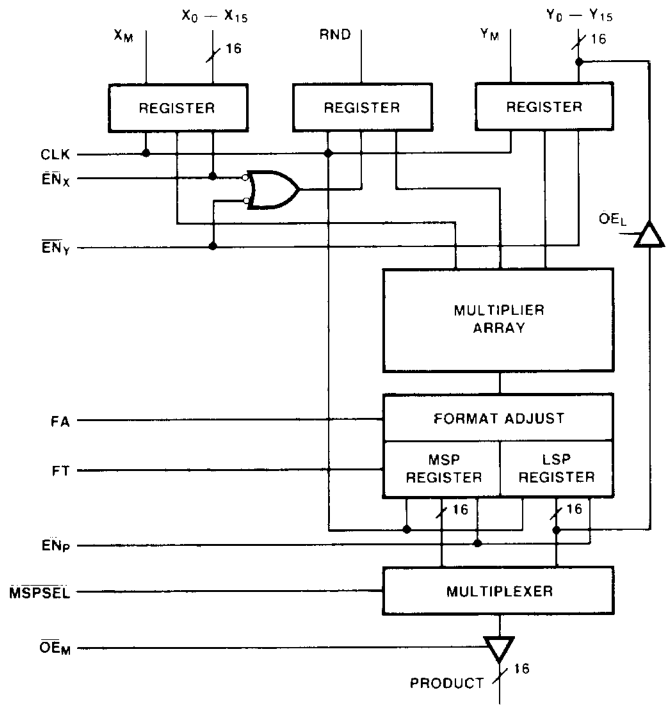
L1017

HIGH SPEED 16 x 16-BIT CMOS MULTIPLIER

FEATURES

- 16 x 16 MULTIPLIER — DOUBLE PRECISION PRODUCT
- HIGH SPEED MULTIPLY
  - — 45 ns Max Clocked Multiply Time
- LOW POWER CMOS TECHNOLOGY
  - — 550 mW Max (active)
  - — 550 μW Max (CMOS Standby)
- SIMPLE INTERFACE
  - — Single 5V $\pm$ 10% Supply
  - — TTL Compatible Inputs and Outputs
- ONE REGISTER CLOCK — SEPARATE ENABLES
- TWO'S COMPLEMENT AND UNSIGNED MAGNITUDE MULTIPLICATION
- PIN COMPATIBLE, HIGH PERFORMANCE REPLACEMENT FOR AMD 29517 AND IDT 7217L
- AVAILABLE IN DIP OR LCC PACKAGES

FUNCTIONAL BLOCK DIAGRAM



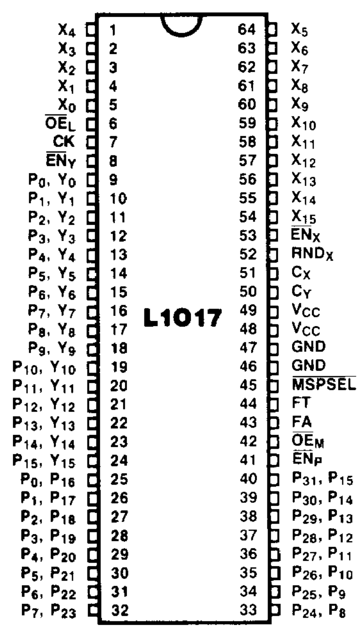
DESCRIPTION

The LATTICE L1017 devices are high performance 16 x 16 bit double precision multipliers. Designed with high speed logic techniques and a modified Booth's algorithm, the devices feature 45 ns, 65 ns, and 90 ns clocked multiply times. These devices offer a performance upgrade and are pin compatible with industry standard multipliers like the AM29517A.

UltraMos™, LATTICE's high performance CMOS technology, provide the multipliers with an active power dissipation of 550 mW maximum and a low CMOS standby power consumption of 550 μW maximum.

The L1017 multipliers generate a 32-bit product from two 16-bit input busses. Internal registers feature separate enable controls with a single common clock. The input data on each port can be individually specified as unsigned magnitude or two's complement, by controlling the state of the C_X and C_Y mode lines. The most significant half of the product (MSP) is available on the 16-bit output port. The least significant half (LSP) is multiplexed with the MSP and can be accessed at the 16-bit output port and the Y operand input port.

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
C_{TERM}	Terminal Voltage with Respect to GND(2)	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($T_A = 0°C$ to $+70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $125°C$)

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL MAX.	MILITARY MIN.	MILITARY MAX.	UNIT
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to V_{CC}	—	2	—	10	μA
$\|I_{LO}\|$	Output Leakage Current	High Z, V_{CC} = max., V_{OUT} = 0 to V_{CC}	—	2	—	10	μA
I_{CC}(1)	Operating Power Supply Current	Output Open	—	100	—	120	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	30	—	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC} - .2V$ or $\leq .2V$	—	.1	—	.1	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −0.4 mA	2.4	—	2.4	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA	—	0.5	—	0.5	V

1. I_{CC} is measured at clock cycle = 10 mhz and V_{IN} = TTL voltages.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE ($T_A = 25°C$, f = 1.0 MHZ)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: This parameter is sampled and not 100% tested.

TEST LOADS

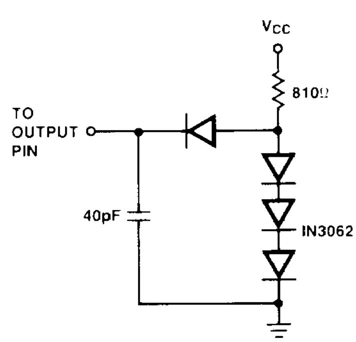


Figure 1. A.C. Output Test Load

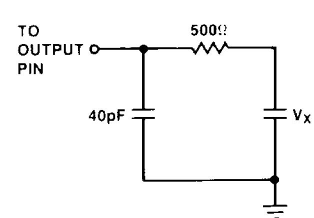


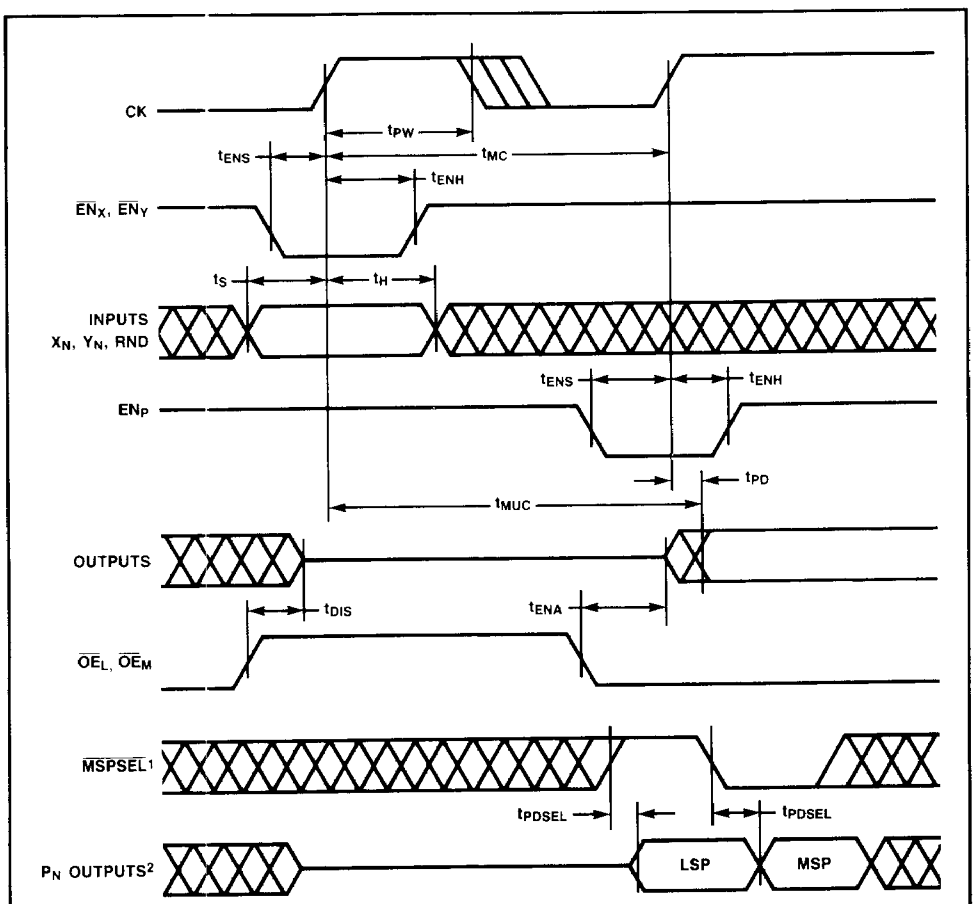
Figure 2. Output Three State Delay Load
V_x = 0V or 2.6V

AC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0°C$ to $70°C$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $125°C$)

SYMBOL	PARAMETER	L1017-45 MIN.	L1017-45 MAX.	L1017-65 MIN.	L1017-65 MAX.	L1017-90 MIN.	L1017-90 MAX.	UNITS
t_{MUC}	Unclocked Multiply Time	—	65	—	95	—	120	ns
t_{MC}	Clocked Multiply Time	—	45	—	65	—	90	ns
t_S	X, Y, RND Setup Time	15	—	20	—	25	—	ns
t_H	X, Y, RND Hold Time	0	—	0	—	0	—	ns
t_{ENA}	3 State Enable Time	0	20	0	30	0	30	ns
t_{DIS}	3 State Disable Time	0	20	0	30	0	30	ns
t_{PW}	Clock Pulse Width	15	—	20	—	25	—	ns
t_{PD}	Output Clock to Valid Data	—	20	—	30	—	30	ns
t_{PDSEL}	Output Control to Valid Data	—	20	—	30	—	30	ns
t_{ENS}	Register Enable Set-up Time	10	—	15	—	20	—	ns
t_{ENH}	Register Enable Hold Time	0	—	0	—	0	—	ns

TIMING DIAGRAM



1. A Transition of $\overline{MSPSEL}$ is not required during any cycle, and in some applications it can be grounded.
2. The order of appearance of the LSP and MSP on the output bus is determined by the logic level sequence of $\overline{MSPSEL}$.

SIGNAL DESCRIPTIONS

X_0 — X_{15} The 16 multipicand data inputs.

Y_0 — Y_{15} The 16 multiplier data inputs. These inputs are time-multiplexed with the least significant product (LSP) outputs.

P_0 — P_{15} The LSP output term. These 16 bits are time-multiplexed with the Y_0 — Y_{15} multiplier inputs or can be accessed from the output port under control of the MSPSEL line.

P_{16} — P_{31} The most significant product (MSP) term output port, comprising the 16 most significant bits of the output. The LSP term can also be accessed from this output port under control of the MSPSEL line.

C_X, C_Y Mode controls for each X_N and Y_N input. When LOW, the controlled input is unsigned data, and when HIGH, the input is 2's complement.

RND This is the round control for the MSP. When active, the L1017 adds 1 to the most significant bit of the LSP, rounding the MSP upward.

CK This is the register clock that is directed to all internal registers. In addition to the inputs, the mode control bits (C_X, C_Y), the RND bit and the output registers are latched with this signal.

ENX, ENY, ENP These are the register enable signals. ENX enables the multipicand (X) input register and it's input mode control bit. ENY does the same for the multiplier (Y) inputs. Either ENX or ENY enable the RND register. ENP enables the output register. Once a register is enabled, it will updated on the next rising edge of the clock (CK).

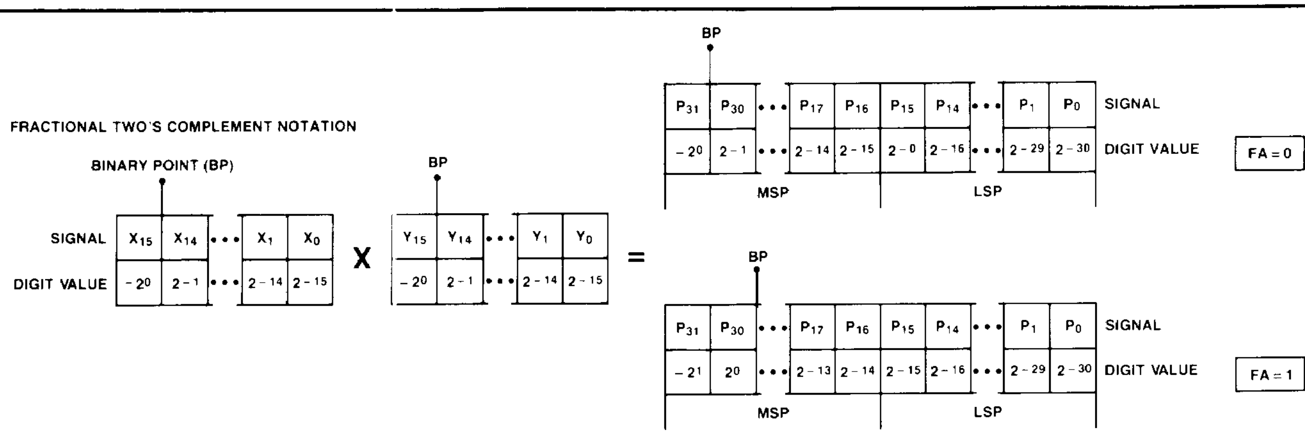
FT Flow-through control. When active (HIGH), the output registers of the LSP and MSP are in transparent or flow-through mode.

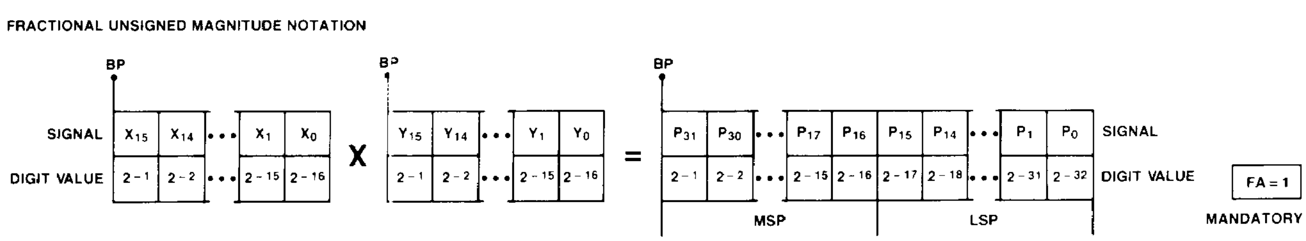
OE_L, OE_M Three-state output enable controls for the LSP and MSP.

MSPSEL Controls the output multiplexer which presents either MSP or LSP terms to the P_{16} — P_{32} output port.

FA Format adjust control. In 2's complement arithmetic, if FA is HIGH, a full 32-bit product is produced with a sign bit in the MSP. If FA is LOW, the sign value of the product is replicated in the most significant bits of the LSP and MSP. In integer or mixed mode, FA must be HIGH to get a valid product, and the most significant bit of the product contains the sign bit if the output is in 2's complement.

DATA FORMATS





INTEGER TWO'S COMPLEMENT NOTATION

X (BP after X_0):

SIGNAL	X_{15}	X_{14}	• • •	X_1	X_0
DIGIT VALUE	-2^{15}	2^{14}	• • •	2^1	2^0

X

Y (BP after Y_0):

SIGNAL	Y_{15}	Y_{14}	• • •	Y_1	Y_0
DIGIT VALUE	-2^{15}	2^{14}	• • •	2^1	2^0

=

P (BP after P_0), FA = 0 MANDATORY:

SIGNAL	P_{31}	P_{30}	• • •	P_{17}	P_{16}	P_{15}	P_{14}	• • •	P_1	P_0
DIGIT VALUE	-2^{30}	2^{29}	• • •	2^{16}	2^{15}	-2^{30}	2^{14}	• • •	2^1	2^0
	MSP					LSP				

P (BP after P_0), FA = 1 MANDATORY:

SIGNAL	P_{31}	P_{30}	• • •	P_{17}	P_{16}	P_{15}	P_{14}	• • •	P_1	P_0
DIGIT VALUE	-2^{31}	2^{30}	• • •	2^{17}	2^{16}	2^{15}	2^{14}	• • •	2^1	2^0
	MSP					LSP				

INTEGER UNSIGNED MAGNITUDE NOTATION

X (BP after X_0):

SIGNAL	X_{15}	X_{14}	• • •	X_1	X_0
DIGIT VALUE	2^{15}	2^{14}	• • •	2^1	2^0

X

Y (BP after Y_0):

SIGNAL	Y_{15}	Y_{14}	• • •	Y_1	Y_0
DIGIT VALUE	2^{15}	2^{14}	• • •	2^1	2^0

=

P (BP after P_0), FA = 1 MANDATORY:

SIGNAL	P_{31}	P_{30}	• • •	P_{17}	P_{16}	P_{15}	P_{14}	• • •	P_1	P_0
DIGIT VALUE	2^{31}	2^{30}	• • •	2^{17}	2^{16}	2^{15}	2^{14}	• • •	2^1	2^0
	MSP					LSP				

INTEGER MIXED MODE NOTATION

X (TWO'S COMPLEMENT) (BP after X_0):

SIGNAL	X_{15}	X_{14}	• • •	X_1	X_0
DIGIT VALUE	-2^{15}	2^{14}	• • •	2^1	2^0

X

Y (UNSIGNED MAGNITUDE) (BP after Y_0):

SIGNAL	Y_{15}	Y_{14}	• • •	Y_1	Y_0
DIGIT VALUE	2^{15}	2^{14}	• • •	2^1	2^0

=

P (BP after P_0), FA = 1:

SIGNAL	P_{31}	P_{30}	• • •	P_{17}	P_{16}	P_{15}	P_{14}	• • •	P_1	P_0
DIGIT VALUE	-2^{31}	2^{30}	• • •	2^{17}	2^{16}	2^{15}	2^{14}	• • •	2^1	2^0
	MSP					LSP				

FRACTIONAL MIXED MODE NOTATION

X (TWO'S COMPLEMENT) (BP after X_{15}):

SIGNAL	X_{15}	X_{14}	• • •	X_1	X_0
DIGITAL VALUE	-2^{0}	2^{-1}	• • •	2^{-14}	2^{-15}

X

Y (UNSIGNED MAGNITUDE) (BP before Y_{15}):

SIGNAL	Y_{15}	Y_{14}	• • •	Y_1	Y_0
DIGITAL VALUE	2^{-1}	2^{-2}	• • •	2^{-15}	2^{-16}

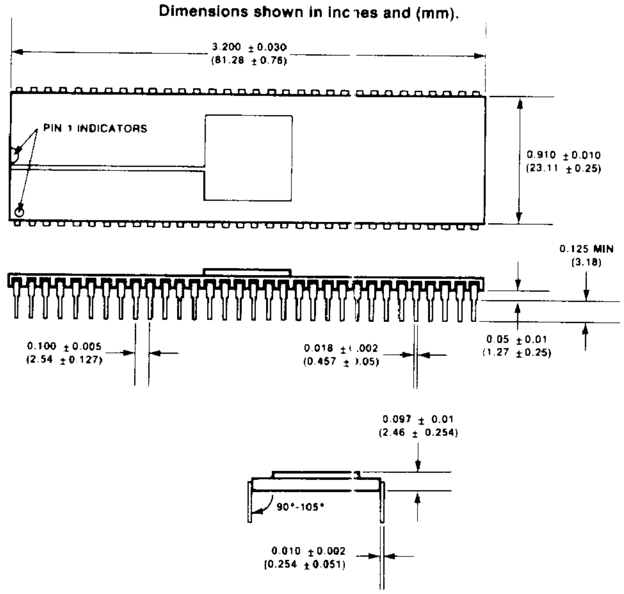
=

P (BP after P_{31}), FA = 1 MANDATORY:

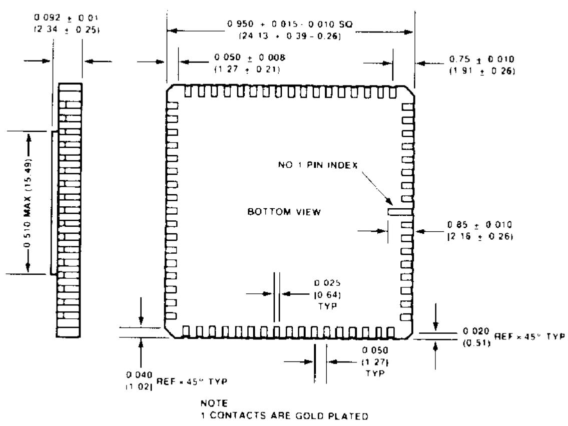
SIGNAL	P_{31}	P_{30}	• • •	P_{18}	P_{17}	P_{16}	P_{15}	• • •	P_1	P_0
DIGIT VALUE	-2^{0}	2^{-1}	• • •	2^{-13}	2^{-14}	2^{-15}	2^{-16}	• • •	2^{-30}	2^{-31}
	MSP					LSP				

PACKAGE INFORMATION

64-PIN HERMETICALLY SEALED
DUAL IN-LINE PACKAGE
Dimensions shown in inches and (mm).

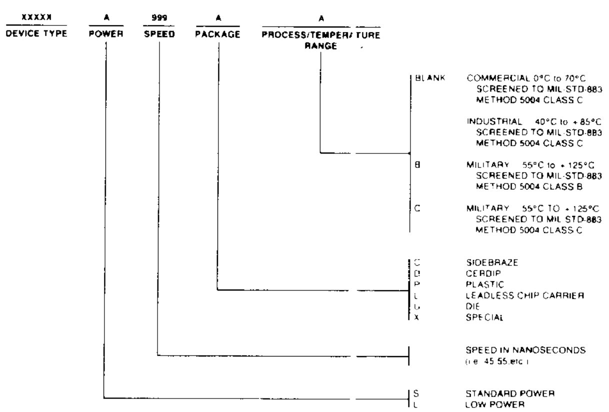


68-TERMINAL LEADLESS CHIP CARRIER
Dimensions shown in inches and (mm).



NOTE
1 CONTACTS ARE GOLD PLATED

ORDERING INFORMATION



LCC PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	V_{CC}	35	P_7, Y_7
2	GND	36	P_6, Y_6
3	GND	37	P_5, Y_5
4	$\overline{MSPSEL}$	38	P_4, Y_4
5	FT	39	P_3, Y_3
6	$\overline{FA}$	40	P_2, Y_2
7	$\overline{OE}_M$	41	P_1, Y_1
8	$\overline{EN}_P$	42	P_0, Y_0
9	N/C	43	N/C
10	P_{31}, P_{15}	44	EN_Y
11	P_{30}, P_{14}	45	CK
12	P_{29}, P_{13}	46	OE_L
13	P_{28}, P_{12}	47	X_0
14	P_{27}, P_{11}	48	X_1
15	P_{26}, P_{10}	49	X_2
16	P_{25}, P_9	50	X_3
17	P_{24}, P_8	51	X_4
18	P_{23}, P_7	52	X_5
19	P_{22}, P_6	53	X_6
20	P_{21}, P_5	54	X_7
21	P_{20}, P_4	55	X_8
22	P_{19}, P_3	56	X_9
23	P_{18}, P_2	57	X_{10}
24	P_{17}, P_1	58	X_{11}
25	P_{16}, P_0	59	X_{12}
26	NC	60	NC
27	P_{15}, Y_{15}	61	X_{13}
28	P_{14}, Y_{14}	62	X_{14}
29	P_{13}, Y_{13}	63	X_{15}
30	P_{12}, Y_{12}	64	EN_X
31	P_{11}, Y_{11}	65	RND
32	P_{10}, Y_{10}	66	C_X
33	P_9, Y_9	67	C_Y
34	P_8, Y_8	68	V_{CC}