OCX961 Crosspoint Switch
Advanced Mini Data Sheet

Features

- 1.6 Gb/s port data bandwidth, >77Gb/s aggregate bandwidth
- Low power CMOS, 2.5V and 3.3V power supply
- SRAM-based, in-system programmable
- 96 configurable I/O ports
  - 48 dedicated differential input ports
  - 48 dedicated differential output ports
  - Supports LVPECL and LVDS I/O
  - LVTTL control interface
  - Output Enable control for all outputs
- Non-blocking switch matrix
  - Patented ActiveArray™ matrix for superior performance
  - Double-buffered configuration RAM cells for simultaneous global updates
  - ImpliedDisconnect™ function for single cycle disconnect/ connect
- Full Broadcast and multicast capability
  - One-to-One and One-to-Many connections
  - Special broadcast mode routes one input to all outputs at maximum data rate
- Low jitter and signal skew
- Low duty cycle distortion
- RapidConfigure™ parallel interface for configuration and readback
- Serial programming interface for configuration
- 304 BGA package with 1.27mm ball spacing
- Intergrated Termination Resistors

Description

The OCX961 SRAM-based device is a non-blocking *48 X 48* digital crosspoint switch capable of data rates of 1.6 Gigabits per second per port. The I/O ports are fixed as either input or output ports. The input and output ports operate in flow-through (asynchronous) mode.

The patented ActiveArray provides greater density, superior performance, and greater flexibility compared to a traditional *n:1* multiplexer architecture. The OCX™ devices support various operating modes covering one input to one output at a time as well as one input to many outputs, plus a special broadcast mode to program one input to all outputs while maintaining maximum data rates. In all modes data integrity and connections are maintained on all unchanged data paths.

The RapidConfigure parallel interface allows fast configuration of the Output Buffers and the switch matrix. Readback is supported for device test and verification purposes. The OCX961 also includes a JTAG-like serial interface for configuration of the device. A functional block diagram of the OCX961 is shown in Figure 1.

Applications

- SONET/SDH and DWDM
- Digital Cross-Connects
- System Backplanes and Interconnects
- High Speed Test Equipment
- ATM Switch Cores
- Video Switching

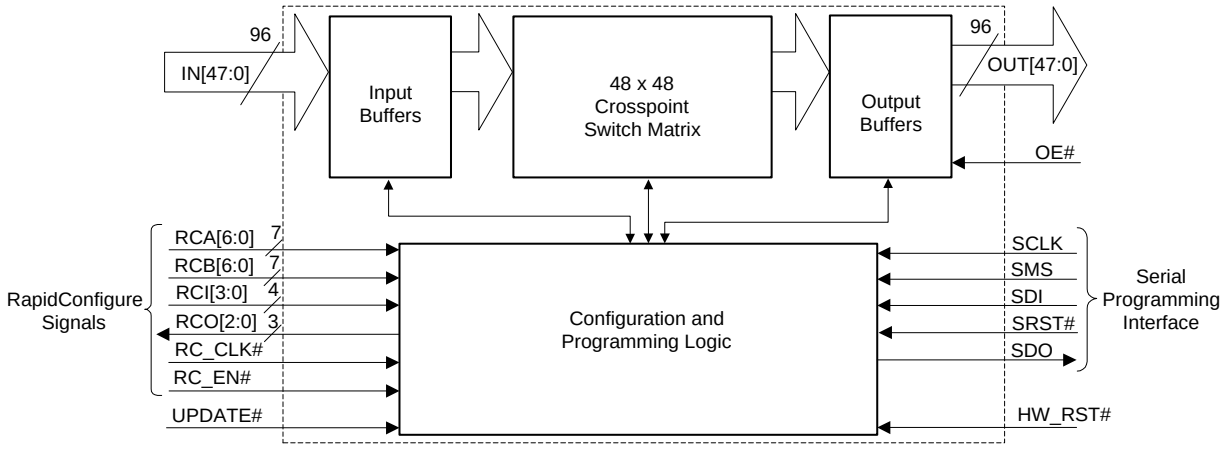

Figure 1 OCX961 Functional Block Diagram

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Tables

1. Introduction

The OCX961 is a differential crosspoint-switching device. The main functional block of the device is a Switch Matrix as shown in Figure 1. The Switch Matrix is a *x-y* structure supporting an input-to-output data flow. Figure 2 shows a conceptual view of the switch matrix with inputs connected to the horizontal trace and outputs to the vertical trace. Connections between vertical and horizontal lines are implemented with a proprietary high-performance buffering circuit. Signal path delays through the Switch Matrix are very well balanced, resulting in predictable and uniform pin-to-pin delays.

Note – For the purpose of clarity, the logic diagrams within this data sheet are conceptual representations only and do not show actual circuit implementation.

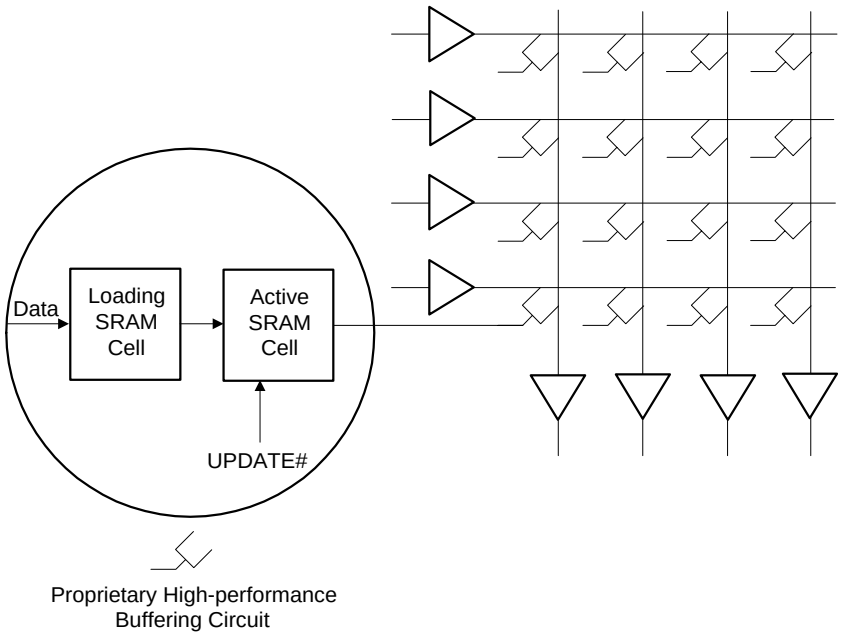


Figure 2 OCX961 Switch Matrix

The Active SRAM cells are responsible for establishing connections in the switch matrix by turning on the interconnect circuit, while the Loading SRAM cell can be used to store a second configuration that can be transferred to the Active SRAM cell at a later time. The two SRAM cells are arranged so that a double buffered scheme can be employed. Through the use of an internal signal (generated automatically during a programming cycle) it is possible to store a second configuration map in the Loading SRAM while the Active SRAM maintains its present connection status. When the UPDATE# signal is asserted low, the contents of the Loading SRAM cell are transferred to the Active SRAM cell and the switch matrix connection is either made or broken.

The UPDATE# signal can be used to control when the switch matrix is reconfigured. For instance, as long as the UPDATE# signal is asserted high, the Loading SRAM cells for the entire switch matrix could be changed without affecting the current configuration of the switch. When the UPDATE# signal is asserted low, the entire switch matrix would be reconfigured simultaneously. If the UPDATE# signal is asserted continuously, all crosspoint programming commands (generated by RapidConfigure or Serial programming cycles) will take effect immediately, since the Loading SRAM cell's contents will be transferred directly to the Active SRAM cell.

1.1 Input and Output Buffers

All of the I/O buffers are differential with flow-through mode. Figure 3 shows the basic block diagram of the input and output blocks with the sources for the output control signals (OE#). The control signals are explained in more details in the following sections.

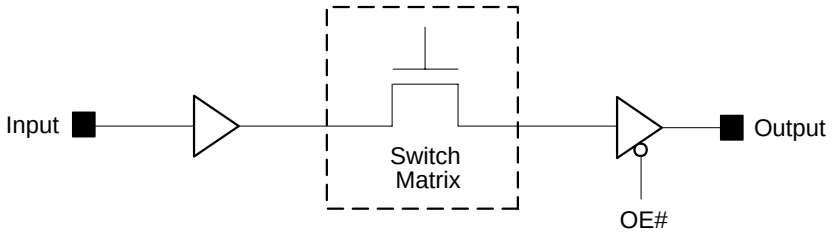


Figure 3 Input and Output Buffer Configuration

1.1.1 Input and Output Port Function Mode

The following legend describes the various modes of the Input and Output Ports and the specification used by the OCXPro™ Software.

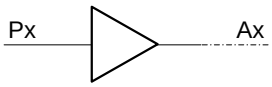
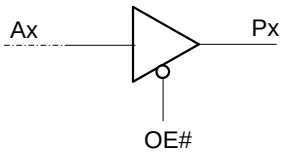
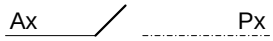
Legend:

Ax–Switch Matrix Signal

Px–Port Signal

OE#–Output Enable (# means “Active Low”)

Table 1 Summary for Programmable I/O Attributes for OCX961

Symbol	I/O Port Function	Mnemonic
	**Input** – The external signal is buffered from the Input Port pin to the corresponding Switch Matrix line.	**IN**
	**Output** – The internal signal is buffered from the corresponding Switch Matrix line to the Output Port pin. In this mode an optional output enable (OE#) can be selected. The default state is logic high with enable set to ON.	**OP**
	**No Connect** – In this mode, the output Port pin is isolated from the Switch Matrix.	**NC**

1.1.2 Broadcast Mode

The OCX961 has a special Broadcast Mode which connects any input to all outputs without performance degradation. The input is selected using RapidConfigure or Serial interface and disconnects all other inputs. The Global Update pin (UPDATE#) must be held high during Broadcast Mode. Asserting the UPDATE# pin returns the array to the previous program condition.

1.2 Output Control Signals

Every output port of the OCX961 has a global Output Enable signal (OE#). All output buffers have output enables that have programmable polarity and are individually configurable.

Additionally each output can be permanently enabled (always ON) or disabled (always OFF) which is useful for applications which need to tri-state outputs (for example when using multiple chips in expansion mode) or for power saving in designs that do not need to use all the outputs available.

Two control bits are used to control the function of the output enable.

1.3 RapidConfigure Interface

RapidConfigure (RC) is a 23 signal parallel interface that is used to program the OCX961 device. The 23 pins are allocated as follows:

RCA[6:0] = RapidConfigure Address A. RCA are input pins.

RCB[6:0] = RapidConfigure Address B. RCB are input pins.

RCI[3:0] = RapidConfigure Instruction Bits

RCO[2:0] = RapidConfigure Readback. RCO are output pins.

RC_CLK# = RapidConfigure Clock (negative edge clock)

RC_EN# = RapidConfigure Cycle Enable (active low)

1.3.1 RapidConfigure Programming Instructions

The RC interface supports both write and read types of operations:

1. Write Operations (reset crosspoint and Input or Output Buffer (IOB), configure an Output Buffer, connect/disconnect crosspoint)
2. Read Operations (Output Buffer and crosspoint configuration read).

Table 2 RapidConfigure Programming Instructions

RCI[3:0]	RCA[6:0]	RCB[6:0]	RCO[2:0]	Instruction	Description
0000				Reserved	
0001				Reserved	
0010	X	X		Reset Crosspoint Array	Reset, along with an Update operation (UPDATE# pin or Update command) resets the entire crosspoint array to no connect. All Output Buffers remain unchanged by this operation.
0011	X	Input Port Address		Set Array to Broadcast mode	Connects the input selected by RCB[6:0] to all output ports and disconnects all other inputs. The Global Update (UPDATE#) pin must be held high during Broadcast mode. Activating the Global Update pin returns the array to the previous program condition.
0100	Output Port Address	Data		Configure an Output Buffer	Program an Output Buffer specified by RCA[6:0]. See Table 4 for RCB[6:0] bit assignment and buffer functionality.

Table 2 RapidConfigure Programming Instructions *(Continued)*

RCI[3:0]	RCA[6:0]	RCB[6:0]	RCO[2:0]	Instruction	Description
0101				Readback Crosspoint, Output Buffer status	This is a two-cycle instruction.
Cycle 1	Output Port Address	Input Port Address	X		Specify the crosspoint connect status at input location specified by RCA[6:0] to the output location specified by RCB[6:0].
Cycle 2	X	X	Output Data		Readback (using RCO[2:0]) the status of the input buffer specified in Cycle 1 by RCA[6:0], the output buffer specified in Cycle 1 by RCO[2:0] and the crosspoint connect status. See Table 3 for RCO[2:0] readback pin assignment.
0110	X	X		Update	Program the Global Update function without the use of the UPDATE# pin.
0111	X	Input Port Address		Disconnect Input	Disconnect the crosspoint cells of the input row location specified by RCA[6:0].
1000	Output Port Address	Input Port Address		Disconnect Input and Output	Disconnect the crosspoint cell at the input location specified by RCA[6:0] to the output location specified by RCB[6:0]. All other connections from the source input address or to the same output address remain the same as before.
1001	Output Port Address	Input Port Address		Connect, with ImpliedDisconnect	Connect the crosspoint cell at the input location specified by RCA[6:0] to the output location specified by RCB[6:0]. All other connections from the same input address or to the same output address are set to no connect (NC).
1010	Output Port Address	Input Port Address		Connect, without ImpliedDisconnect	Connect the crosspoint cell at the input location specified by RCA[6:0] to the output location specified by RCB[6:0]. All other connections to the same output address are set to “no connect” while all other connections from the same input address remain the same as before.
1011				Reserved	
1100				Reserved	
1101	X	X		Reset All	Reset the switch matrix to no connects (NC). Update is forced internally. Sets the Output buffer to Flow-through mode with Output Enabled.
1110				Reserved	
1111				Reserved	

Note – X = Don’t care.

Table 3 RCO[2:0] Readback Pin Assignment

RCO[2:0]	Readback Location	Signal/Function
O2	Crosspoint	**Connection Status:** 0 = No connection (NC) — (default state at reset) 1 = Connected
O1, O0 0,0 0,1 1,0 1,1	Output Buffer	**Output Enable:** Output enabled (ON) – this is the default state at reset Output disabled (OFF) Output controlled by OE (active high) Output controlled by OE# (active low)

Table 4 Programming an Output Buffer using RapidConfigure

RCB[6:0]	Signal/Function
B6, B5, B4, B3, B2	Don’t care
B1, B0 0,0 0,1 1,0 1,1	**Output Enable:** Output enabled (ON) – this is the default state at reset Output disabled (OFF) Output controlled by OE (active high) Output controlled by OE# (active low)

1.4 Serial Interface Configuration Controller

The Output port attributes and the Switch Matrix connections can be programmed using the serial bus. The RapidConfigure Interface can be enabled or disabled using the serial bus.

The serial interface mode is always available for configuration regardless of whether the RapidConfigure mode is enabled or disabled. However, proper care must be taken when switching between Serial Interface and RapidConfigure for configuring the devices. Before attempting to change Switch Matrix connections or output port configuration through the Serial Interface, the user must first ensure that the RapidConfigure mode is disabled by using the Serial Interface serial mode to set the RCE bit to zero in the Mode Control Register.

1.4.1 Serial Interface

The dedicated Serial interface has five pins: Serial Data Out (SDO), Serial Mode Select (SMS), Serial Data In (SDI), Serial Reset (SRST#), and Serial Clock (SCLK), for device configuration and verification. The I-Cube supplied software will automatically generate the necessary bitstream from a higher-level textual description of the required configuration. Data on the SDI and SMS pins are clocked into the device on the rising edge of the SCLK signal, while the valid data appears on the SDO pin after the falling edge of SCLK. For more detailed information on Serial programming, refer to the *OCX Family Register Programming Manual.*

1.4.2 Output Port Configuration

Output port configuration is accomplished by loading the appropriate bitstream into the programming registers present at each Output port. The serial bus is used to load configuration data into the Output port programming registers, one Output port at a time.

1.4.3 Switch Matrix Configuration

The contents of the SRAM cells controlling Switch Matrix connection can be modified using the Serial interface. This is accomplished by loading the configuration data, one word at a time, into the SRAM cells in the Switch Matrix.

1.4.4 Mode Control Register Configuration

The OCX961 contains a single bit Mode Control Register used to store user flags for RapidConfigure Enable (RCE). These are required for proper functioning of the device. The contents of this register can be changed using the Serial interface and a special Serial instruction.

Table 5 Mode Control Register

RCE	Mode
0	RapidConfigure interface disabled (OFF)
1	RapidConfigure interface enabled (ON)

1.4.5 Serial Interface Architecture

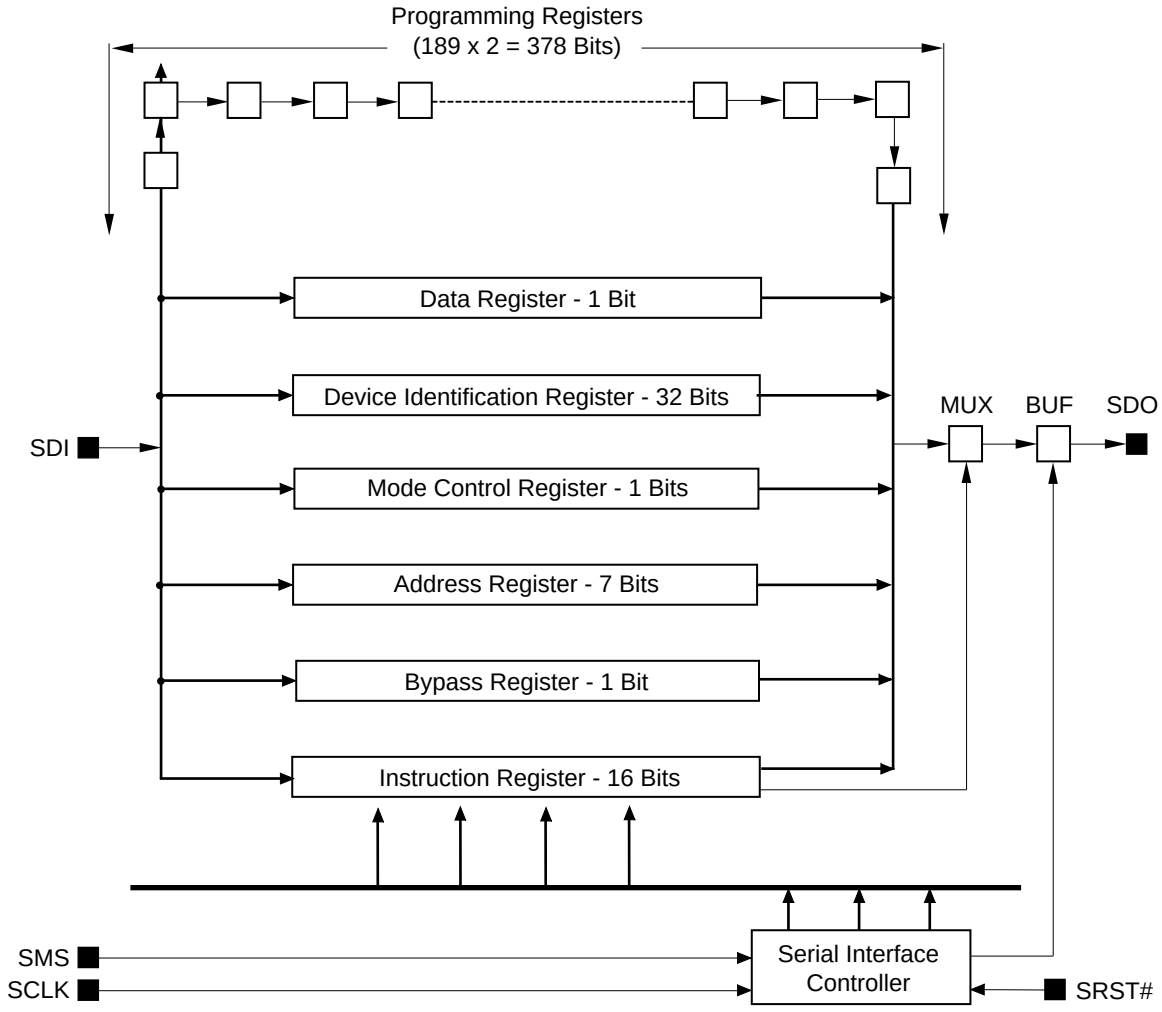


Figure 4 OCX961 Serial Interface Architecture

1.4.6 Serial Interface State Machine

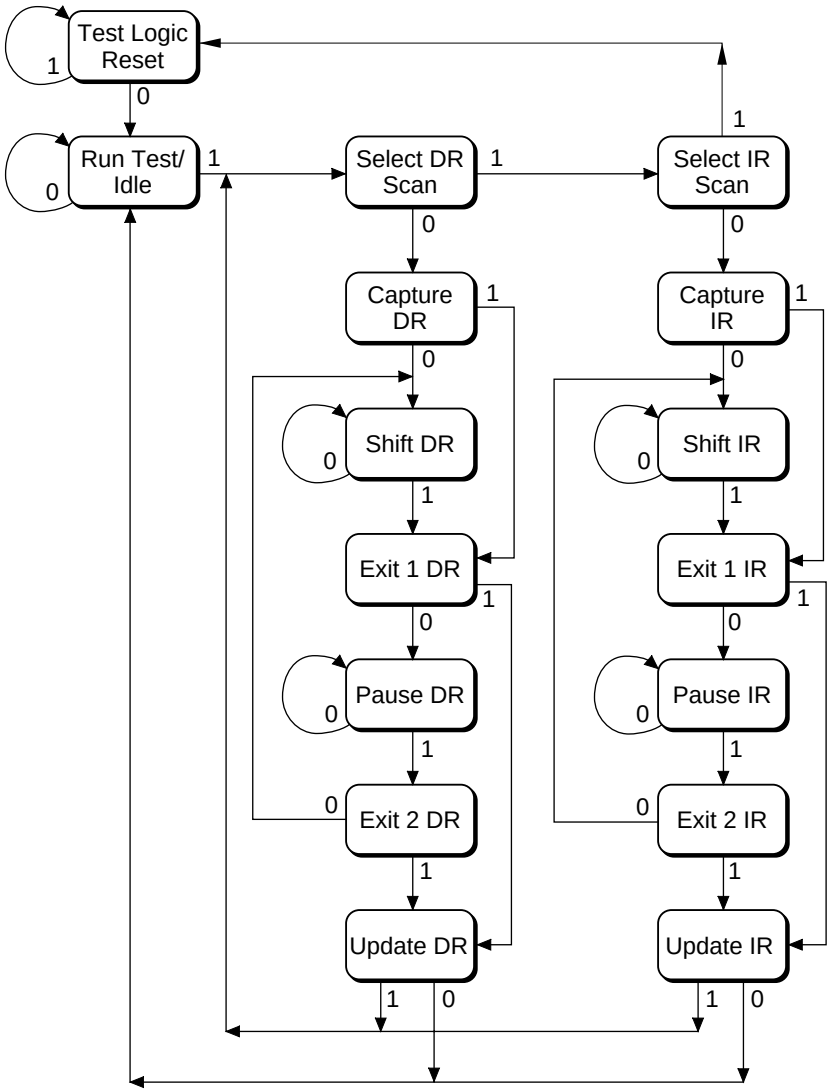


Figure 5 OCX961 Serial Interface State Machine

1.4.7 Serial Input Format

Table 6 Serial Input Format

	Instruction				Data					Address A						
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	I3	I2	I1	I0	BB	BA	B9	B8	B7	A6	A5	A4	A3	A2	A1	A0

1.4.8 Serial Interface Instructions

Table 7 Serial Interface Instructions

I [3:0]	BB	BA	B9	B8	B7	A6-A0	Instruction	Description
0 0 0 0	X	X	X	X	X	X	Sample/EXTEST	Places the device in scan mode.
0 0 0 1	X	X	X	X	X	X	Sample/EXTEST	Places the device in scan mode.
0 0 1 0	X	X	X	X	X	X	Reset the Crosspoint Array	Reset, along with an Update operation (UPDATE# pin or Update command) resets the entire Crosspoint Array to no-connect (B7 and B8 are not changed).
0 0 1 1	X	X	X	X	X	X	Set Array for Broadcast mode	Use the Address Register as the Input address to be the broadcast input. Connects the selected Input to all Output cells and disconnects all other Inputs. Activating the Global Update instruction returns the Crosspoint array from the Broadcast mode to the previous programed state.
0 1 0 0	X	X	X	OE	OE	Output Buffer Address	Program a Buffer	Programs the Output Buffer address specified in the Serial instruction (A6-A0). The configuration data is also specified in the Serial instruction bits BA-B7. See Table 8 for bit assignment of the Buffer functionality.
0 1 0 1	X	X	X	X	X	Output Address/ Buffer	Configuration readback	Readback the connectivity of the Crosspoint cell with the Input location specified in the Address Register and the Output location specified Serial instruction (A0-A6). It also returns the configuration of the Output Buffer addressed in the Serial instruction (A0-A6). The readback data is shifted out of SDO in the following sequence: 1. Crosspoint Connect (1=connected, 0=no connection) 2. Output Enable—B7 (see Table 8) 3. Output Enable—B8 (see Table 8) 4. Reserved (Don't Care) 5. Reserved (Don't Care) 6. State of Broadcast bit 7. State of the RCE bit NOTE: This instruction does not increment the Address Register. This instruction also requires two DR cycles
0 1 1 0	X	X	X	X	X	X	Update the Crosspoint Array	Update the programmed connection from the Loading SRAM to the Active SRAM.
0 1 1 1	X	X	X	X	X	X	Disconnect Input cell	Disconnect the Crosspoint connections from the Input address specified in the Address Register.
1 0 0 0	X	X	X	X	X	Output Address	Disconnect Input and Output	Disconnect the Crosspoint cell at the Input location specified at the Address Register and the Output location specified in the Disconnect instruction (A6-A0). All other connections from the same input address or to the same output address remain the same.

Table 7 Serial Interface Instructions *(Continued)*

I [3:0]	BB	BA	B9	B8	B7	A6-A0	Instruction	Description
1 0 0 1	X	X	X	X	X	Output Address	Connect with ImpliedDisconnect	Connects the Crosspoint cell at the Input location specified on the Address Register and the output location specified in the Connect Serial instruction (A6-A0). All other connections from the same Input address or the same Output address are set to no-connects. NOTE: This instruction increments the Address Register (Input address).
1 0 1 0	X	X	X	X	X	Output Address	Connect—no ImpliedDisconnect	Connects the Crosspoint cell at the Input address specified in the Address Register and the Output address specified in the Connect instruction (A6-A0). All connections to the same output address are set to "no connect" while all other connections from the same input remain the same as before.
1 0 1 1	X	X	X	X	X	Input Address	Set the Address Register	Sets the 7-bit Address Register with the 7-bit address (A6-A0) of the Instruction Register. The 7-bit address of the Address Register becomes the Input port address for Crosspoint Access.
1 1 0 0	X	X	X	X	X	X	Device ID out	Serialize the device ID and revision history out to SDO. ID for the OCX961 is **0x0000D89F**
1 1 0 1	X	X	X	X	X	X	Reset Output Buffer and Crosspoint Array	Resets the Crosspoint Array to no-connects. Sets the Output buffer to Flow-through mode with Output Enabled. The device ID is serialized to SDO.
1 1 1 0	X	X	X	X	X	X	Set RCE Bit	Sets the RCE bit of the Mode Control Register with the Serial instruction bit A0. To turn ON the RCE bit, encode bit A0 to 1. To turn OFF the RCE bit, encode bit A0 to 0.
1 1 1 1	X	X	X	X	X	X	Bypass	Places device in a mode to pass SDI data to SDO with one clock delay. Used for programming and testing devices through serial connected controls.

Table 8 Programming an Output using the Serial Interface

BA, B9, B8, B7	Signal/Function
B8, B7	**Output Enable:**
0,0	Output enabled (ON) – this is the default state at reset
0,1	Output disabled (OFF)
1,0	Output controlled by OE (active high)
1,1	Output controlled by OE# (active low)

Table 9 Number of Cycles and Configuration Time

Operation	OCX961 Serial Cycles
Reset Sequence (SMS = “11111”)	7
Enable or Disable RapidConfigure	28
Change attributes of ONE Output Port	28
Change attributes of ALL Output Ports	2,240
Reset Controller + Reset ALL Output Ports + Clear ALL SRAM cells	35
Connect or disconnect two Ports	56
Configure Entire Switch Matrix (All Switch Matrix Connections)	181,440
Completely Configure the Device (All Output Ports and All Switch Matrix Connections)	183,680

1.5 ImpliedDisconnect

ImpliedDisconnect is a feature that provides the ability to make fast switch connection changes. When using the normal “Connect” command, all other connection to the specified output are set to “no connect”. However, the specified input remains connected to any other outputs to which it was connected before.

The “Connect with ImpliedDisconnect” commands allow the user to disconnect the specified input from all other outputs as well. This enables the user to make a complete connection change in one RapidConfigure cycle.

1.6 Device Reset Options

The power-on reset, RapidConfigure reset, hardware reset, and Serial reset functions will program the output buffers to flow-through mode (with Global Clock selected), and Output Enabled (ON). The Serial interface can be reset via the SRST# pin or by clocking five consecutive one to the SMS pin. The hardware reset pin can be done accomplished through the HW_RST# pin (active low). RC reset can be accomplished by applying the RC instruction 1101 to the RCI[3:0] pins.

Table 10 Device Reset Options

Programming Interface	Reset Method	Output Ports	Switch Matrix	RCE Mode Control	Serial TAP
Hardware Reset	Power-on Reset	OP	NC	1 (RC Enabled)	TLR[1]
	HW_RST# (low pulse)	OP	NC	1 (RC Enabled)	TLR
Serial Reset	1. Low Pulse on SRST#	Unchanged	Unchanged	Unchanged	TLR
	2. SMS high for 5 TCLK cycles	Unchanged	Unchanged	Unchanged	TLR
	3. Device Reset (instruction 1101)	OP	NC	1 (RC Enabled)	TLR
	4. Reset Crosspoint Array (instruction 0010)	Unchanged	NC	Unchanged	Unchanged
RapidConfigure Reset	1. Device reset (instruction 1101)	OP	NC	1 (RC Enabled)	Unchanged
	2. Reset Crosspoint Array (instruction 0010)	Unchanged	NC	Unchanged	Unchanged

1. TLR = Test Logic Reset state.

2. Pin Description

Table 11 OCX961 Pin Description

Pin Name	# of Pins	Type	Description
INP[47:0]	48	Input	Non-inverting differential input signals
INN[47:0]	48	Input	Inverting differential input signals
OUTP[47:0]	48	Output	Non-inverting differential input signals
OUTN[47:0]	48	Output	Inverting differential input signals
OE#	1	Input	Global Output Enable
HW_RST#	1	Input	Hardware Reset
UPDATE#	1	Input	Global Update
RC Pins			
RCA[6:0]	7	Input	RapidConfigure Address A
RCB[6:0]	7	Input	RapidConfigure Address B
RCO[2:0]	3	Output	RapidConfigure Readback
RCI[3:0]	4	Input	RapidConfigure Instruction Bits
RC_CLK#	1	Input	RapidConfigure Clock
RC_EN#	1	Input	RapidConfigure Cycle Enable
Serial Interface Pins			
SCLK	1	Input	Serial Clock
SMS	1	Input	Serial Mode Select
SDI	1	Input	Serial Data In
SRST#	1	Input	Serial Reset
SDO	1	Output	Serial Data Out
Power and Ground Pins			
V_{DD}.CORE	12	2.5V Power	Core Voltage
V_{DD}.PAD (2)	8	3.3V Power	Differential Output Buffer Voltage
V_{DD}.IN (1, 3)	8	3.3V Power	LVTTL Control pins Voltage and Differential Input Buffer Voltage
V_{SS}	38	Ground	Ground
NC	3	No Connect	No Connect

NOTES:

1. Dedicated differential input buffers can receive both LVPECL and LVDS voltage levels using 3.3V supply.
2. V_{DD}.PAD is 3.3V for LVPECL outputs.
3. The LVTTL control, Serial pins, and differential input ports are 3.3V—they are not 5V tolerant.

3. Differential I/O Standards

The OCX961 support the two most popular differential signaling standards: Low Voltage Positive Emitter Coupled Logic (LVPECL) and Low Voltage Differential Signaling (LVDS).

LVPECL is commonly used in video switching applications or those designs requiring transmission of high-speed clock signals. This is the default I/O supported by the OCX961 device.

LVDS is typically used in communication systems as high speed, low noise point-to-point links. The OCX961 conforms to the ANSI/TIA/EIA-644 standard covering electrical specifications for output drivers and receiver inputs.

3.1 LVPECL

LVPECL is a differential signaling standard that specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage or a board termination voltage is not required.

Transmitting and receiving circuits for LVPECL are shown in Figure 6 with termination resistors integrated on-chip, thus, removing the need for any external resistors. Integrated Output Attenuation resistors produce the required LVPECL output swing while providing a 100 ohm output impedance to minimize return reflections.

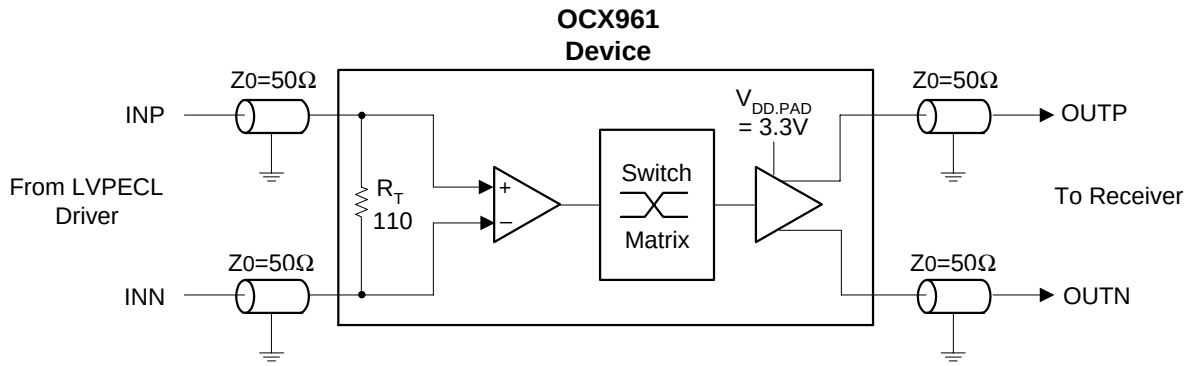


Figure 6 OCX961 Operating in LVPECL Mode

3.2 LVDS

LVDS is a differential signaling standard that requires the use of two pins per input or output. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage or a board termination voltage is not required.

Note – It is possible to operate the OCX961 device withh $V_{DD.}$PAD = 2.5V that will allow the outputs to closely approximate “true LVDS” levels. Refer to the application note “Operating the OCX961 in LVDS Mode” for further details.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 12 Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{DD}.CORE	Supply Voltage (core)	-0.3 to +3.0	V
V_{DD}.IN	Supply Voltage (inputs)	-0.3 to +3.6	V
V_{DD}.PAD	Supply Voltage (differential outputs)	-0.3 to +3.6	V
V_{IN}[2]	Input Voltage	-0.3 to +3.6[3]	V
T_J	Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_{MAX}	Maximum Power Dissipation	6	W
ESD[6]	Electrostatic Discharge	2000	V

4.2 Recommended Operating Conditions

Table 13 Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}.CORE	Supply Voltage (core)	+2.375 to +2.625	V
V_{DD}.PAD[4]	Supply Voltage (differential output buffers)	3.3V ±10%	V
V_{DD}.IN	Supply Voltage (inputs)	+3.0 to +3.6	V
T_A	Operating Temperature: Commercial Operating Temperature: Industrial	0 to +70 -40 to +85	°C

4.3 Pin Capacitance

Table 14 Pin Capacitance[5]

Symbol	Parameter	Max	Units
C_{PIN}	Signal Pin Capacitance	10	pF

1. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. A maximum undershoot of 2V for a maximum duration of 20 ns is acceptable. Overshoot to 3.6V is acceptable.
3. All inputs are 3.3V tolerant with the V_{DD} pin at 2.5V or 3.3V.
4. Note that min and max values for V_{DD} for differential outputs are I/O Standard dependent.
5. Capacitance measured at 25°C. Sample tested only.
6. Measured using Human Body Model.

4.4 DC Electrical Specifications

(T_A = -40°C to 85°C, V_{DD}.IN = 3.3V ±10%, V_{DD}.CORE = 2.5V ±5%)

Table 15 LVTTL DC Electrical Specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High-level Input	Ports are 3.3V tolerant	2.0	3.6	V
V_{IL}	Low-level Input	Ports are 3.3V tolerant	-0.3	0.8	V
V_{OH}	High-level Output	V_{DD}.PAD = Min I_{OH} = -4mA	2.4	V_{DD}.PAD+ 0.3	V
V_{OL}	Low-level Output	V_{DD}.PAD = Min I_{OL} = 8mA		0.4	V
IL_{IH}, IL_{IL} (1)	Input Pin Leakage Current	V_{DD}.IN= Max 0.0 < In < $V_{DD.PAD}$		+5 -50	µA
IL_{OZ}	Tristate Leakage Output OFF State	V_{DD}.PAD = Max 0.0 < In < $V_{DD.PAD}$		+5 -5	µA
Power					
P_{DDQ} (2)	Quiescent Power	All V_{DD} = Max		0.5	W

Table 16 LVPECL DC Electrical Specifications

Symbol	DC Parameters	Min	Max	Units
V_{IN_DIFF}	Input Differential Voltage	±100		mV
V_{IN_COM}	Input Common Mode Voltage	0.25	2.25	V
V_{OUT_DIFF}	Output Differential Voltage	±650	±900	mV
V_{OUT_COM}	Output Common Mode Voltage	$\frac{V_{DD}.PAD}{2}$	$\frac{V_{DD}.PAD}{2}$	V

1. All LVTTL input pins have pull-up resistors.
2. See section 5 for dynamic power consumption calculation.
3. Maximum capacitive load is 12 pF.

The V_{OH} levels are 200mV below standard single-ended LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The above table summarizes the DC output specifications of LVPECL.

4.5 LVPECL AC Electrical Specifications

(V_{DD}.IN = 3.3V ±10%, V_{DD}.CORE = 2.5V ±5%, , V_{DD}.PAD = 3.3V ±10%)

Table 17 LVPECL AC Electrical Specifications

Symbol	Parameter	0°C to 70°C		-40°C to +85°C		Units
		Min	Max	Min	Max	
R_{DATA}	NRZ Data Rate (1)		1.6		1.6	Gb/s
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay, Fanout = 1		3.0		3.5	ns
t_{W+}	Input Flow-through Positive Pulse Width	0.6		0.6		ns
t_{W-}	Input Flow-through Negative Pulse Width	0.6		0.6		ns
t_{DCD+}, t_{DCD-}	Duty Cycle Distortion		0.12		0.12	ns
t_{JITTER}	Output Jitter	TBD	TBD	TBD	TBD	ps
t_{SK}	Skew between Output Ports (1)		0.2		0.25	ns
t_{PHZ_OT}, t_{PLZ_OT}	Output Enable to Valid Data		5		5	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to High Z State		5		5	ns
t_{RC}	RapidConfigure Clock Period	12		12		ns
t_{W+_RC} t_{W-_RC}	RapidConfigure Clock Pulse Width	5		5		ns
t_{S_RC}	RapidConfigure Address Setup to RC_CLK#	3		4		ns
t_{H_RC}	RapidConfigure Address and Enable Hold Time to RC_CLK#	3		4		ns
t_{P_UD}	Update of Crosspoint to Data Out		10		10	ns
f_{SI}	Serial Clock Frequency (SCLK)		20		20	MHz
t_{W_SI}	Serial Clock Pulse Width (SCLK) @ 20MHz cycle	20	30	20	30	ns
t_{S_SI}	Serial Setup Time	4		4		ns
t_{H_SI}	Serial Hold Time	0		0		ns
t_{P_SI}	Serial Clock to Output Data Valid (SDO)		20		20	ns

NOTES:

1. These parameters are guaranteed but not tested in production.

4.6 Timing Diagrams

Note – For the purpose of clarity, the timing diagrams within this data sheet are conceptual representations only and do not show actual circuit implementation.

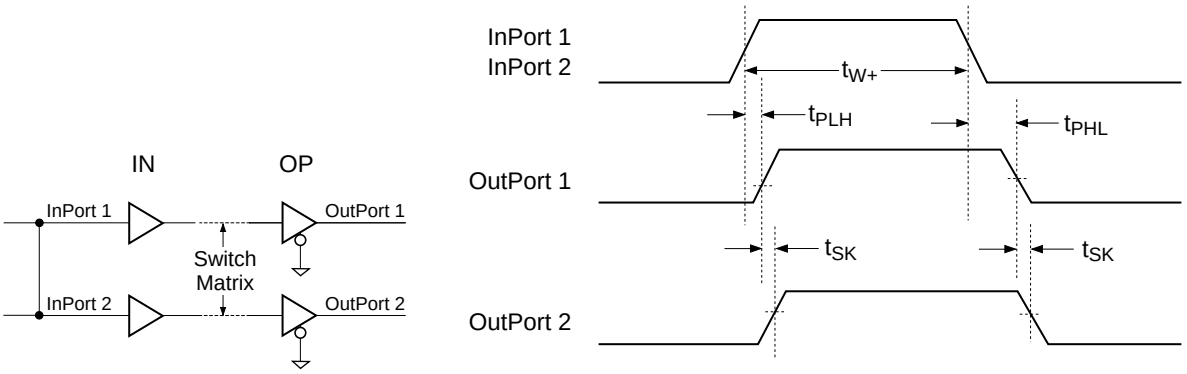


Figure 7 Flow-Through Mode Timing

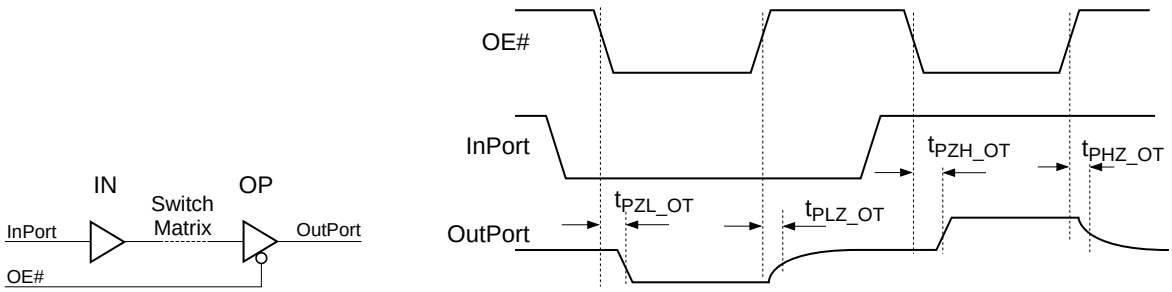


Figure 8 Output Enable Timing

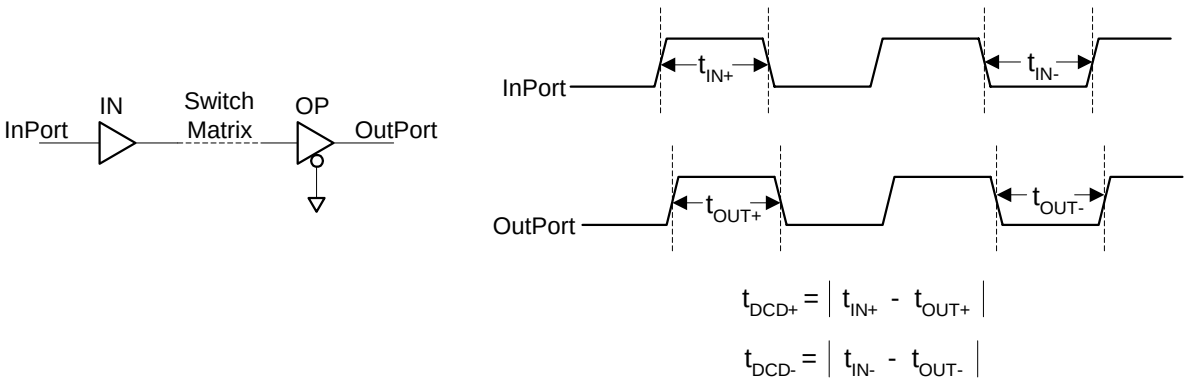


Figure 9 Duty Cycle Distortion

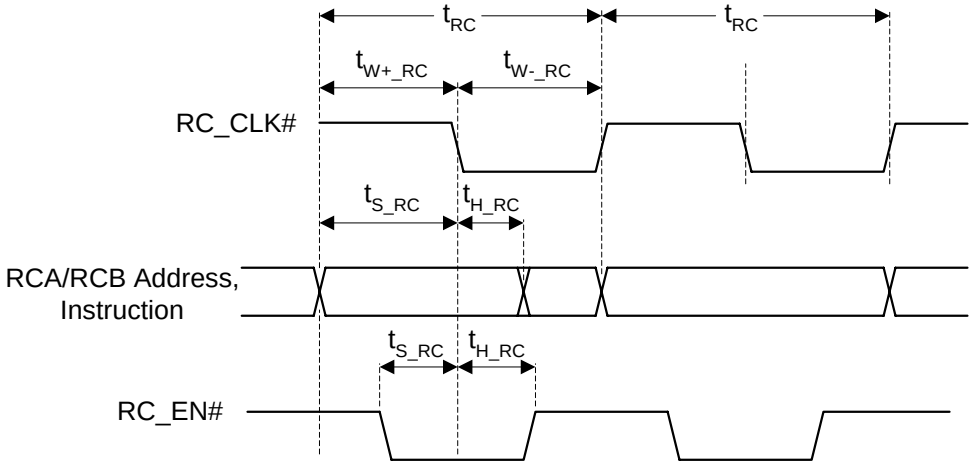


Figure 10 RapidConfigure Write Cycle

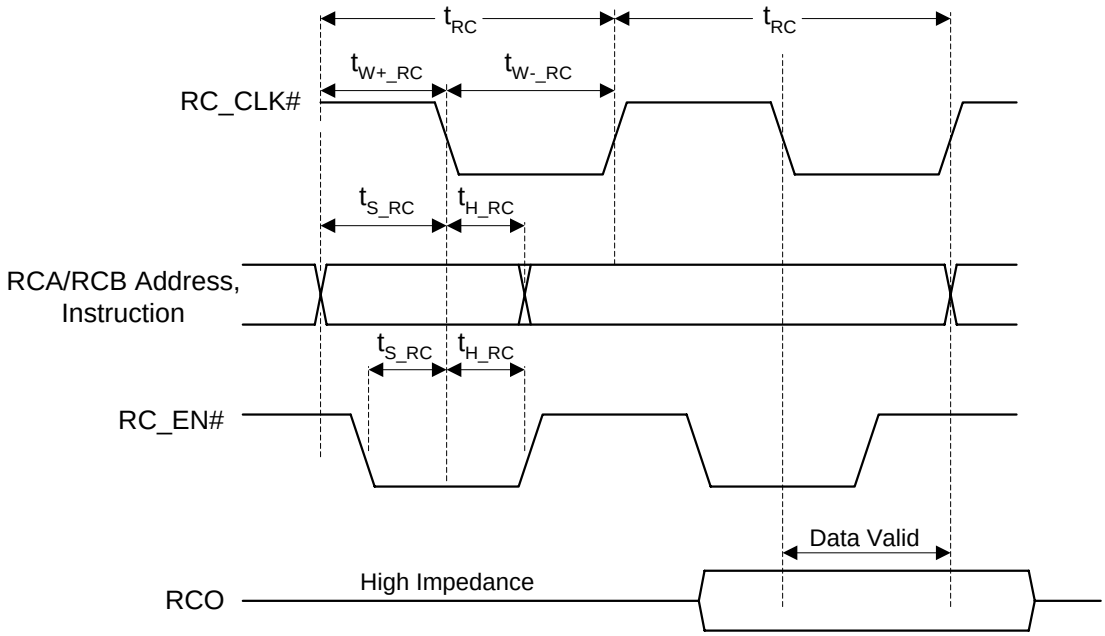


Figure 11 RapidConfigure Read Cycle

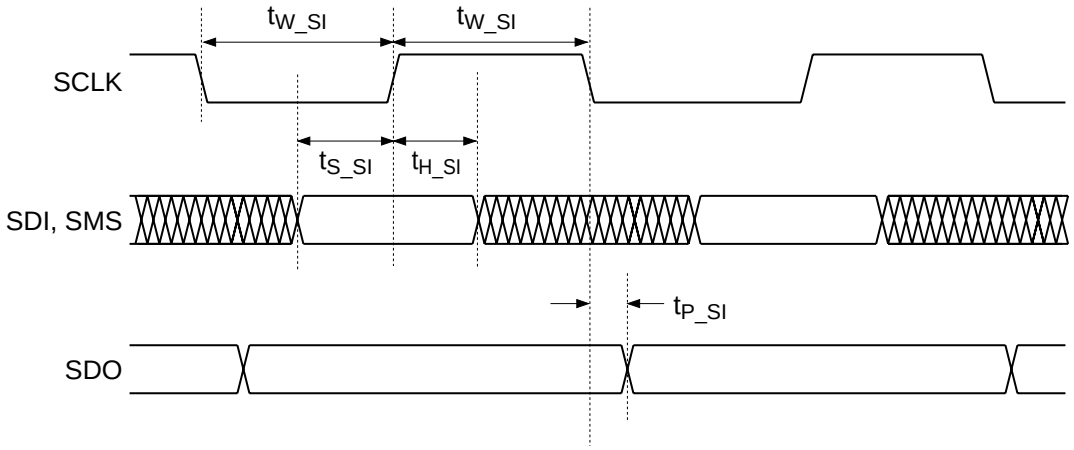


Figure 12 Serial Timing

Typical Performance at 1.6 Gb/s with PRBS Data

(Currently not available for this document)

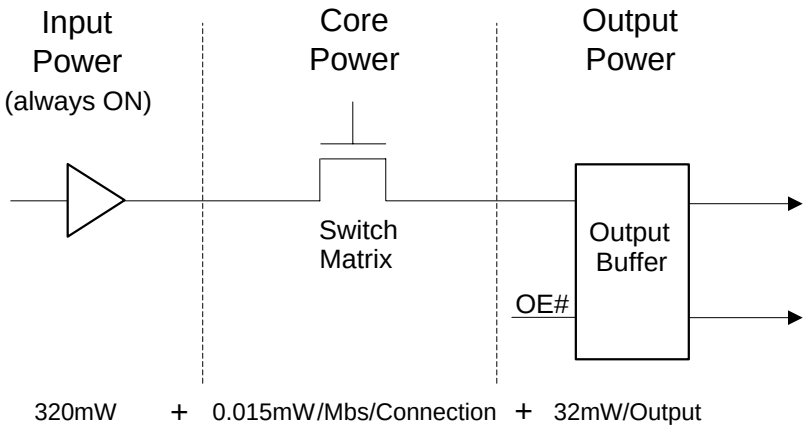
Figure 13 Typical Performance

5. Power Consumption

Chip power, consists of three integral elements (refer to Figure 14):

1. **Input Power**—This element is fixed (always ON) due to the DC current for differential outputs.
2. **Core Power**—This element is the same for LVPECL or LVDS outputs. Core power is a function of data rate (Mb/s) and the number of connection paths through the switch matrix.
3. **Output Power**—This element is a fixed amount for each differential output. The value is zero if the Output Enable (OE#) is disabled or set to OFF.

5.1 Power for LVPECL I/O



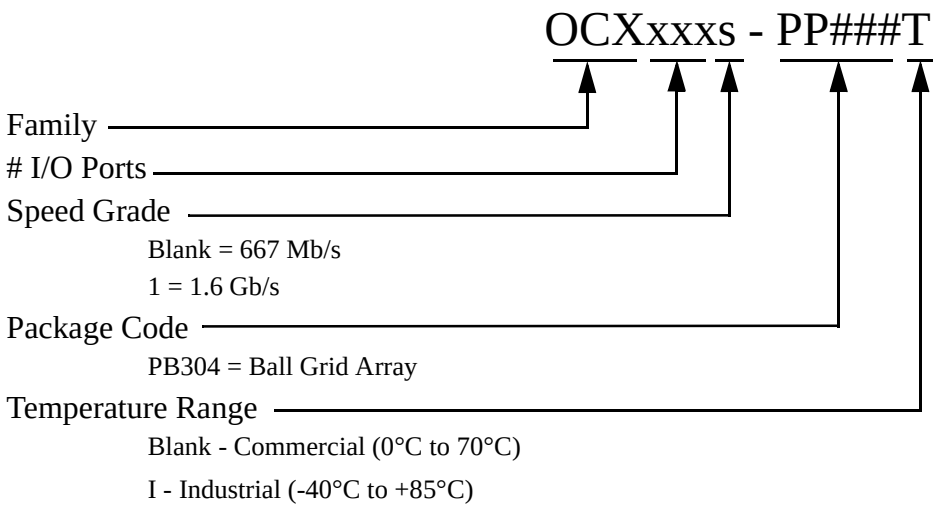
Example: Worst Case = (320mW) + (0.015 mW x 667 x 48) + (32mW x 48)

320mW + 480mW + 1536mW

= 2.34 watts

Figure 14 Power Consumption Diagram for the OCX961 using LVPECL

6. Component Availability and Ordering Information



7. Glossary

CROSSPOINT: A single cell controlled by two RAM bits. The RAM bits are connected in a master-slave configuration to provide an update for programming and changing program information all at once.

CROSSPOINT ARRAY: An array of Crosspoint cells used to connect any input port to any output port.

INPUT OR OUTPUT PATH: The signal flow from pin to array and array to pin. Each path has a register with selectable clocks, drivers for the loaded outputs with selectable enables, and sense circuits to detect changes on either side of the IO Buffer.

PORT: A name followed by a number to identify a pin on the device.

RAPIDCONFIGURE: A parallel programming method for the OCX devices. The RC mode uses 23 dedicated pins to program the Crosspoint Array and the IO Buffers. The 23 pins consist of an enable, a clock, four instruction bits, two seven-bit address fields, and a three-bit data field.

Revision History

Date/	Version No.	Description
4/25/2001	Revision 1.0	Preliminary release of “Advanced” mini data sheet.

8. Product Status Definition

Data Sheet Identification	Product Status	Definition
Advanced	Formative or In Design	This data sheet contains the design specifications for product development. Specification may change in any manner without notice.
Preliminary	Preproduction Product	This data sheet contains the preliminary data, and supplementary data will be published at a later date. I-Cube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Full Production	This data sheet contains final specifications. I-Cube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	No longer in Production	This data sheet contains specifications for a product that has been discontinued by I-Cube. The data sheet is provided for reference information only.

OCX961 Crosspoint Switch Advanced Mini Data Sheet— Rev 1.0, April 2001

I-Cube®, Inc.

2605 S. Winchester Blvd.
Campbell, CA 95008 USA

Phone: +(408) 341-1888
Fax: +(408) 341-1899
Email: marketing@icube.com
Internet: http://www.icube.com

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