TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

262,144-WORD × 2-BANK × 32-BIT SYNCHRONOUS GRAPHICS RAM

DESCRIPTION

The TC59G1632AFB is a CMOS synchronous graphics random access memory organized as 262,144 words × 2 banks × 32 bits. Fully synchronous operations are referenced to the leading edge of the clock input and can transfer data at up to 125M words per second. These devices are controlled by command settings. Each bank is kept active so that the DRAM core sense amplifiers can be used as a cache. The refresh functions, Auto Refresh and Self-Refresh, are easy to use. Using the programmable Mode register and Special Mode register, the system can choose the mode which will maximize its performance. This device is ideal for graphic frame buffer memory in applications such as workstations and personal computers.

FEATURES

ITEM		TC59G1632AFB		
		-80	-10	-12
t_{CK}	Clock Cycle Time (min)	8 ns	10 ns	12 ns
t_{RAS}	Active to Precharge Command Period (min)	48 ns	60 ns	72 ns
t_{CAC}	Access Time from Read Command (max)	21 ns	24 ns	27.5 ns
t_{AC}	Access Time from CLK (max)	7.5 ns	8 ns	9 ns
t_{RC}	Ref/Active to Ref/Active Command Period (min)	80 ns	100 ns	120 ns
I_{CC1}	Operation Current (max) (Single Bank)	175 mA	145 mA	125 mA
I_{CC6}	Self-Refresh Current (max)	2 mA	2 mA	2 mA

- Single power supply of 3.3 V ± 0.3 V
- Up to 125 MHz clock frequency
- Synchronous operations: All signals referenced to the positive edges of the clock.
- Architecture: Pipeline
- Organization: 262,144 words × 2 banks × 32 bits

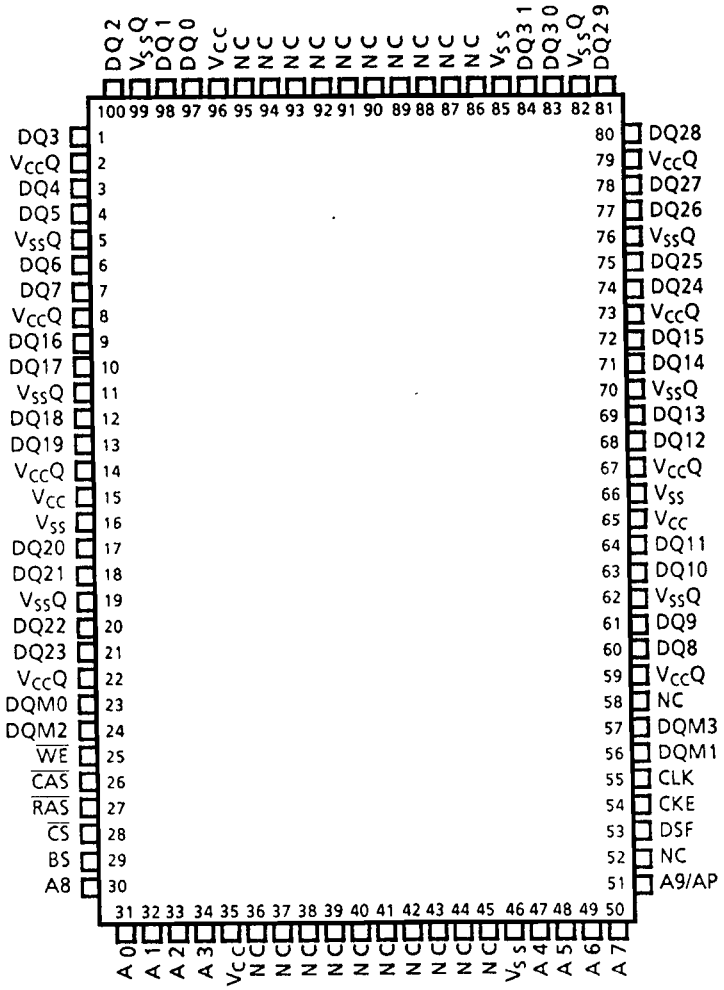
Bank Select: BS
Row Address: A0 to A9
Column Address: A0 to A7

- Programmable Mode register / Special Mode register
- Auto Refresh and Self-Refresh
- Burst Length: 1, 2, 4, 8, Full page
- $\overline{CAS}$ Latency: 1, 2, 3
- Burst Stop Function
- Single Write mode
  Write Per Bit (Old Mask mode)
- Byte data controlled by DQM0 to 3
- 2K Refresh cycles / 32 ms
- Interface: LVTTL
- Package
  TC59G1632AFB: TQFP 100 - P - 1420 - 0.65A

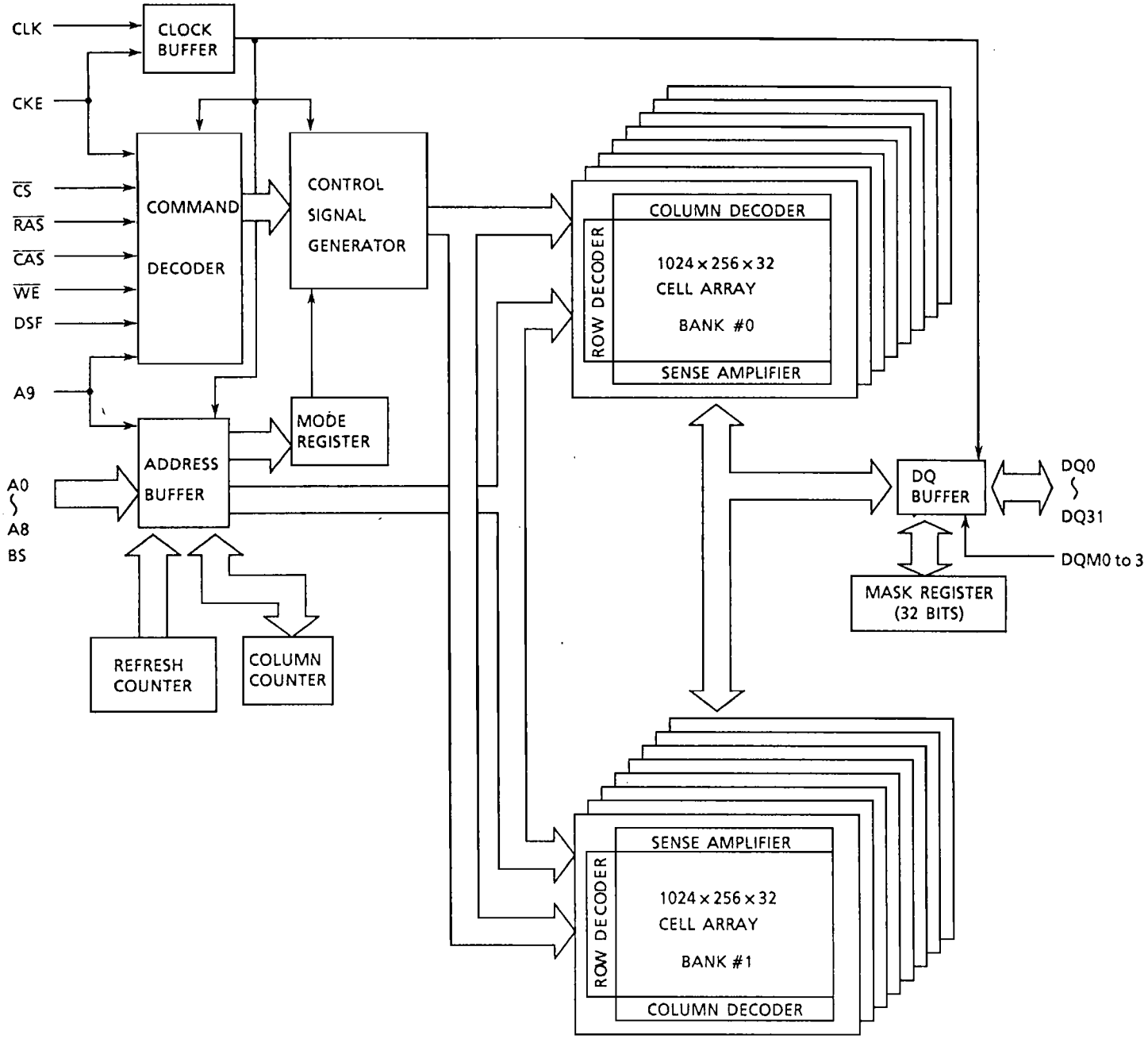
PIN NAMES

A0 to A9	Address
BS	Bank Select
DQ0 to DQ31	Data Input / Output
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
DQM0 to 3	Output Disable / Write Mask
CLK	Clock Inputs
CKE	Clock Enable
V_{CC}	Power (+3.3 V)
V_{SS}	Ground
$V_{CC}Q$	Power (+3.3 V) (for I/O Buffer)
$V_{SS}Q$	Ground (for I/O Buffer)
NC	No Connection
DSF	Special Function Enable

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}, V_{OUT}	Input/Output Voltage	−0.3 to V_{CC} + 0.3	V	1
V_{CC}, $V_{CC}Q$	Power Supply Voltage	−0.3 to 4.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	−55 to 150	°C	1
T_{SOLDER}	Soldering Temperature (10 s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	2
$V_{CC}Q$	Power Supply Voltage (for I/O buffer)	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	−	V_{CC} + 0.3	V	2
V_{IL}	LVTTL Input Low Voltage	−0.3	−	0.8	V	2

Note: V_{IH} (max) = Vcc/VccQ + 1.2 V for pulse width ≦ 5 ns
V_{IL} (min) = Vss/VssQ − 1.2 V for pulse width ≦ 5 ns

CAPACITANCE (V_{CC} = 3.3 V, f = 1 MHZ, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_I	Input Capacitance (A0 to A9, BS, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM0 to 3, CKE)	−	5	pF
	Input Capacitance (CLK)	−	6	pF
C_O	Input/Output Capacitance	−	5	pF

RECOMMENDED DC OPERATING CONDITIONS (V_{CC} = 3.3 V ± 0.3 V, Ta = 0° to 70°C)

ITEM		SYMBOL	MAX			UNIT	NOTES
			-80	-10	-12		
OPERATING CURRENT t_{CK} = min, t_{RC} = min Active Precharge Command Cycling without Burst Operation	1-Bank Operation	I_{CC1}	175	145	125	mA	3
	2-Bank Interleaved Operation	I_{CC1B}	270	225	190		3
STANDBY CURRENT t_{CK} = min, $\overline{CS}$ = V_{IH} $V_{IH/L}$ = $V_{IH\,(min)}$ / $V_{IL\,(max)}$ Bank: Inactive State	CKE = V_{IH}	I_{CC2}	75	65	60		3
	CKE = V_{IL} (Power-down Mode)	I_{CC2P}	2	2	2		3
STANDBY CURRENT CLK = V_{IL}, $\overline{CS}$ = V_{IH} $V_{IH/L}$ = V_{IH} (min) / V_{IL} (max) Bank: Inactive State	CKE = V_{IH}	I_{CC2S}	20	20	20		
	CKE = V_{IL} (Power-down Mode)	I_{CC2PS}	2	2	2		
NO OPERATING CURRENT t_{CK} = min $\overline{CS}$ = V_{IH} (min) Bank: Active State (2 Banks)	CKE = V_{IH}	I_{CC3}	80	70	65		
	CKE = V_{IL} (Power-down Mode)	I_{CC3P}	4	4	4		
BURST OPERATING CURRENT t_{CK} = min I_{OUT} = 0 mA Bank: Active State (2 Banks)	Read Cycle	I_{CC4R}	220	210	200		3, 4
	Write Cycle	I_{CC4W}	200	165	145		3
AUTO REFRESH CURRENT t_{CK} = min Auto Refresh Command Cycling		I_{CC5}	175	145	125		3
SELF-REFRESH CURRENT Self-Refresh Mode CKE = 0.2 V		I_{CC6}	2	2	2		

ITEM	SYMBOL	MIN	MAX	UNIT	NOTES
INPUT LEAKAGE CURRENT (0 V ≦ V_{IN} ≦ V_{CC}, All Other Pins Not under Test = 0 V)	$I_{I(L)}$	−5	5	μA	
OUTPUT LEAKAGE CURRENT (Output disabled, 0 V ≦ V_{OUT} ≦ V_{CCQ})	$I_{O(L)}$	−5	5	μA	
LVTTL OUTPUT H LEVEL VOLTAGE (I_{OUT} = −2 mA)	V_{OH}	2.4	−	V	
LVTTL OUTPUT L LEVEL VOLTAGE (I_{OUT} = 2 mA)	V_{OL}	−	0.4	V	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0° to 70°C) (NOTES: 5, 6, 7)

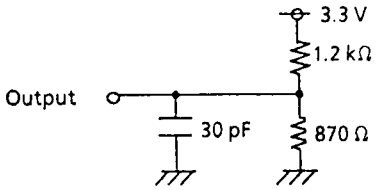
SYMBOL	PARAMETER		-80		-10		-12		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Ref/Active-to- Ref/Active-Command Period		80		100		120		ns	9
t_{RAS}	Active-to-Precharge-Command Period		48	100000	60	100000	72	100000		9
t_{RCD}	Active-to-Read/Write-Command Delay Time		24		30		36			9
t_{CCD}	Read/Write (a)-to-Read/Write (b)-Command Period		8		10		12			9
t_{RP}	Precharge-to-Active-Command Period		24		30		36			9
t_{RRD}	Active (a)-to-Active (b)-Command Period		20		20		24			9
t_{CAC}	Access Time from Read Command			21		24		27.5		9
t_{WR}	Write Recovery Time	CL* = 1	24		30		36			
		CL* = 2	12		15		18			
		CL* = 3	8		10		12			
t_{CK}	CLK Cycle Time	CL* = 1	24	1000	30	1000	36	1000		
		CL* = 2	12	1000	15	1000	18	1000		
		CL* = 3	8	1000	10	1000	12	1000		
t_{CH}	CLK High Level Width		2		3		4			10
t_{CL}	CLK Low Level Width		2		3		4			10
t_{AC}	Access Time from CLK	CL* = 1		21		24		27.5		
		CL* = 2		9		9		9.5		
		CL* = 3		7.5		8		9		
t_{OH}	Output Data Hold Time		2.5		2.5		2.5			
t_{HZ}	Output Data High-Impedance Time		3	8	3	10	3	12		8
t_{LZ}	Output Data Low-Impedance Time		0		0		0			
t_{SB}	Power-down Mode Entry Time		0	8	0	10	0	12		
t_T	Transition Time of CLK (Rise and Fall)		1	10	1	10	1	10		
t_{DS}	Data-in Setup Time		3		3		3			
t_{DH}	Data-in Hold Time		1		1		1.5			
t_{AS}	Address Setup Time		3		3		3			
t_{AH}	Address Hold Time		1		1		1.5			
t_{CKS}	CKE Setup Time		3		3		3			
t_{CKH}	CKE Hold Time		1		1		1.5			
t_{CMS}	Command Setup Time		3		3		3			
t_{CMH}	Command Hold Time		1		1		1.5			
t_{REF}	Refresh Time			32		32		32	ms	
t_{RSC}	Mode Register Set Cycle Time		8		10		12		ns	9
t_{SBW}	Special Mode Register Set Cycle Time		8		10		12			9

* CL is $\overline{CAS}$ Latency.

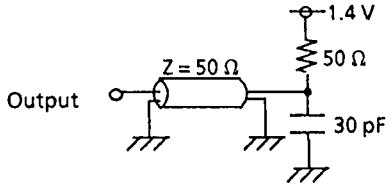
NOTES:

1. Conditions outside the limits listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and are measured at the minimum values of t_{CK} and t_{RC}. Input signals are changed once during t_{CK}.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. The Power-up sequence is described in Note 11.
6. AC TEST CONDITIONS

Output Reference Level	1.4 V / 1.4 V
Output Load	See Diagram (B) Below
Input Signal Levels	2.4 V / 0.4 V
Transition Time (Rise and Fall) of Input Signals	2 ns
Input Reference Level	1.4 V



LVTTL AC TEST LOAD (A)



LVTTL AC TEST LOAD (B)

7. Transition times are measured between V_{IH} and V_{IL}. The transition (rise and fall) of input signals has a fixed slope.
8. t_{HZ} defines the time at which the outputs go open circuit and is not referenced to output voltage levels.

9. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows:

number of clock cycles = specified value of timing / clock period

(count fractions as a whole number)

Relationship between latency and frequency (unit: clock cycles)

-80 Version (Calculation with t_{CK} = 8 ns to 24 ns)

CLK period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}	t_{SBW}
	80 ns	48 ns	24 ns	21 ns	24 ns	8 ns	20 ns	8 ns
≧ 24.0 ns	4	2	1	1	1	1	1	1
≧ 16.0 ns	5	3	2	2	2	1	2	1
≧ 14.0 ns	6	4	2	2	2	1	2	1
≧ 12.0 ns	7	4	2	2	2	1	2	1
≧ 10.0 ns	8	5	3	3	3	1	2	1
≧ 9.0 ns	9	6	3	3	3	1	3	1
≧ 8.0 ns	10	6	3	3	3	1	3	1

-10 Version (Calculation with t_{CK} = 10 ns to 30 ns)

CLK period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}	t_{SBW}
	100 ns	60 ns	30 ns	24 ns	30 ns	10 ns	20 ns	10 ns
≧ 30.0 ns	4	2	1	1	1	1	1	1
≧ 20.0 ns	5	3	2	2	2	1	1	1
≧ 18.0 ns	6	4	2	2	2	1	2	1
≧ 15.0 ns	7	4	2	2	2	1	2	1
≧ 13.4 ns	8	5	3	3	3	1	2	1
≧ 12.5 ns	8	5	3	3	3	1	2	1
≧ 12.0 ns	9	5	3	3	3	1	2	1
≧ 10.0 ns	10	6	3	3	3	1	2	1

-12 Version (Calculation with t_{CK} = 12 ns to 36 ns)

CLK period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}	t_{SBW}
	120 ns	72 ns	36 ns	27.5 ns	36 ns	12 ns	24 ns	12 ns
≧ 36.0 ns	4	2	1	1	1	1	1	1
≧ 24.0 ns	5	3	2	2	2	1	1	1
≧ 20.0 ns	6	4	2	2	2	1	2	1
≧ 18.0 ns	7	4	2	2	2	1	2	1
≧ 16.0 ns	8	5	3	3	3	1	2	1
≧ 15.0 ns	8	5	3	3	3	1	2	1
≧ 14.4 ns	9	5	3	3	3	1	2	1
≧ 13.4 ns	9	6	3	3	3	1	2	1
≧ 12.0 ns	10	6	3	3	3	1	2	1

10. t_{CH} is the pulse width of CLK measured from the leading edge to the falling edge and referenced to V_{IH} (min). t_{CL} is the pulse width of CLK measured from the falling edge to the leading edge and referenced to V_{IL} (max).

11. Power-up Sequence

Power-up must be performed in the following sequence.

1) Power must be applied to V_{CC} and $V_{CC}Q$ (simultaneously) while all input signals are held in the NOP state. The CLK signals must be started at the same time.

2) After power-up a pause of at least 200 μseconds is required. The DQM and CKE signals must then be held High (at the V_{CC} level) to ensure that the DQ output is High-Impedance.

3) Both banks must be precharged.

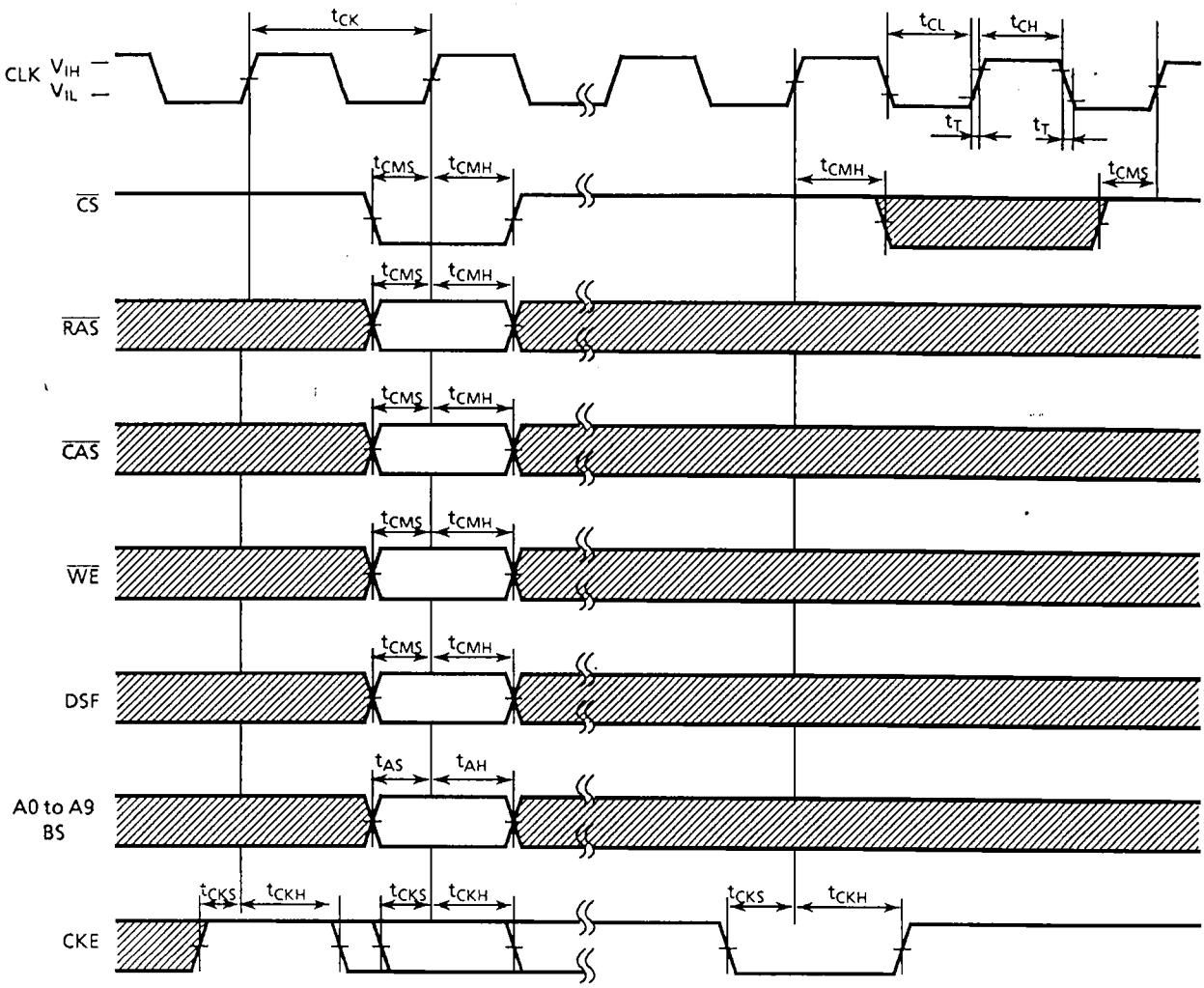
4) The Mode Register Set command must be asserted to initialize the Mode register.

5) A minimum of eight Auto Refresh dummy cycles are required to stabilize the internal circuitry of the device.

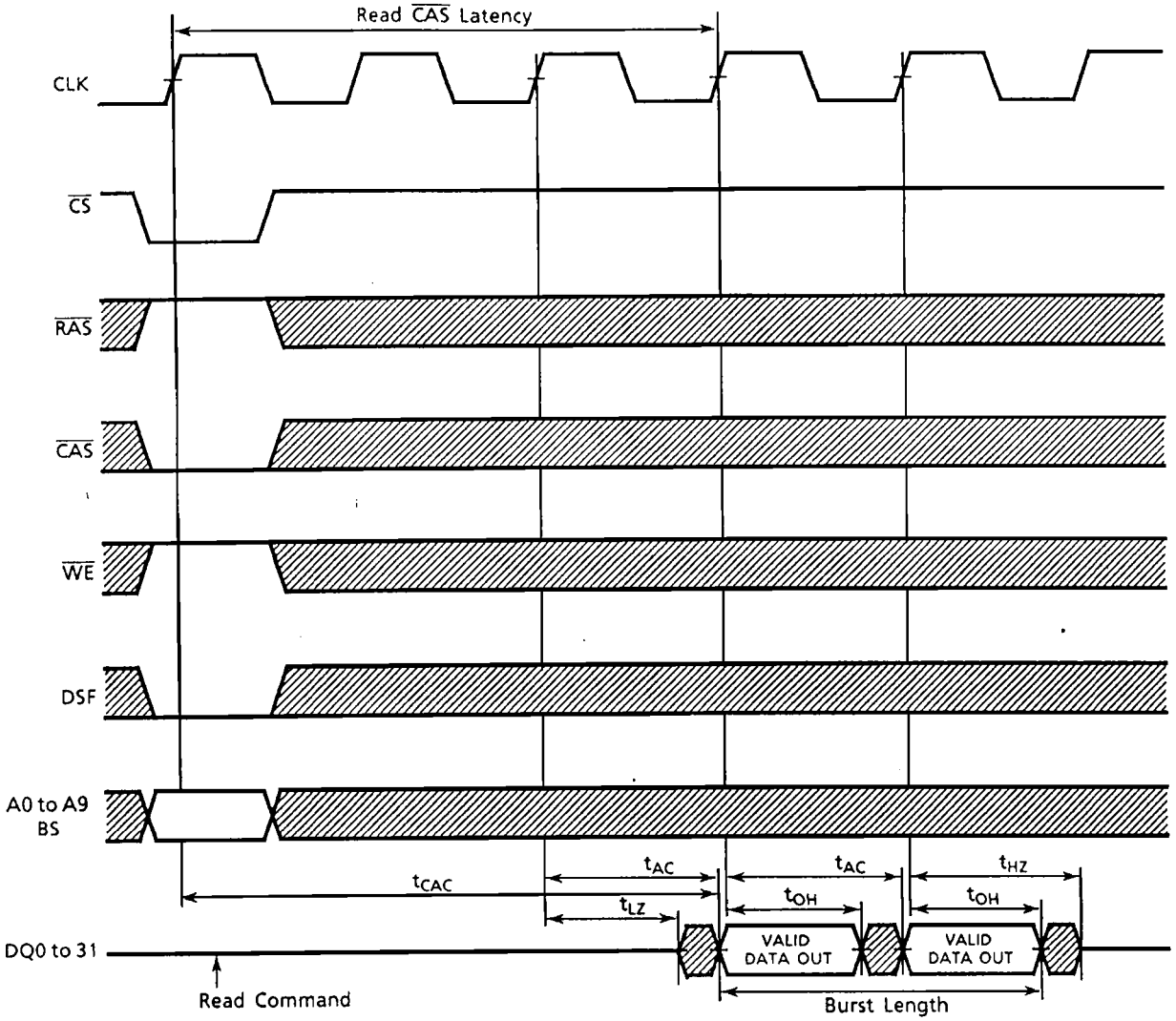
The Mode Register Set command can be invoked either before or after the Auto Refresh dummy cycles.

TIMING DIAGRAMS

Command Input Timing

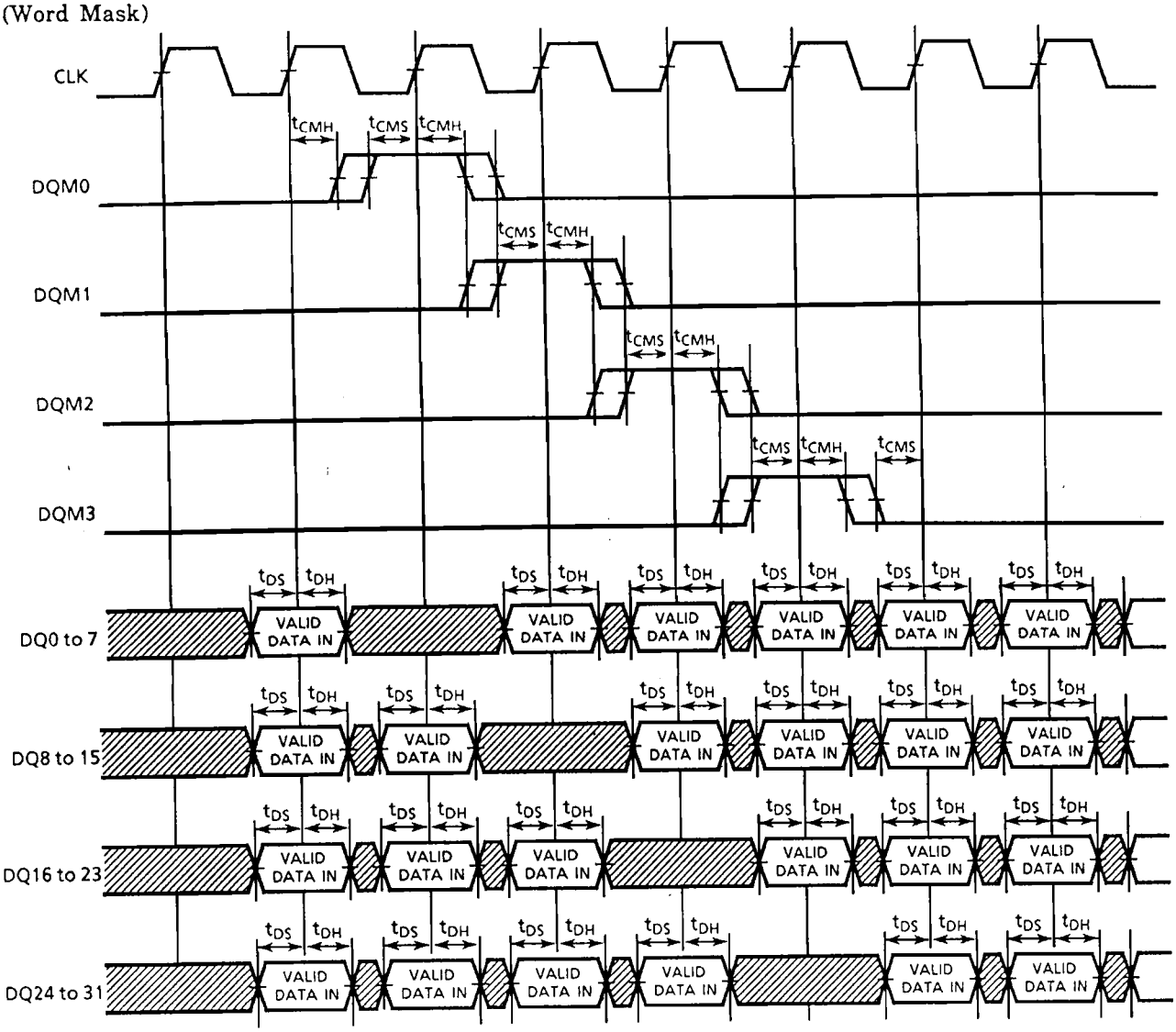


Read Timing

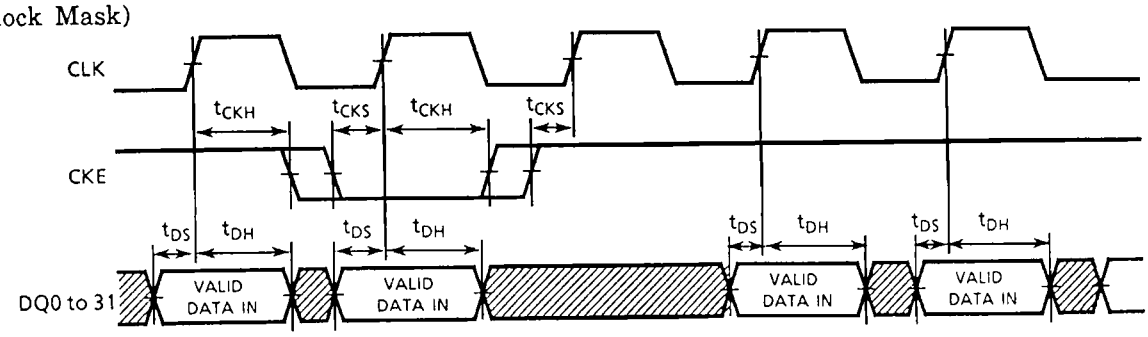

Read $\overline{CAS}$ Latency
CLK
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
DSF
A0 to A9
BS
t_{CAC}
t_{AC}
t_{LZ}
t_{AC}
t_{OH}
t_{HZ}
t_{OH}
DQ0 to 31
VALID DATA OUT
VALID DATA OUT
Read Command
Burst Length

Control Timing for Input Data

(Word Mask)

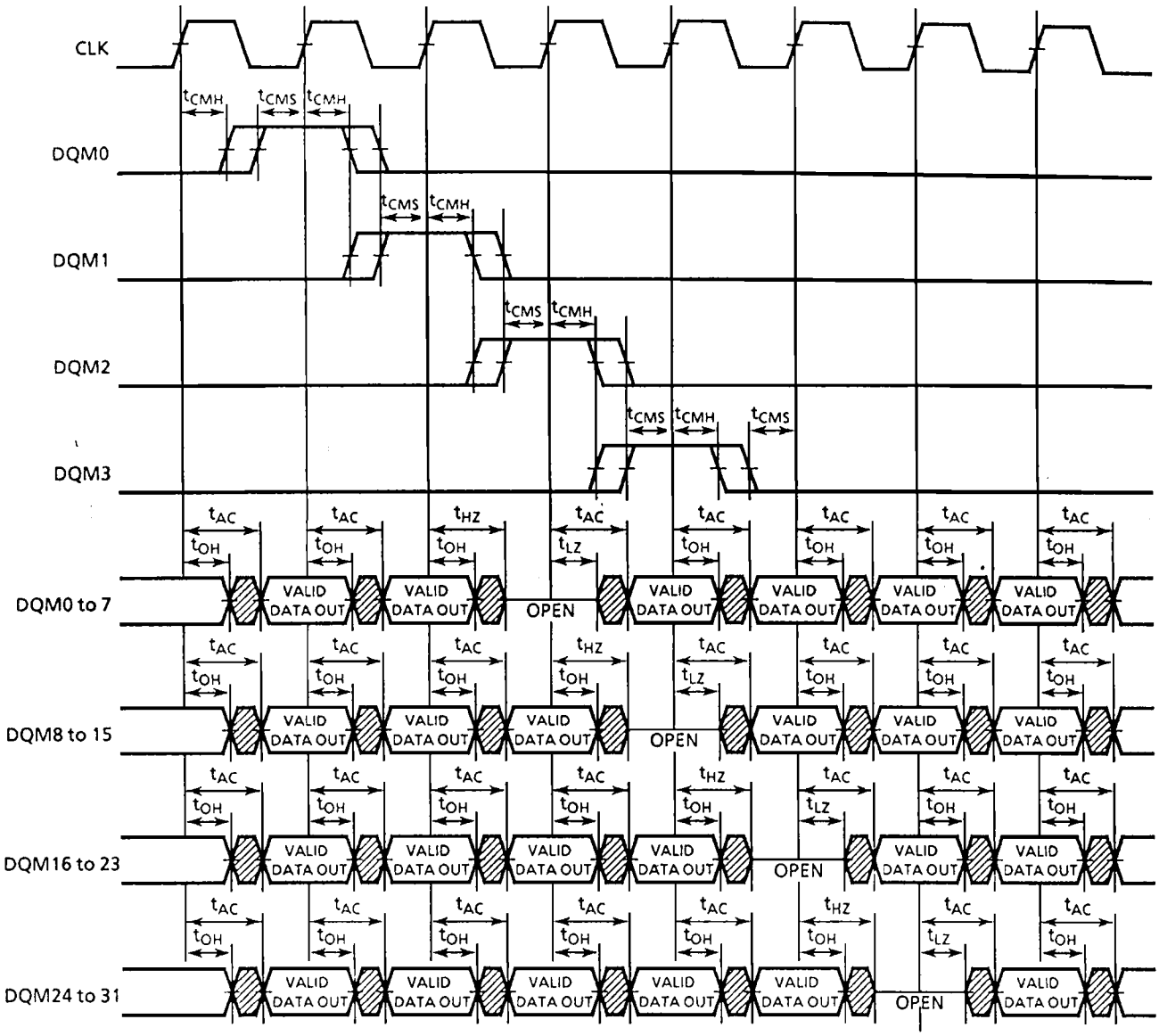


(Clock Mask)

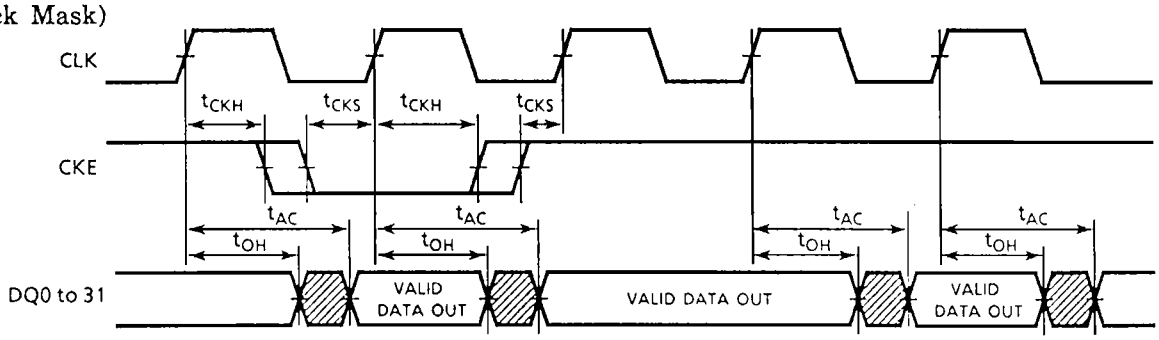


Control Timing for Output Data

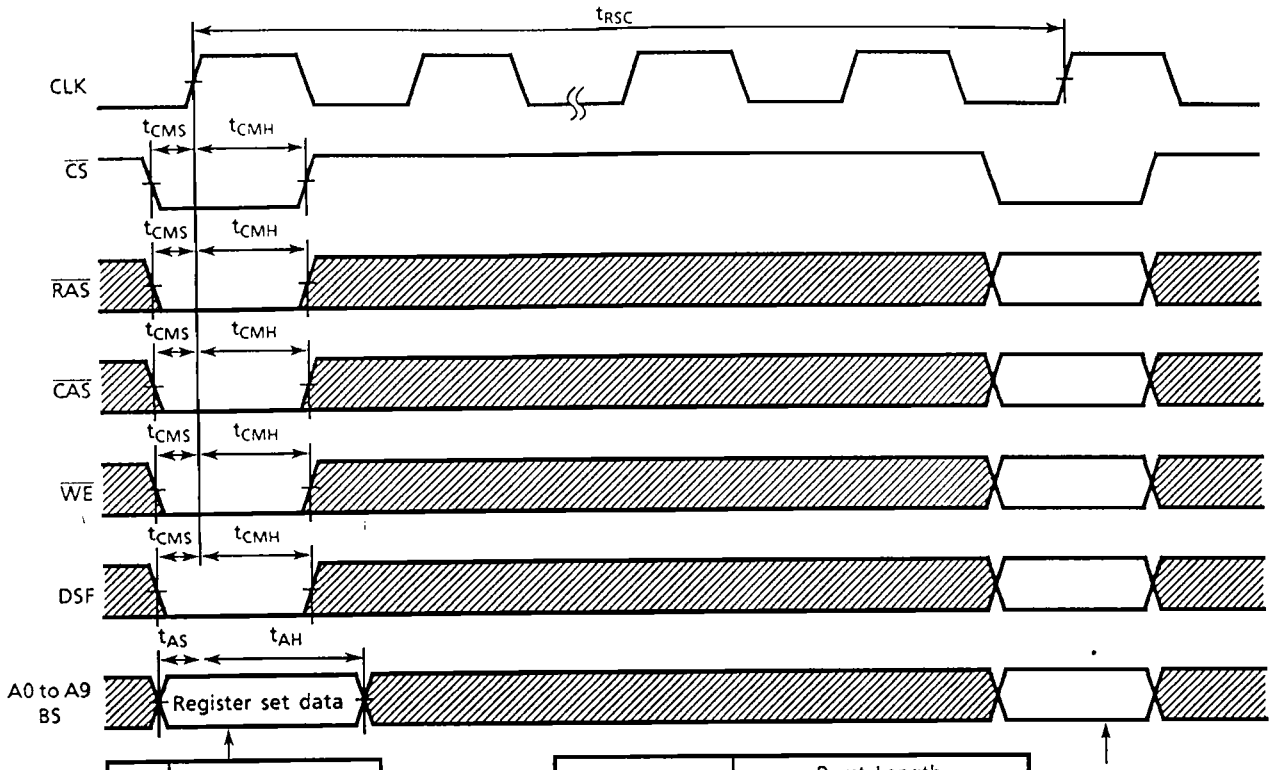
(Output Enable)



(Clock Mask)



Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	0	(Test Mode)
A8	×	Reserved
A9	×	Reserved
BS	Single Write Mode	

NOTE: 0 = Low level
1 = High level
× = Don't care

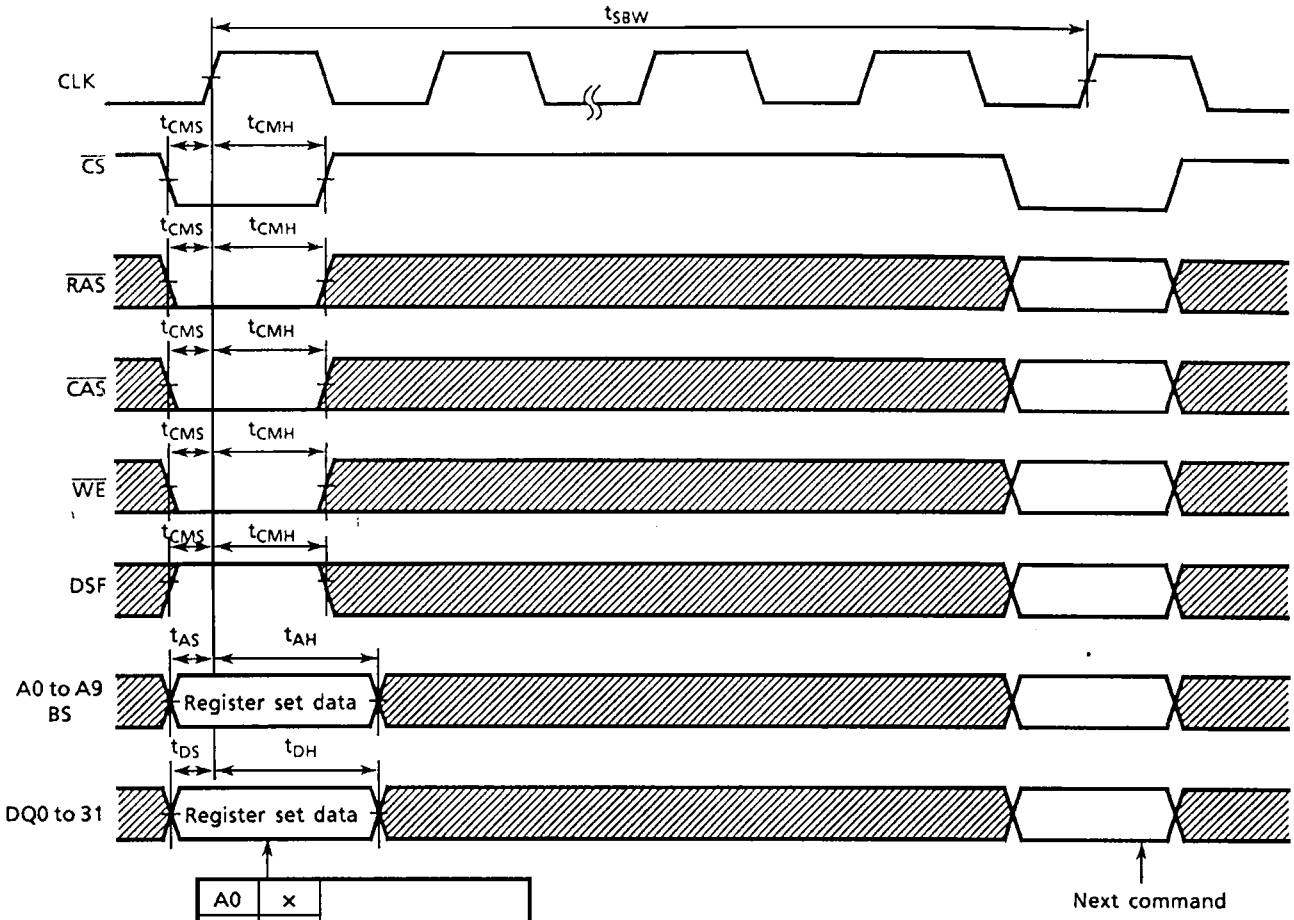
			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	1	Reserved
0	0	1	2	Reserved
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleaved

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	
1	1	1	

BS	Single Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Special Mode Register Set Cycle



A0	×	Reserved
A1	×	
A2	×	
A3	×	
A4	×	
A5	Load Mask (LM)	
A6	0	Unused
A7	×	Reserved
A8	×	
A9	×	
BS	×	

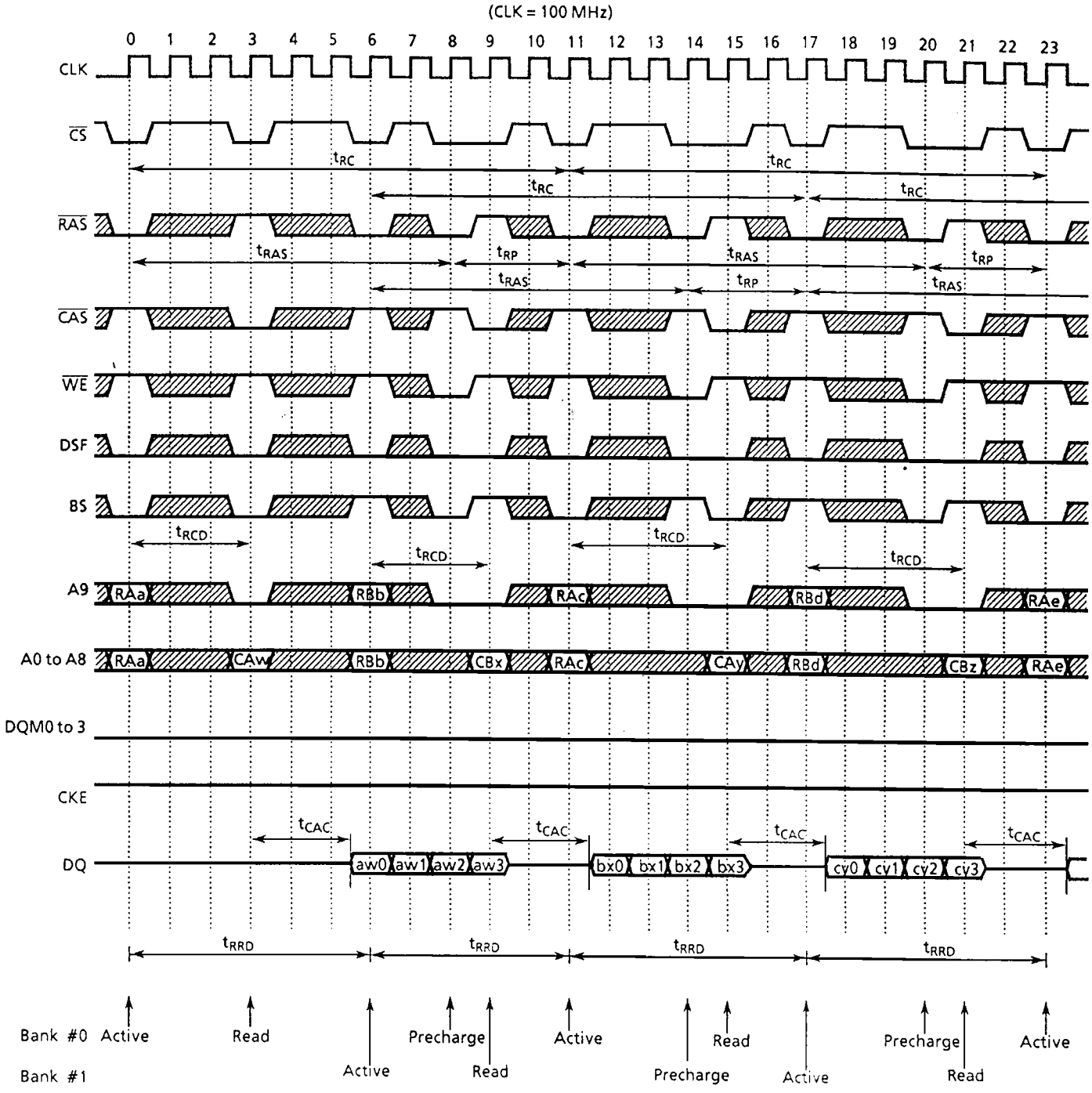
A5	Load Mask Register Set Mode
0	Unchanged
1	Load

DQi	Load Mask
0	Enable
1	Disable

NOTE: A6 must be set to 0.

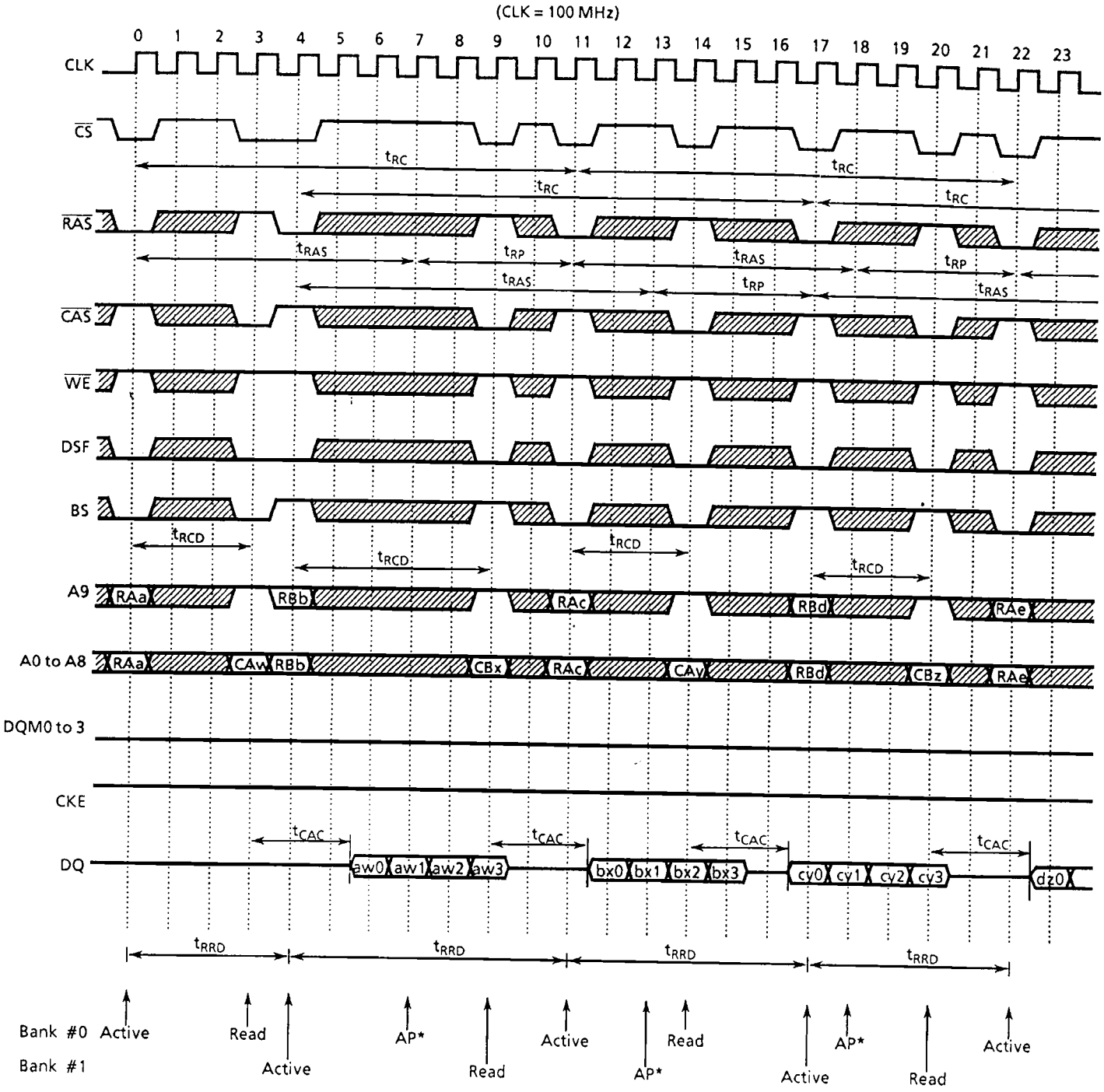
OPERATING TIMING EXAMPLES (-10 Version)

Figure 1. Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



NOTE: See Figure 20.

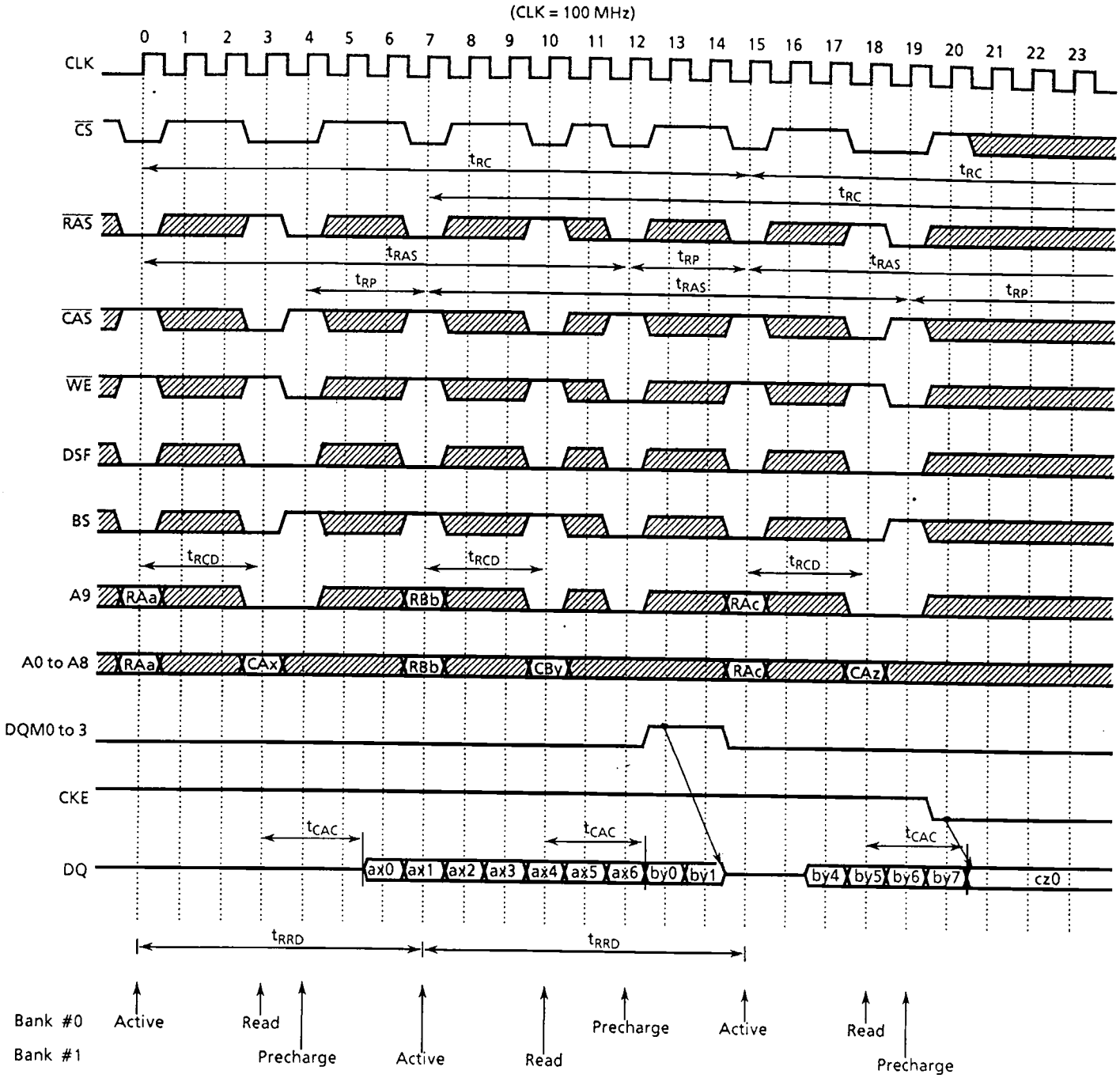
Figure 2. Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3, Auto Precharge)



* AP is the internal precharge start timing.

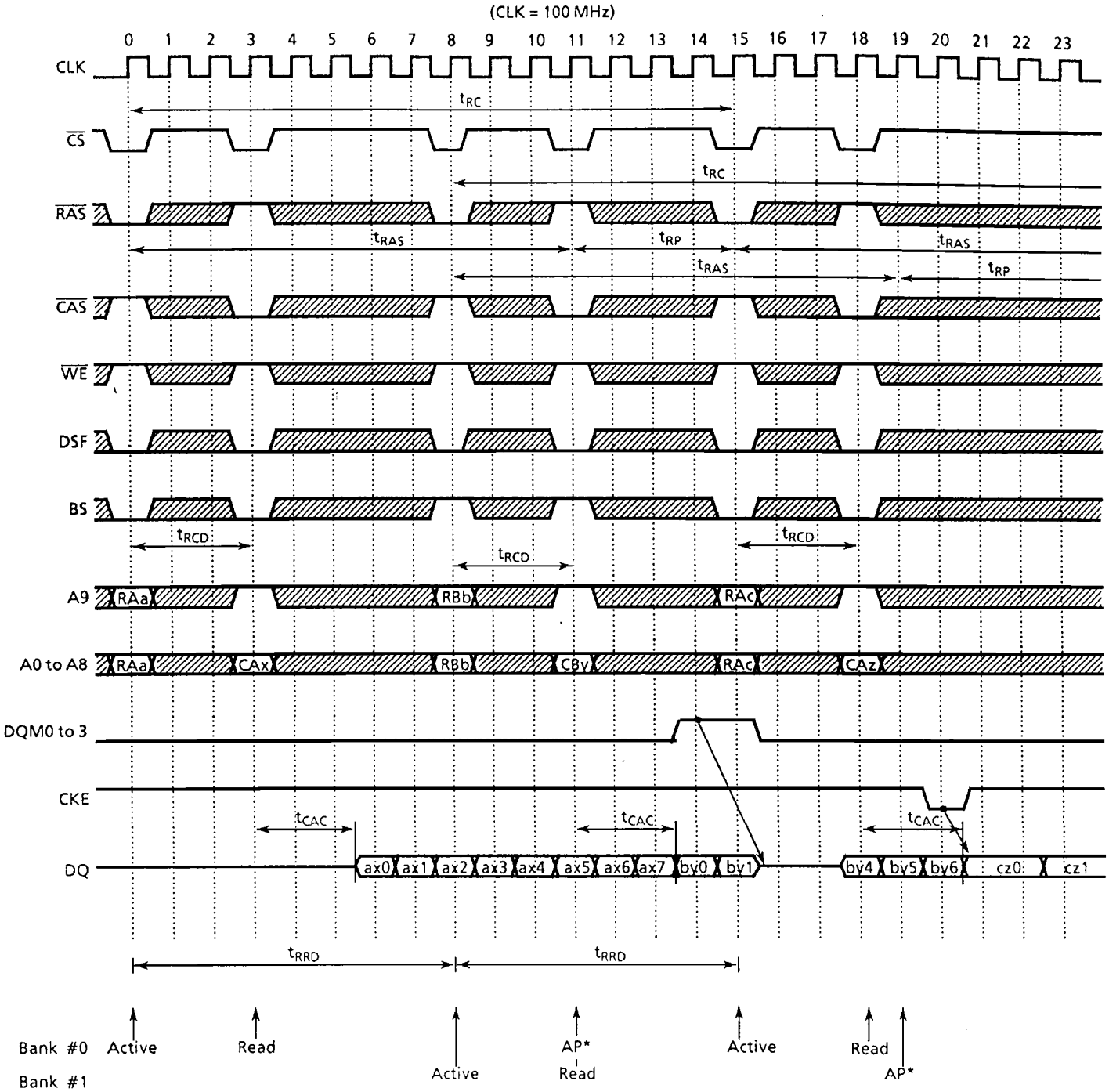
NOTE: See Figure 15.

Figure 3. Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3)



NOTE: See Figure 20.

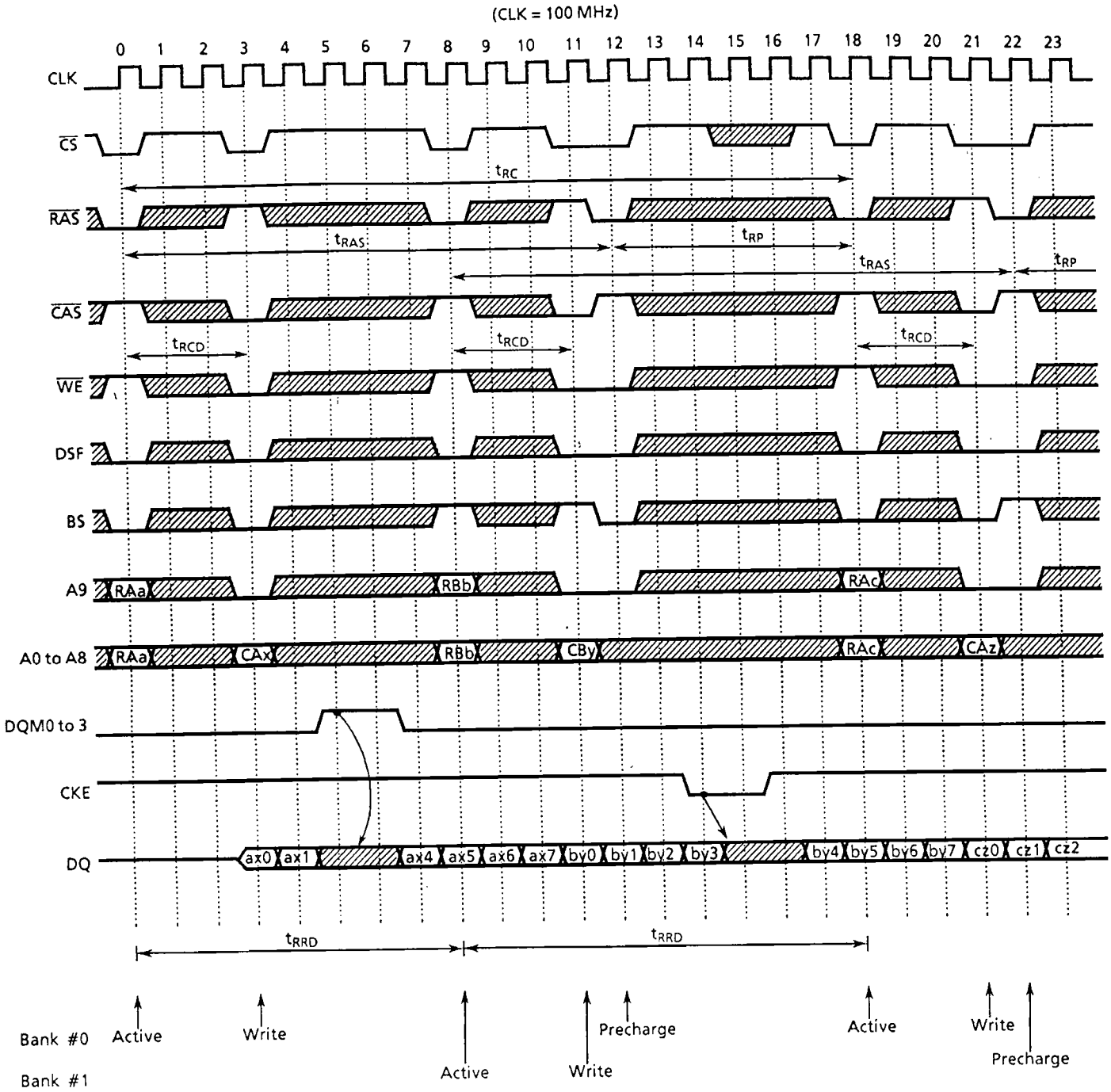
Figure 4. Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3, Auto Precharge)



* AP is the internal precharge start timing.

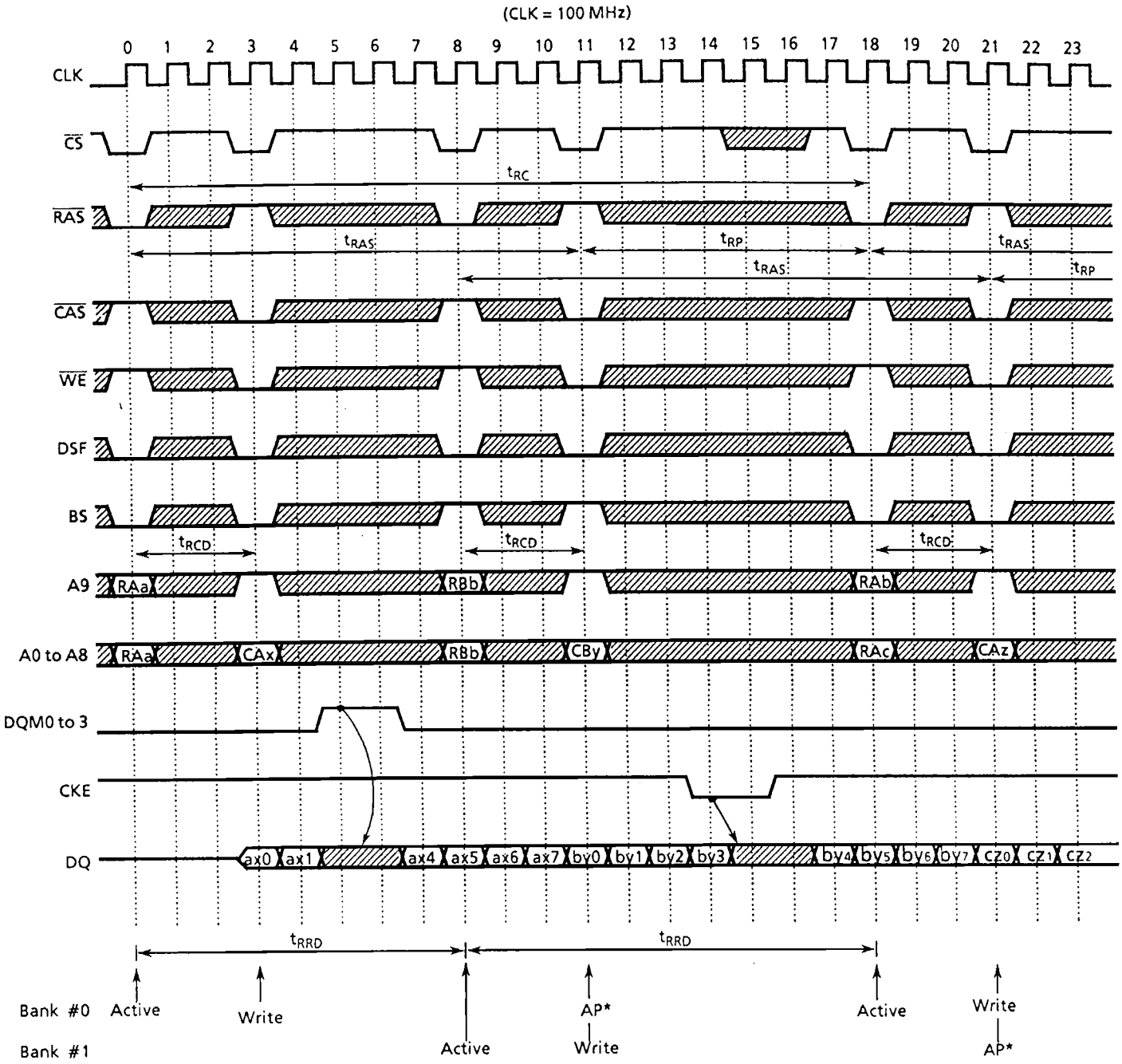
NOTE: See Figure 15.

Figure 5. Interleaved Bank Write (Burst Length = 8)



NOTE: See Figure 20.

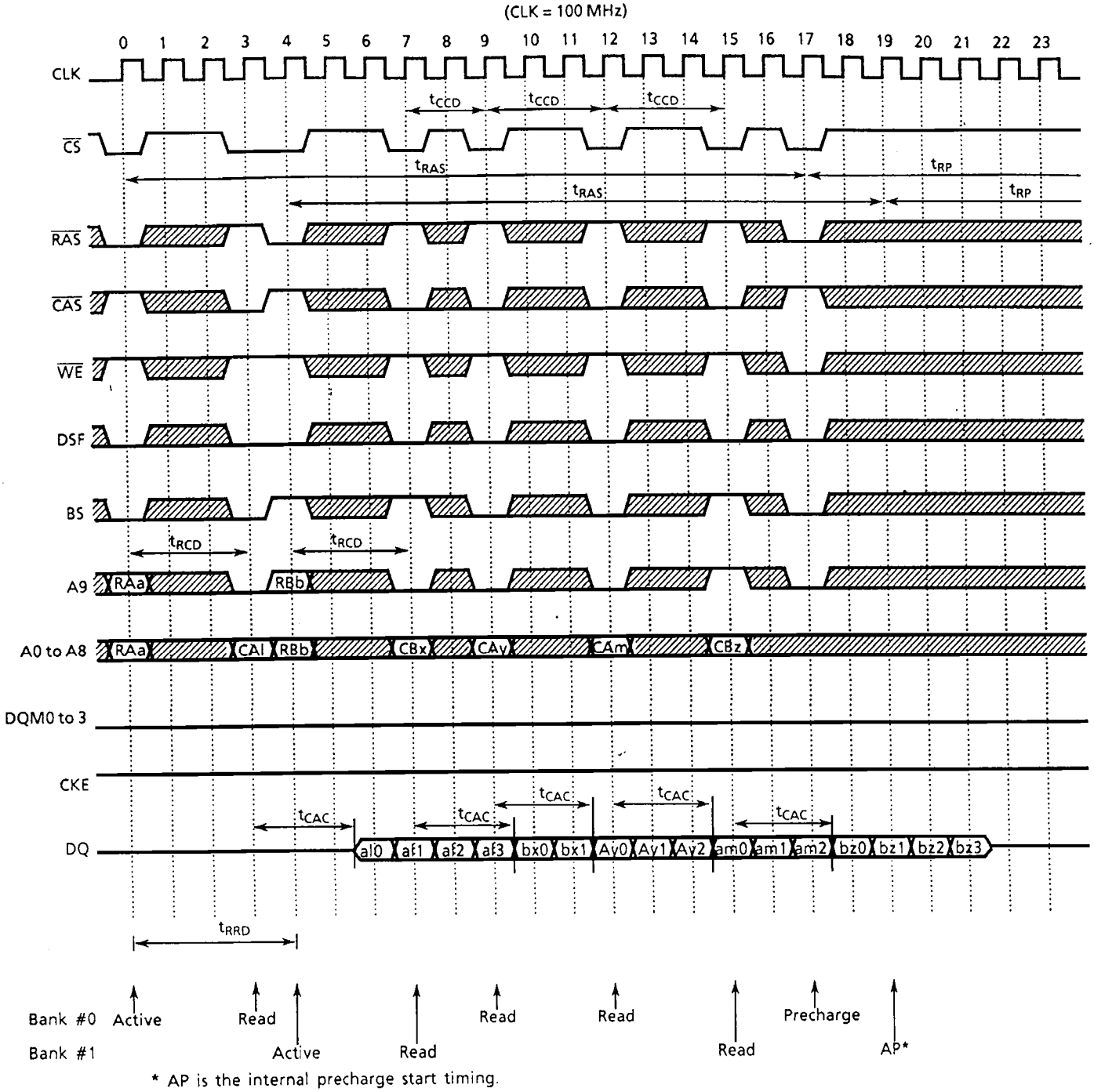
Figure 6. Interleaved Bank Write (Burst Length = 8, Auto Precharge)



* AP is the internal precharge start timing.

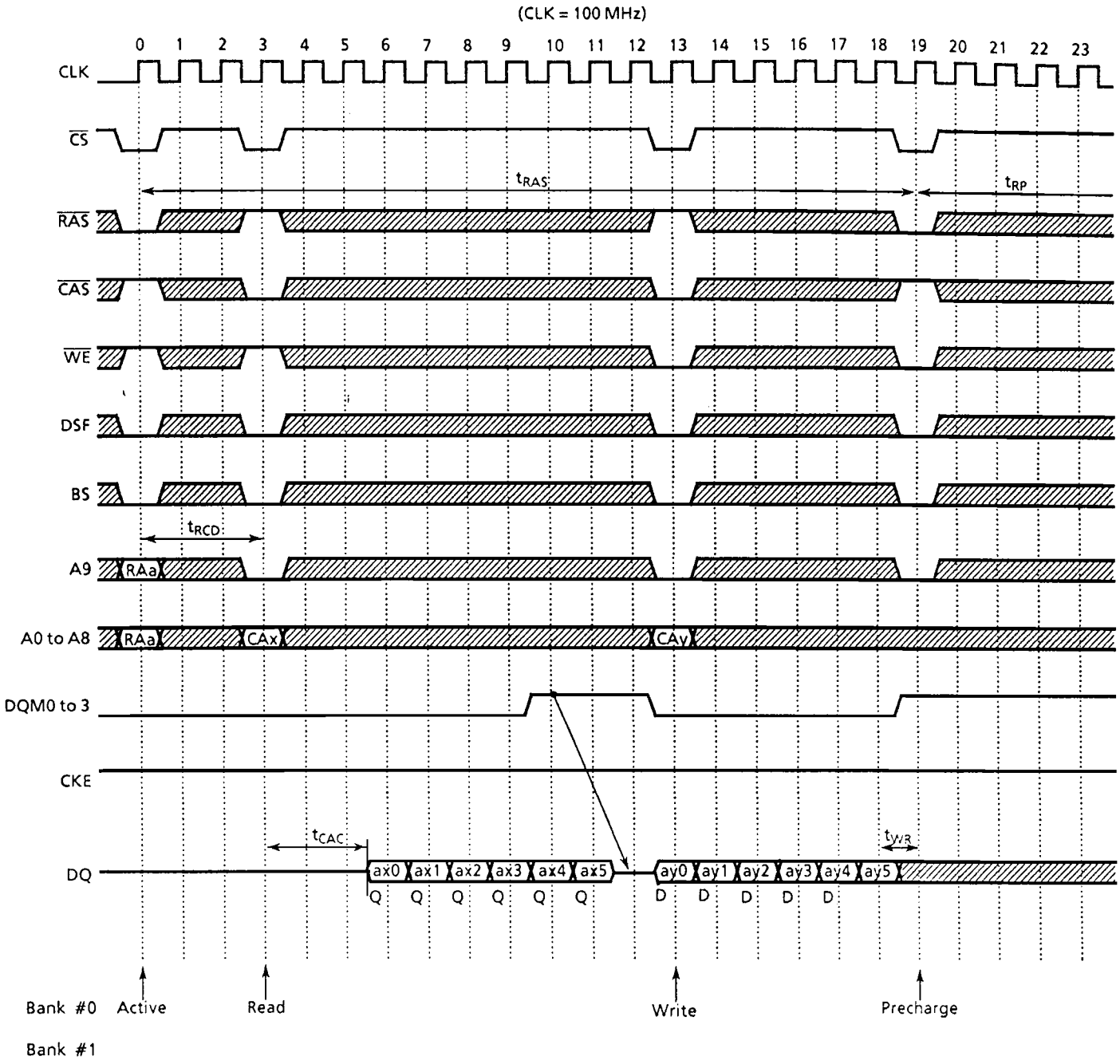
NOTE: See Figure 16.

Figure 7. Page Mode Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



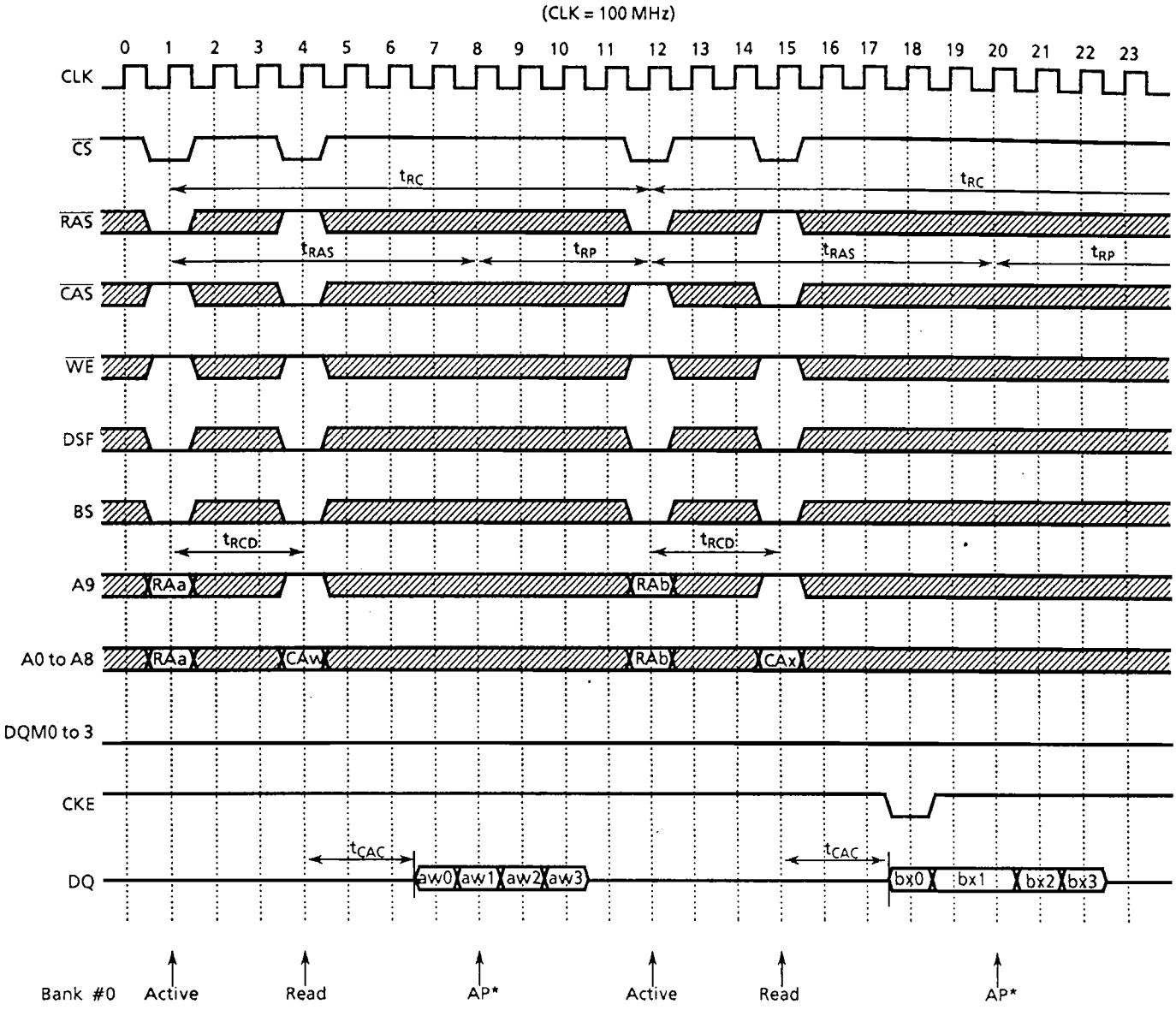
* AP is the internal precharge start timing.

Figure 8. Page Mode Read / Write (Burst Length = 8, $\overline{CAS}$ Latency = 3)



NOTE: See Figures 17 and 20.

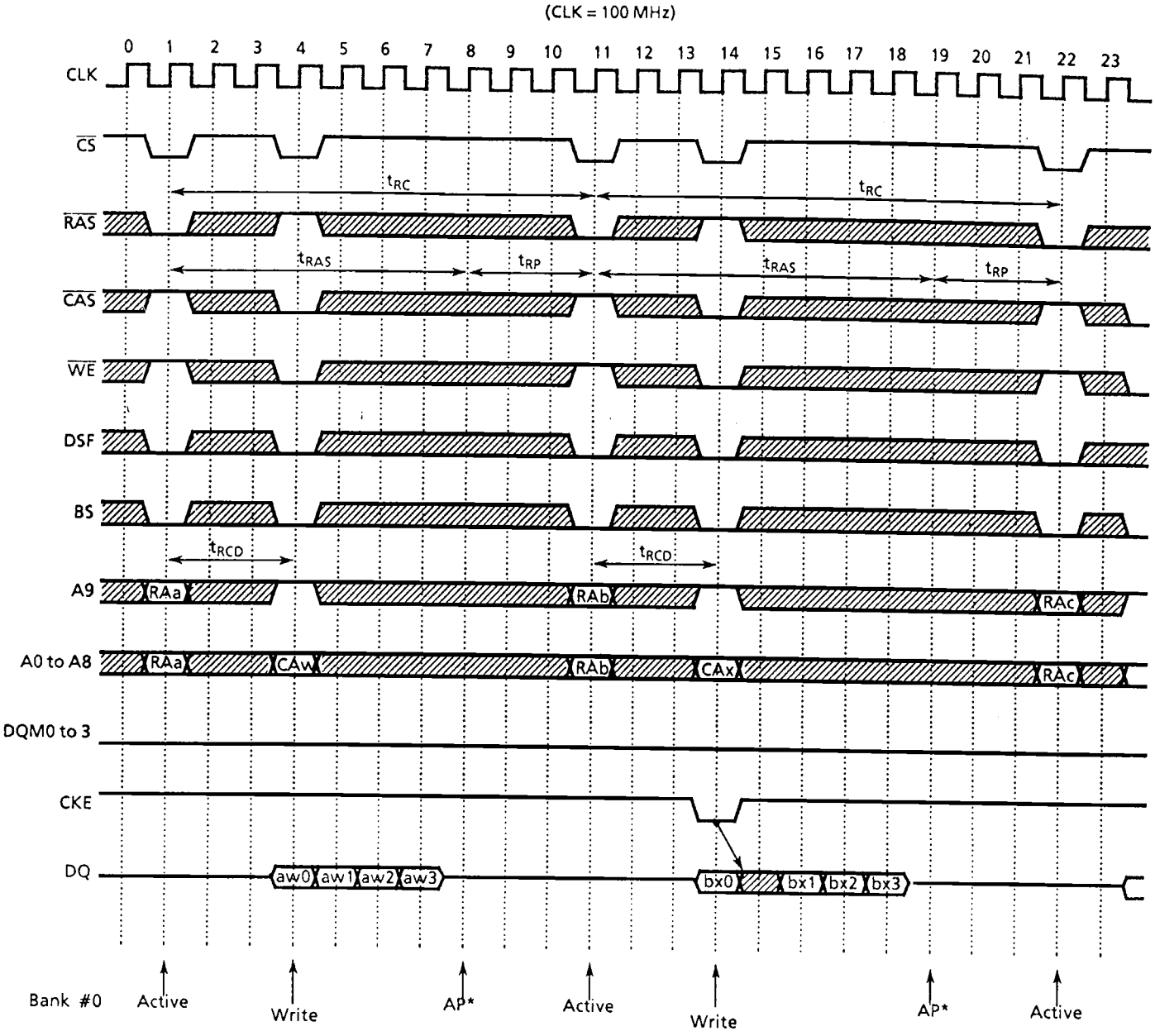
Figure 9. Auto Precharge Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



*AP is the internal precharge start timing.

NOTE: See Figure 15.

Figure 10. Auto Precharge Write (Burst Length = 4)



* AP is the internal precharge start timing.

NOTE : See Figure 16.

Figure 11. Auto Refresh Cycle

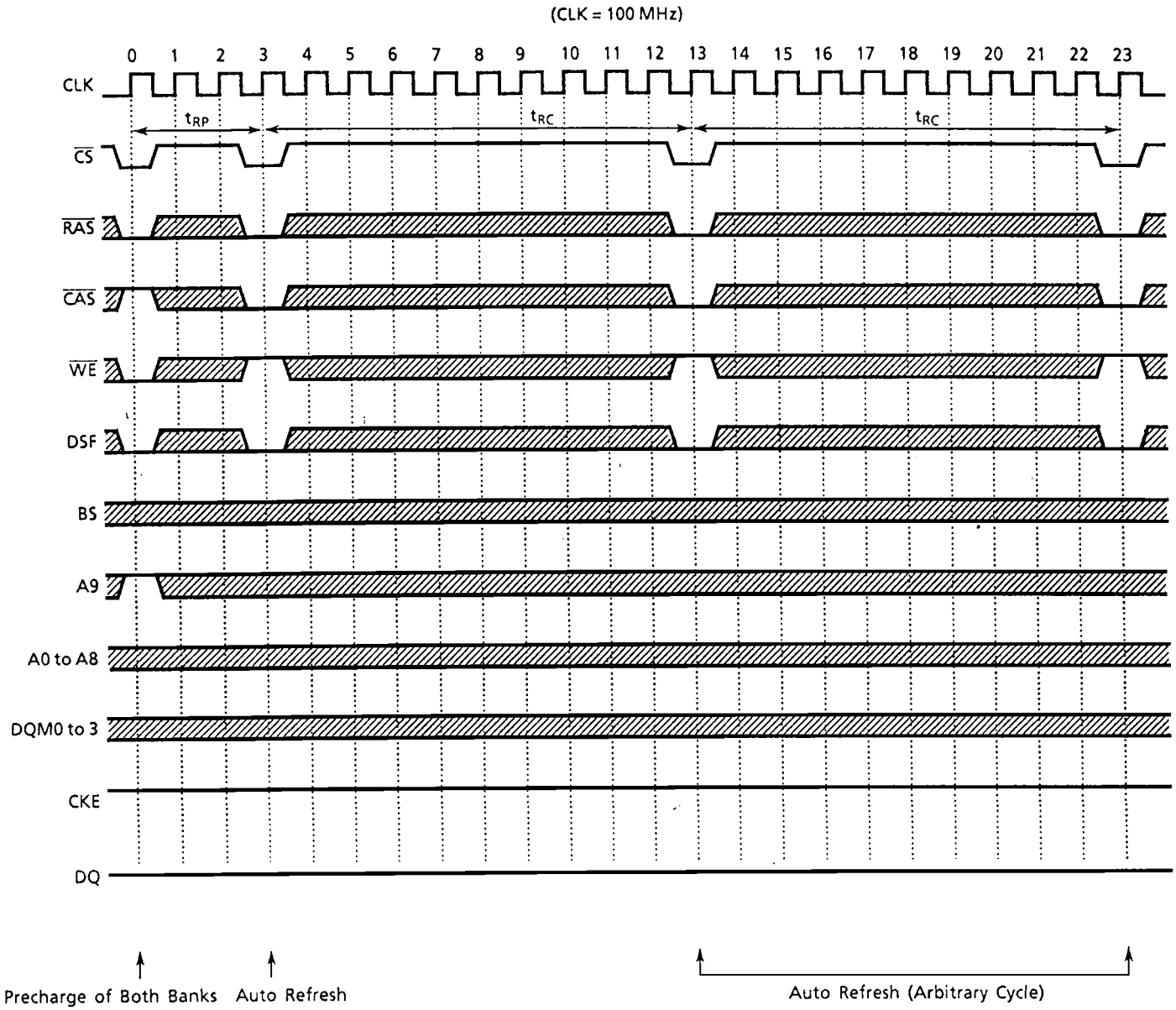
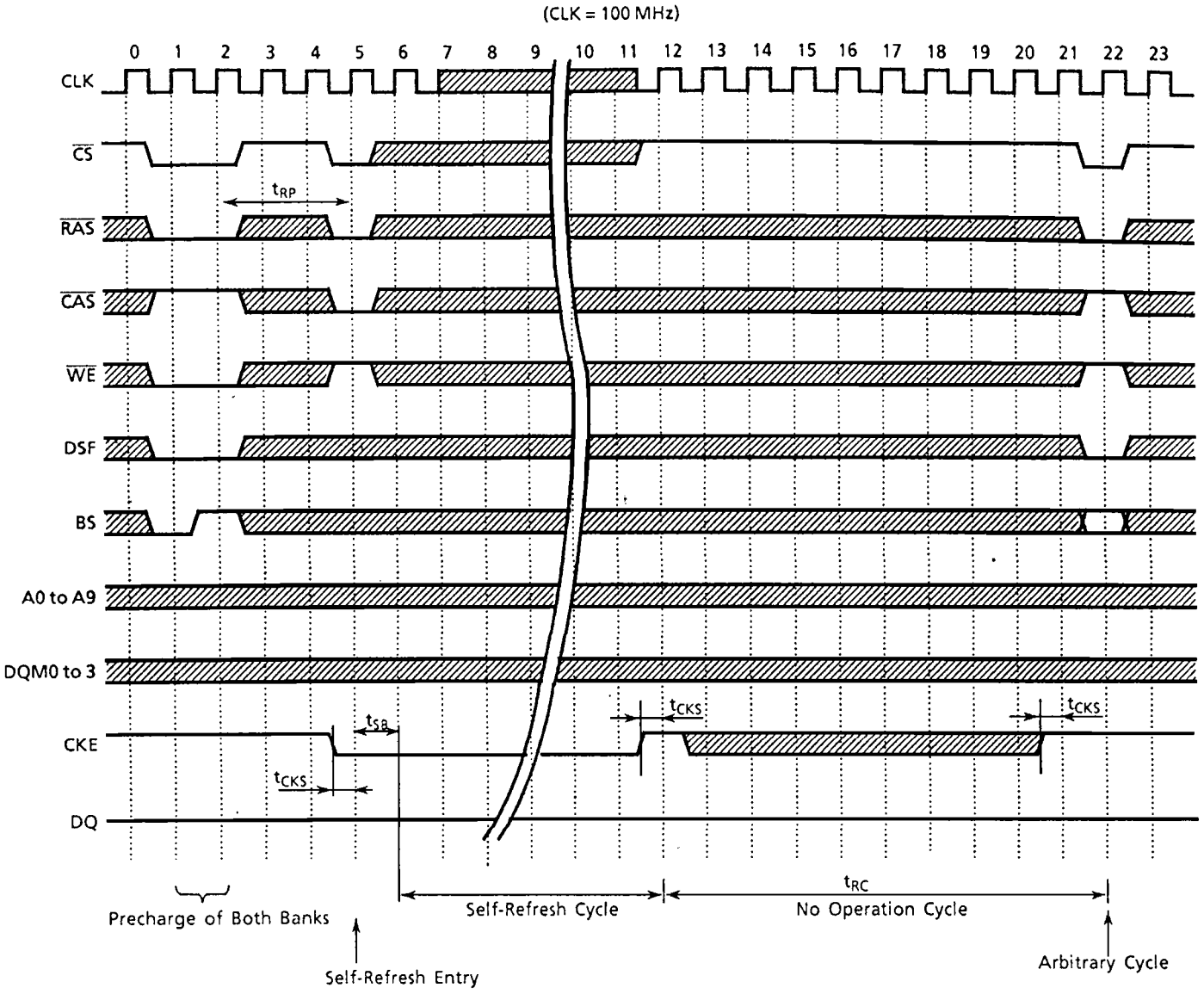
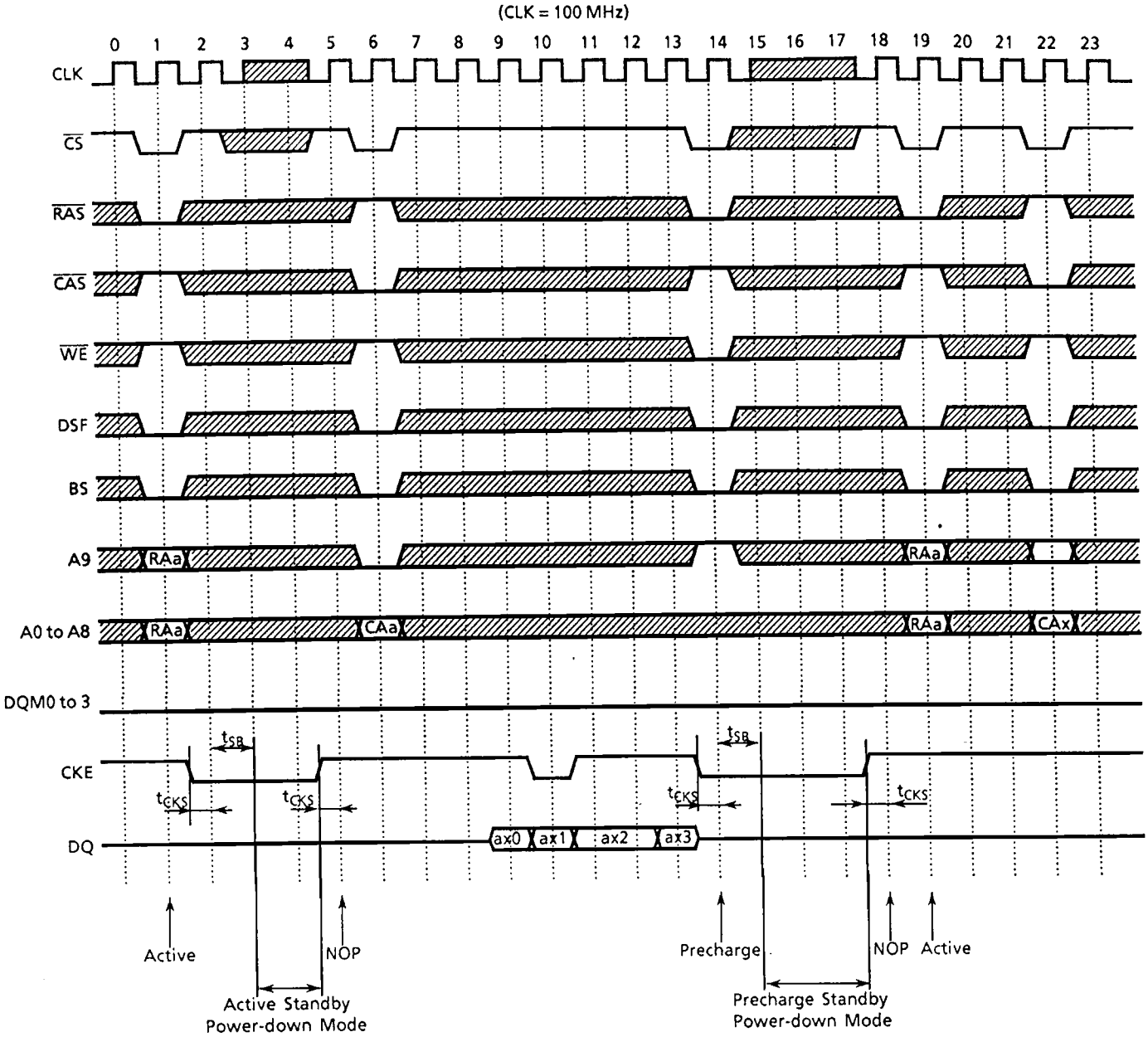


Figure 12. Self-Refresh Cycle



NOTE: See Figure 21.

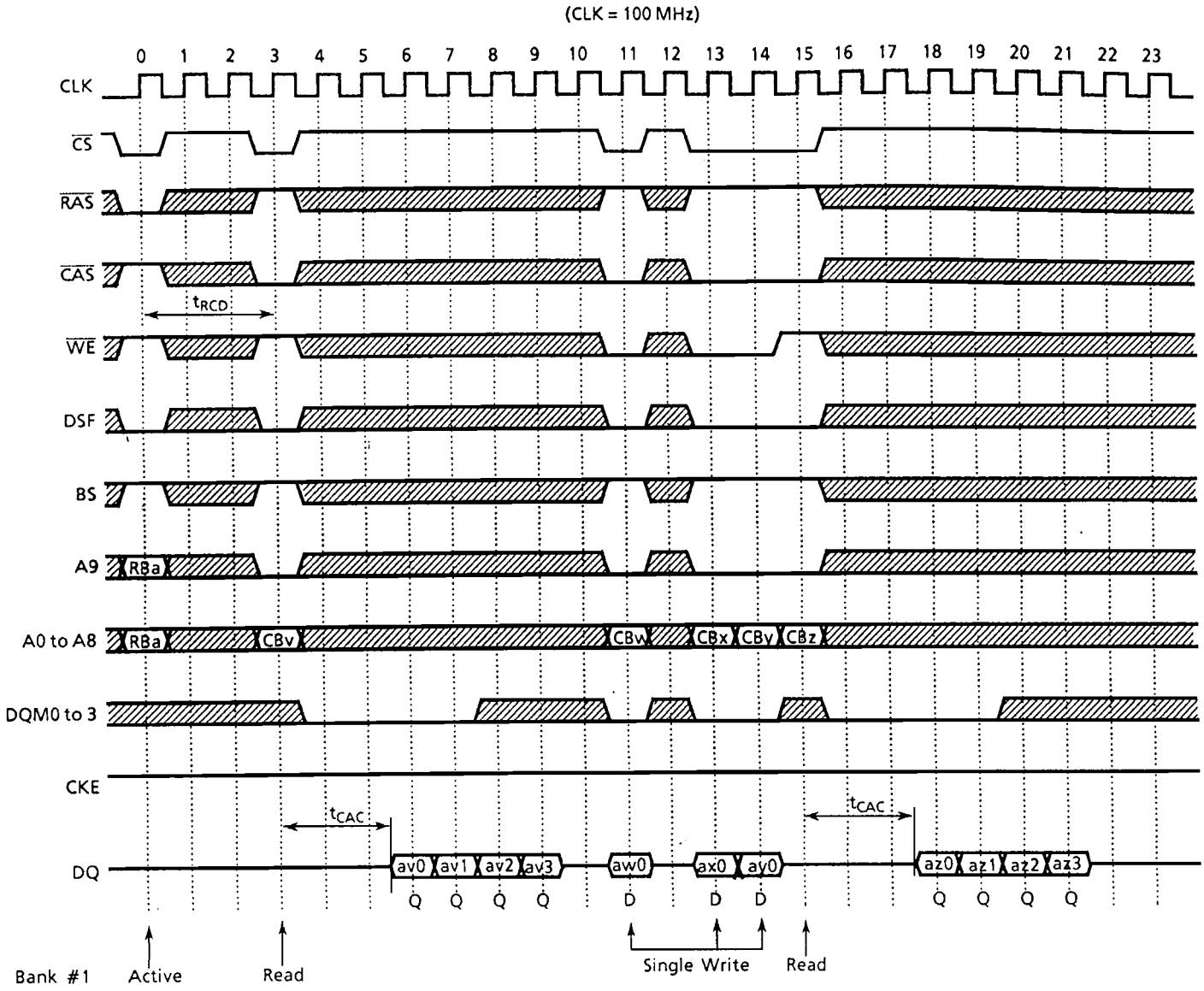
Figure 13. Power-down Mode



NOTE: Power-down mode is invoked by asserting CKE Low.
All input/output buffers (except the CKE buffer) are turned off in Power-down mode.
When CKE goes High, the No operation command must be input on the next rising edge of CLK.

See Figure 21.

Figure 14. Burst Read and Single Write (Burst Length = 4, $\overline{CAS}$ Latency = 3)



PIN FUNCTIONS

CLOCK INPUT: CLK

The CLK input is used as the reference for S-GRAM operations. All operations are synchronized to the positive edge of CLK.

CLOCK ENABLE: CKE

The CKE input is used to suspend the internal CLK. When the CKE signal is asserted Low, the internal CLK is suspended and output data is held constant. When both banks are in the Idle state, the CKE input controls initiation of the Power-down and Self-Refresh modes.

BANK SELECT: BS

The TC59G1632AFB is organized as two-bank memory cell arrays. The BS input is latched on assertion of the operation commands and selects the bank to be used for the operation. When BS is asserted Low, Bank #0 is selected. When BS is asserted High, Bank #1 is selected.

ADDRESS INPUTS: A0 to A9

The 18 address bits required to decode the 262,144 ×32 ×2 cell locations of the TC59G1632AFB are multiplexed into the 10 address input pins (A0 to A9). The 10 row address bits are latched on the Bank Activate command and the eight column address bits are latched on the Read or Write command.
Also, the A0 to A9 inputs are used to set the value of the Mode register or the Special Mode register in a Mode Register Set cycle or Special Mode Register Set cycle.

CHIP SELECT: $\overline{CS}$

The $\overline{CS}$ input controls the latching of commands on the leading edge of CLK when $\overline{CS}$ is asserted Low. No commands are latched as long as $\overline{CS}$ is held High.

ROW ADDRESS STROBE: $\overline{RAS}$

The $\overline{RAS}$ input defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ inputs, and is latched on the leading edge of CLK. When $\overline{RAS}$ and $\overline{CS}$ are asserted Low and $\overline{CAS}$ is asserted High, either the Bank Activate command or the Precharge command is selected by the $\overline{WE}$ signal. When $\overline{WE}$ is asserted High, the Bank Activate command is selected and the bank designated by BS is turned on so that it is in the Active state. When $\overline{WE}$ is asserted Low, the Precharge command is selected and the bank designated by BS is switched to the Idle state after the Precharge operation.

COLUMN ADDRESS STROBE: $\overline{CAS}$

The $\overline{CAS}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ inputs, and is latched on the leading edge of CLK. When $\overline{RAS}$ is held High and $\overline{CS}$ is asserted Low, column access is initiated by asserting $\overline{CAS}$ Low. Then, the Read or Write command is selected by asserting $\overline{WE}$ Low or High.

WRITE ENABLE: $\overline{WE}$

The $\overline{WE}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ inputs, and is latched on the leading edge of CLK. The $\overline{WE}$ input is used to select the Bank Activate or Precharge command, or the Read or Write command.

SPECIAL FUNCTION CONTROL INPUT: DSF

The DSF input defines the operation commands in conjunction with the $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ inputs, and is latched on the leading edge of CLK. The DSF input is used to select the Masked Write Disable or Enable command and the Special Mode Register Set cycle.

DATA INPUT / OUTPUT MASK: DQM0 to 3

The DQM0 to DQM3 input enables output in a Read cycle and functions as the input data mask in a Write cycle. When DQM0 to DQM3 are asserted High on the leading edge of CLK, output data is disabled after two clock cycles during a Read cycle, or input data is masked on the same clock cycle during a Write cycle.

The DQM0 to DQM3 inputs function as byte data control.

DQM0 → DQ0 to 7
DQM1 → DQ8 to 15
DQM2 → DQ16 to 23
DQM3 → DQ24 to 31

DATA INPUT / OUTPUT: DQ0 to 31

The DQ0 to DQ31 input and output data are synchronized with the leading edge of CLK.

Operation Modes

Fully synchronous operations are performed, latching commands on the leading edge of CLK. Table 1 shows the truth table for the operation commands.

Table 1. Truth Table (Notes (1) and (2))

Command	State	CKEn-1	CKEn	DQM(7)	BS	A9	A0-8	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF
Bank Active & Masked Write Disable	Idle (3)	H	X	X	V	V	V	L	L	H	H	L
Bank Active & Masked Write Enable	Idle (3)	H	X	X	V	V	V	L	L	H	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L	L
Write	Active (3)	H	X	X	V	L	V	L	H	L	L	L
Write with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	L	L
Read	Active (3)	H	X	X	V	L	V	L	H	L	H	L
Read with Auto Precharge	Active (3)	H	X	X	V	H	V	L	H	L	H	L
Mode Register Set	Idle	H	X	X	V	X	V	L	L	L	L	L
Special Mode Register Set	Idle (5)	H	X	X	X	X	V	L	L	L	L	H
No Operation	Any	H	X	X	X	X	X	L	H	H	H	X
Burst Stop	Active (4)	H	X	X	X	X	X	L	H	H	L	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H	L
Self-Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H	X
Self-Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X	X
								L	H	H	H	X
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X	X
Power-down Mode Entry	Any(6)	H	L	X	X	X	X	X	X	X	X	X
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X	X
Power-down Mode Exit	Any (Power-down)	L	H	X	X	X	X	H	X	X	X	X
								L	H	H	H	X
Data Write / Output Enable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Mask / Output Disable	Active	H	X	H	X	X	X	X	X	X	X	X

Notes: (1) V = Valid X = Don't care L = Low level H = High level
(2) CKE_n signal is the input level when the command is issued.
CKE_{n-1} signal is the input level one clock cycle before the command is issued.
(3) The bank state designated by the BS signal
(4) Device states are 1, 2, 4, 8 and Full Page Burst operation.
(5) The Special Mode Register Set operation is also available in Row Active state.
(6) Power-down mode cannot be initiated during a Burst cycle.
When this command is asserted during a Burst cycle, the device enters Clock Suspend mode.
(7) DQM0 to DQM3

1. Command Functions

1 - 1 Bank Activate & Masked Write Disable command

($\overline{RAS}$=L, $\overline{CAS}$=H, $\overline{WE}$=H, DSF=L, BS=Bank, A0 to A9=Row Address)

The Bank Activate command activates the bank designated by the BS (Bank Select) signal. Row addresses are latched on A0 to A9 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the Active state is specified by t_{RAS}. After this command is used, the Write command performs the No Mask Write operation.

1 - 2 Bank Activate & Masked Write Enable command

($\overline{RAS}$=L, $\overline{CAS}$=H, $\overline{WE}$=H, DSF=H, BS=Bank, A0 to A9=Row Address)

The Bank Activate command activates the bank designated by BS. After this command is performed, the Write command performs the Masked Write operation. In the Masked Write, the I/O mask data stored in the Write Mask register is used.

1 - 3 Bank Precharge command

($\overline{RAS}$=L, $\overline{CAS}$=H, $\overline{WE}$=L, DSF=L, BS=Bank, A9=L, A0 to A8=Don't care)

The Bank Precharge command precharges the bank designated by BS. The precharged bank is switched from the Active state to the Idle state.

1 - 4 Precharge All command

($\overline{RAS}$=L, $\overline{CAS}$=H, $\overline{WE}$=L, DSF=L, BS=Don't care, A9=H, A0 to A8=Don't care)

The Precharge All command precharges both banks simultaneously. Both banks are then switched to the Idle state.

1 - 5 Write command

($\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=L DSF=L, BS=Bank, A9=L, A0 to A7=Column Address)

The Write command performs a Write operation to the bank designated by BS. The write data is latched on the leading edge of CLK. The length of the write data (Burst Length) and the column access sequence (Addressing mode) must be set in the Mode register on power-up prior to the Write operation.

If DSF = L when the Bank Activate command is executed, then the I/O Mask for that bank is disabled, If DSF=H when the Bank Activate command is executed, then the I/O Mask for that bank is enabled.

The A8 input is Don't care.

1 - 6 Write with Auto Precharge command

($\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=L, DSF=L, BS=Bank, A9=H, A0 to A7=Column Address)

The Write with Auto Precharge command performs a Precharge operation automatically after performing a Write operation. This command must not be interrupted by any other command. The A8 input is Don't care.

1-7 Read command

($\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=H, DSF=L, BS=Bank, A9=L, A0 to A7=Column Address)

The Read command performs a Read operation on the bank designated by BS. The read data is read sequentially synchronized to the leading edge of CLK. The length of the read data (Burst Length), Addressing mode and $\overline{CAS}$ Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode register on power-up prior to the Read operation. The A8 input is Don't care.

1-8 Read with Auto Precharge command

($\overline{RAS}$=H, $\overline{CAS}$=L, $\overline{WE}$=H, DSF=L, BS=Bank, A9=H, A0 to A7=Column Address)

The Read with Autoprecharge command automatically performs a Precharge operation after performing a Read operation. This command must not be interrupted by any other command. The A8 input is Don't care.

1-9 Mode Register Set command

($\overline{RAS}$=L, $\overline{CAS}$=L, $\overline{WE}$=L, DSF=L, BS, A0 to A9=Register Data)

The Mode Register Set command sets values for the $\overline{CAS}$ latency, Addressing mode and Burst Length in the Mode register. The default values in the Mode register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while both banks are in the Idle state.

1-10 Special Mode Register Set command

($\overline{RAS}$=L, $\overline{CAS}$=L, $\overline{WE}$=L, DSF=H, BS, A0 to A4, A7 to A9=Don't care, A5, A6, DQ0 to DQ31=Register Data)

The TC59G1632AFB is provided with a 32-bit Write Mask register which provides the I/O mask data during the masked functions such as the Write per Bit function. The Special Mode Register Set command is used to load the Mask register. When A5 in the Special Mode register is High, the write mask data on the Wi/IOi pins is latched into the Write Mask register. A6 in the Special Mode register must be Low state.

1-11 No Operation command

($\overline{RAS}$=H, $\overline{CAS}$=H, $\overline{WE}$=H)

The No Operation command simply performs no operation (the same as Device Deselect).

1-12 Burst Stop command

($\overline{RAS}$=H, $\overline{CAS}$=H, $\overline{WE}$=L, DSF=L)

The Burst Stop command is used to stop a Burst operation. This command is valid during 1-, 2-, 4- and 8-word Burst and Full Page Burst operation.

1-13 Device Deselect command

($\overline{CS}$=H)

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF and Address inputs are ignored. This command is similar to the No Operation command.

1-14 Auto Refresh command

($\overline{RAS}$=L, $\overline{CAS}$=L, $\overline{WE}$=H, DSF=L, CKE=H, BS, A0 to A9=Don't care)

The Auto Refresh command is used to refresh the row address provided by the Internal Refresh counter. The two banks (#0 and #1) are refreshed alternately by the Auto Refresh command and the Refresh counter is incremented automatically. The Refresh operation must be performed 2048 times within 32 ms. The next command can then be issued t_{RC} after completion of the Auto Refresh command. When the Auto Refresh command is issued, both banks must be in the Idle state. The Auto Refresh operation is equivalent to a $\overline{CAS}$-before-$\overline{RAS}$ operation in a conventional DRAM.

1-15 Self-Refresh Entry command

($\overline{RAS}$=L, $\overline{CAS}$=L, $\overline{WE}$=H, CKE=L, DSF, BS, A0 to A9=Don't care)

The Self-Refresh Entry command is used to enter Self-Refresh mode. While the device is in Self-Refresh mode, all input and output buffers (except the CKE buffer) are disabled and the Refresh operation is automatically performed. Self-Refresh mode is terminated by taking CKE High (the Self-Refresh Exit command)

1-16 Self-Refresh Exit command

(CKE=H, $\overline{CS}$=H or CKE=H, $\overline{RAS}$=H, $\overline{CAS}$=H, DSF=Don't care)

This command is used to exit Self-Refresh mode. Any subsequent commands can be issued t_{RC} after completion of this command.

1-17 Clock Suspend Mode Entry / Power-down Mode Entry commands

(CKE= L)

When either bank is in the Active state, the internal CLK is suspended for one cycle when this command is issued (when CKE is asserted Low). The device state remains unchanged while the CLK is suspended. Alternatively, when both banks are in the Idle state, this command initiates Power-down mode. All input and output buffers (except the CKE buffer) are turned off in Power-down mode.

1-18 Clock Suspend Mode Exit / Power-down Mode Exit commands

(CKE= H)

If the internal CLK has been suspended, operation of the internal CLK can be resumed by invoking this command (asserting CKE High). When the device is in Power-down mode, the device exits this mode and all disabled buffers are put into the Active state. Any subsequent commands can be issued t_{CK}(min)+t_{CKS}(min) after completion of this command.

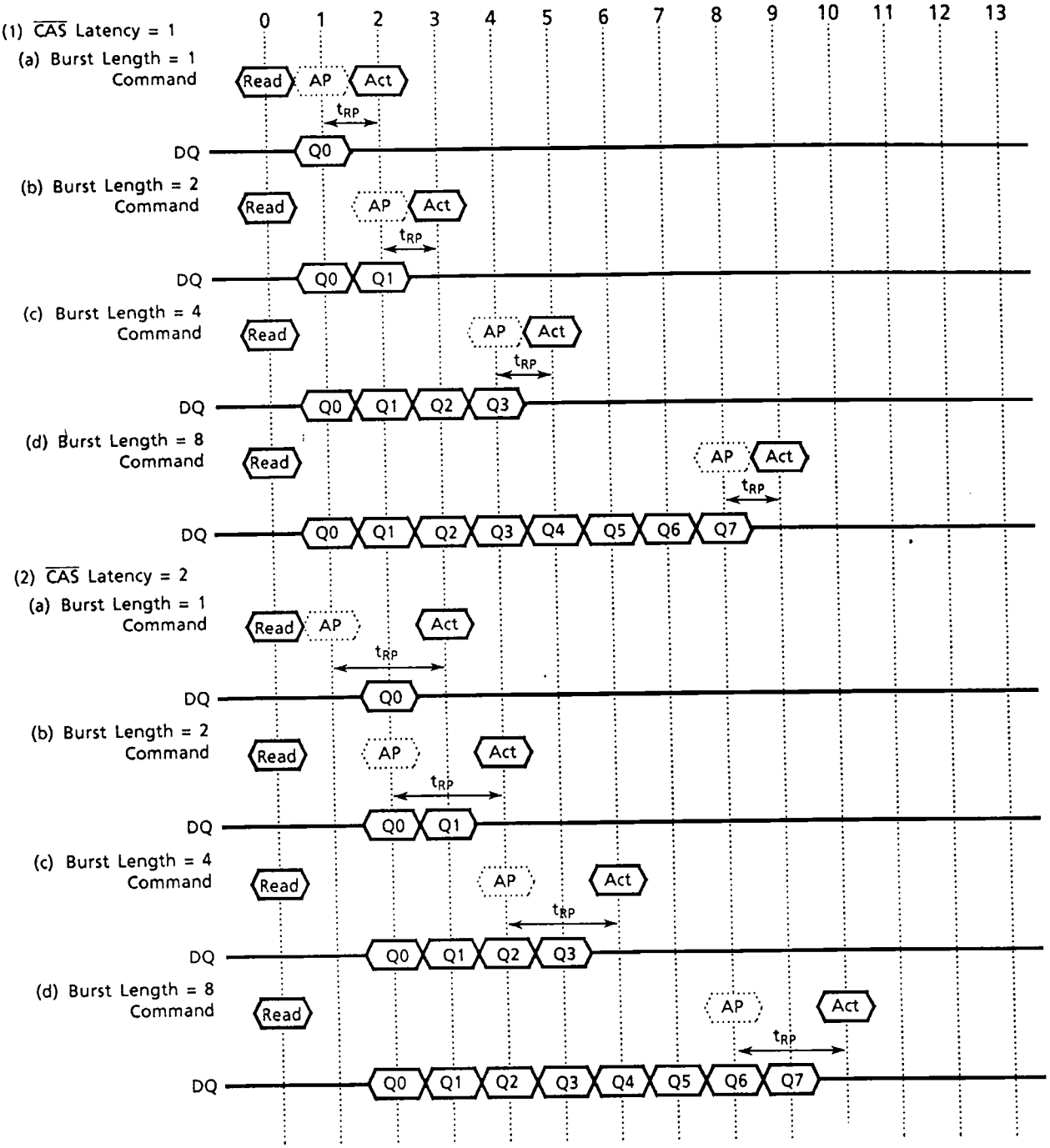
1-19 Data Write / Output Enable, Data Mask / Output Disable commands

(DQM= L / H)

During a Write cycle, the DQM signals function as a data mask and can control every word of the input data. During a Read cycle, the DQM signals control the output buffers.

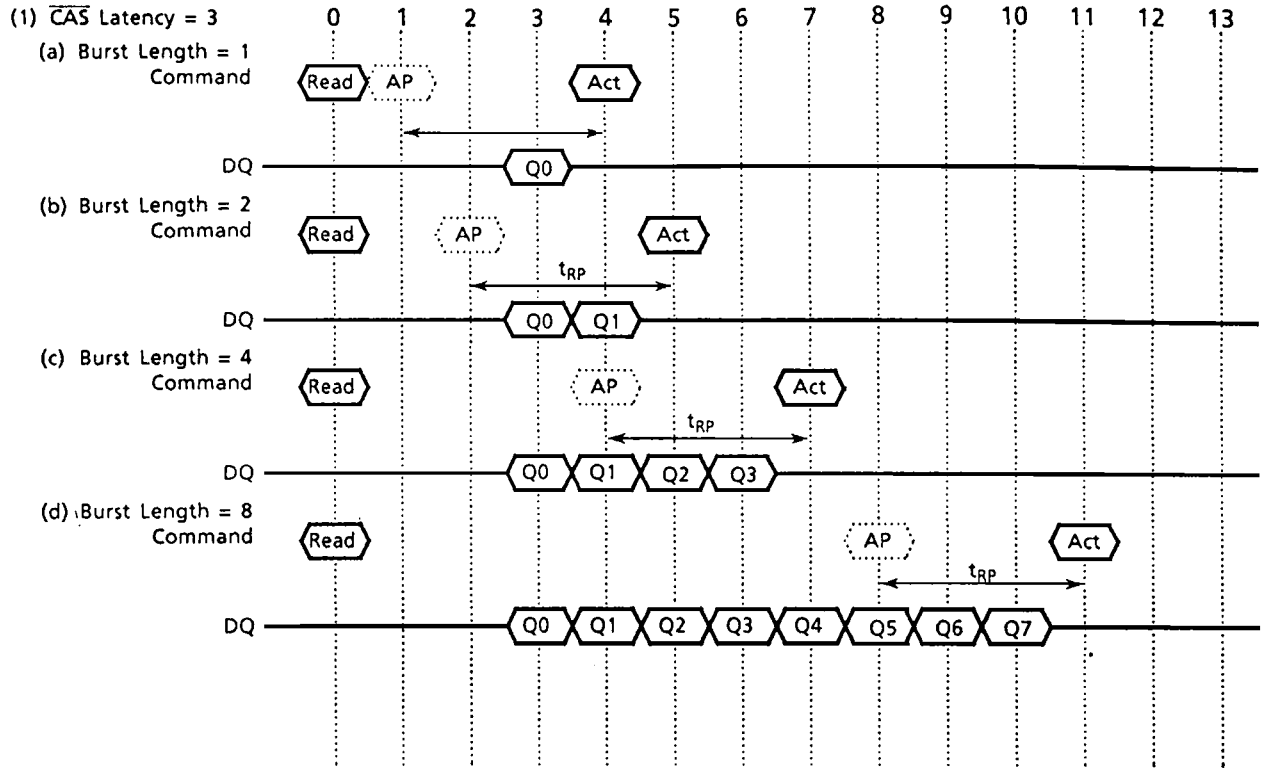
DQM0 to DQM3 are used for byte control. The inputs DQM0 to DQM3 correspond to DQ0 to 7, DQ8 to 15, DQ16 to 23 and DQ24 to 31 respectively. During Write-per-Bit operation, the Mask data on DQM0 to DQM3 takes priority over the data in the Write Mask register.

Figure 15-1. Auto Precharge timing (Read cycle)



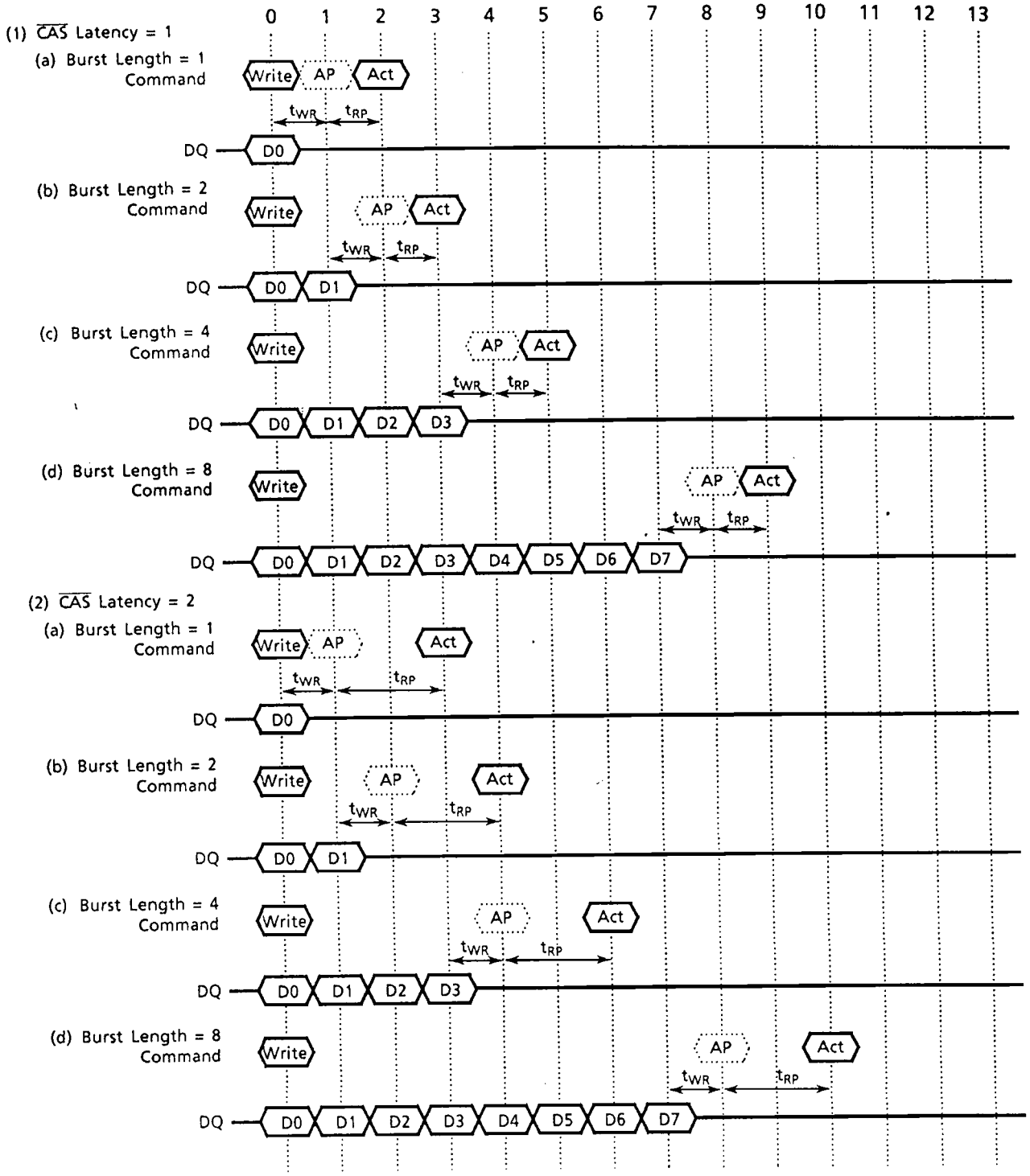
NOTES:
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from the Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 15-2. Auto Precharge timing (Read cycle)



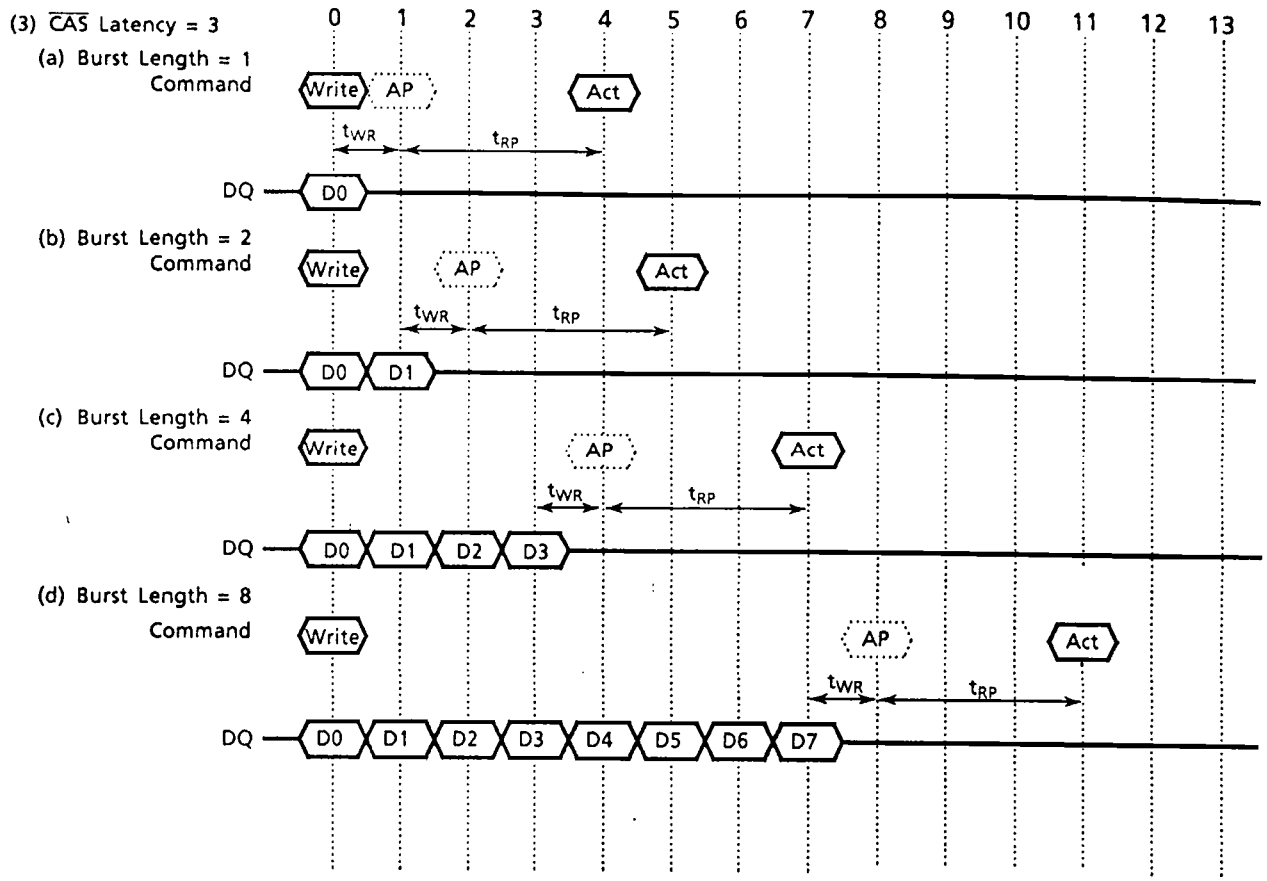
NOTES:
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from the Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 16-1. Auto Precharge timing (Write cycle)



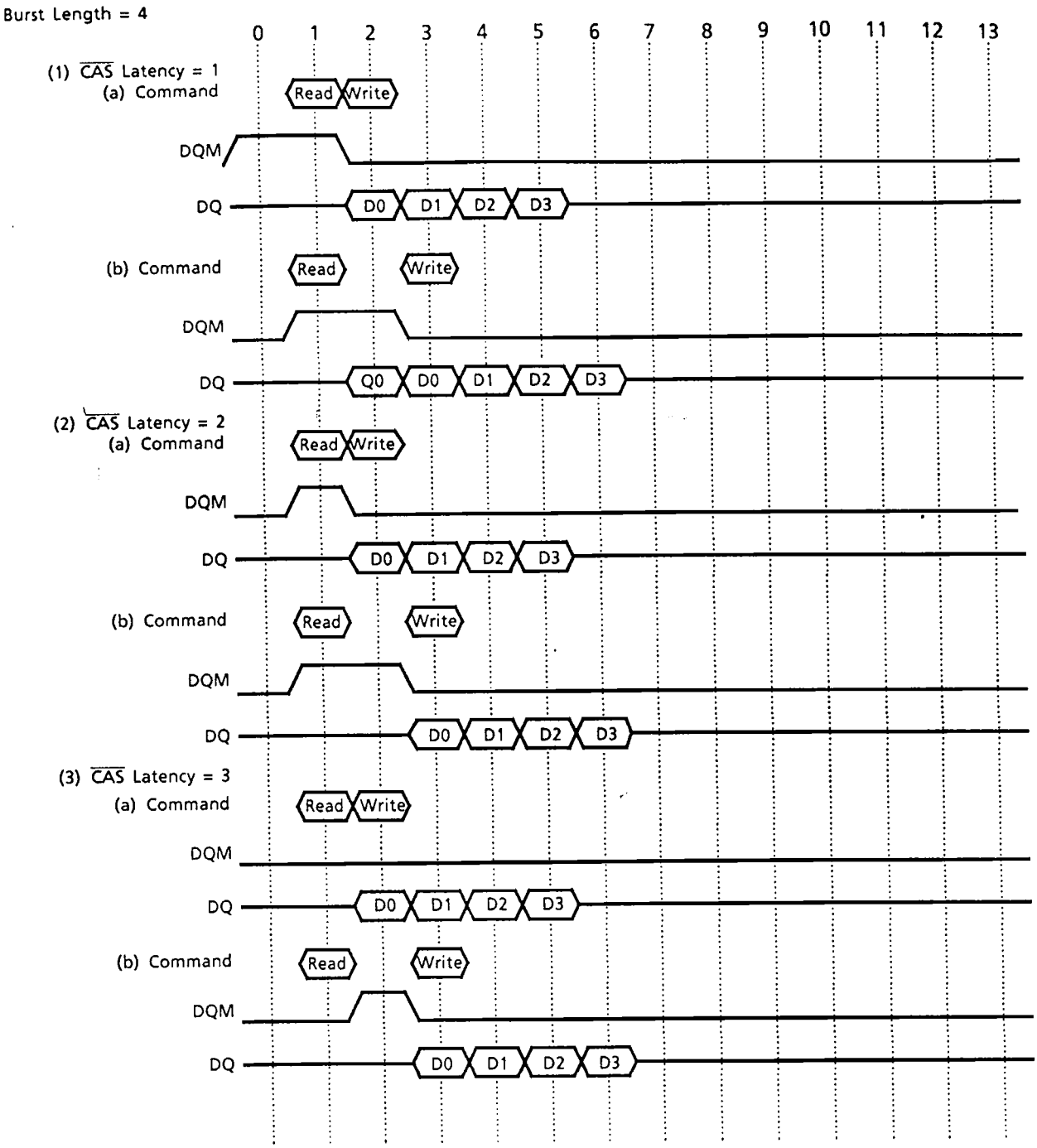
NOTES:
- Write represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from the Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 16-2. Auto Precharge timing (Write cycle)



NOTES:
- Write represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from the Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 17. Timing chart for Read-to-Write cycle



NOTE: • The output data must be masked by DQM to avoid I/O conflict.

Figure 18. Timing chart for Write-to-Read cycle

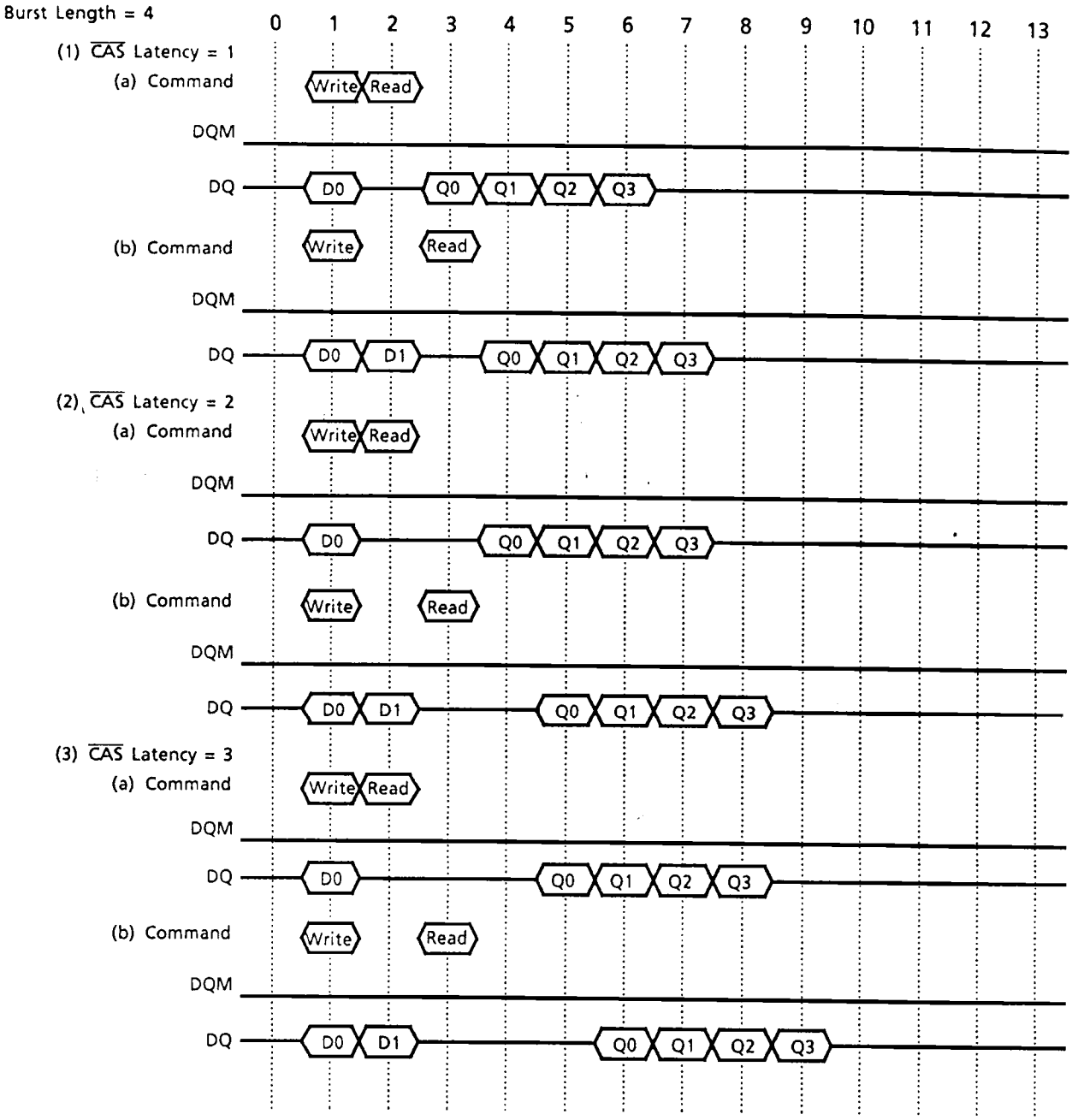
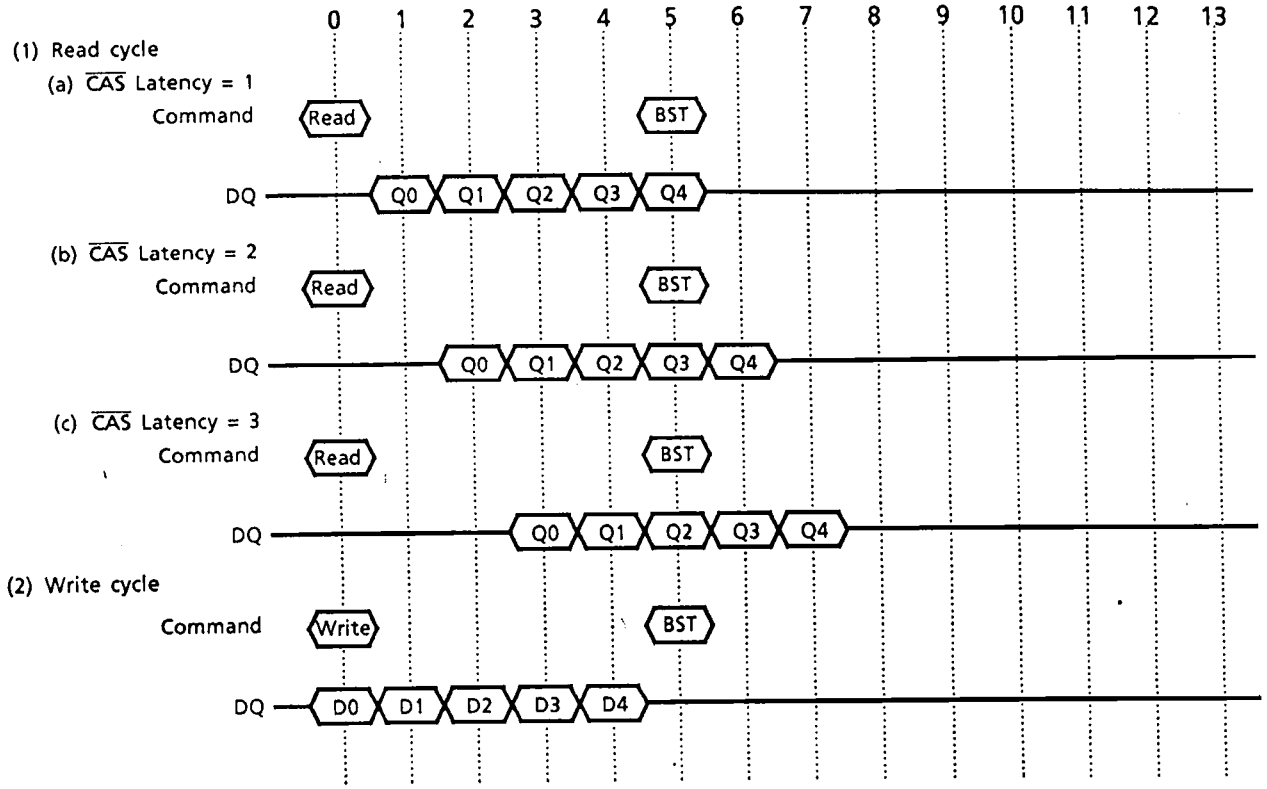


Figure 19. Timing chart for Burst Stop cycle (Burst Stop command)



NOTES: • BST represents the Burst Stop command.

• The Burst Stop command is effective in 1-, 2-, 4- and 8-word bursts and in a Full Page cycle.

Figure 20-1. Timing chart for Burst Stop cycle (Precharge command)

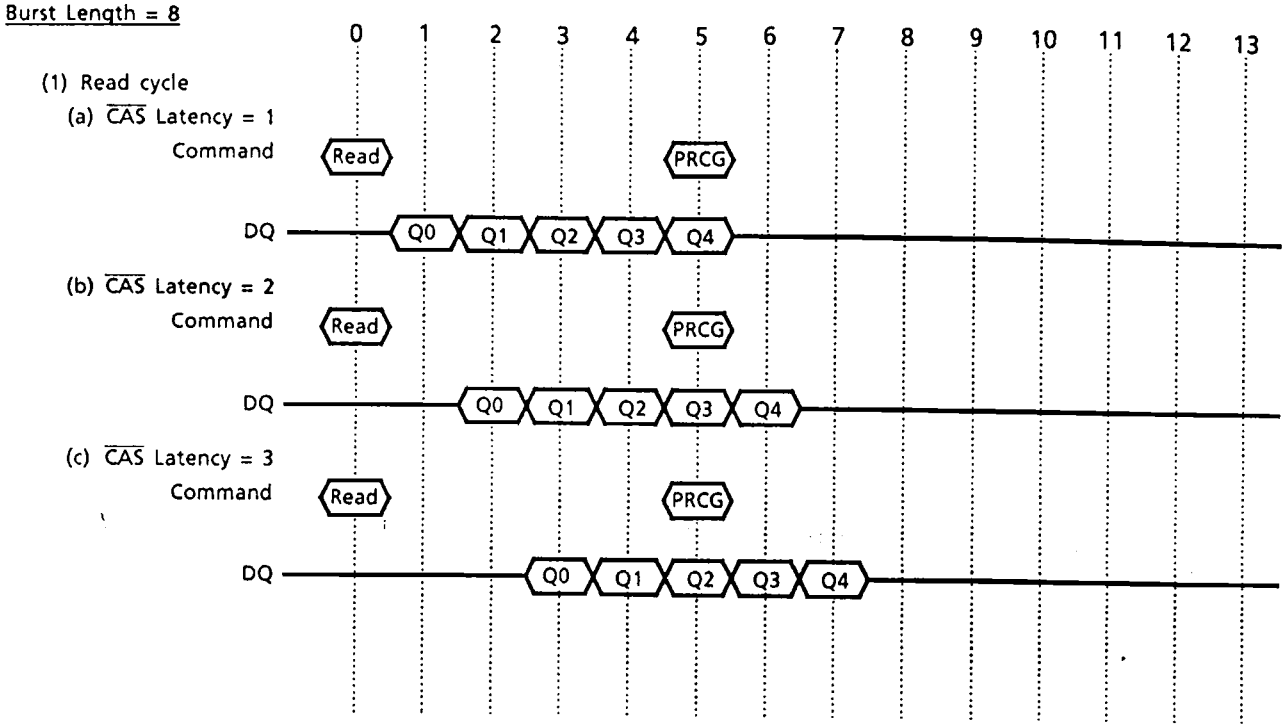
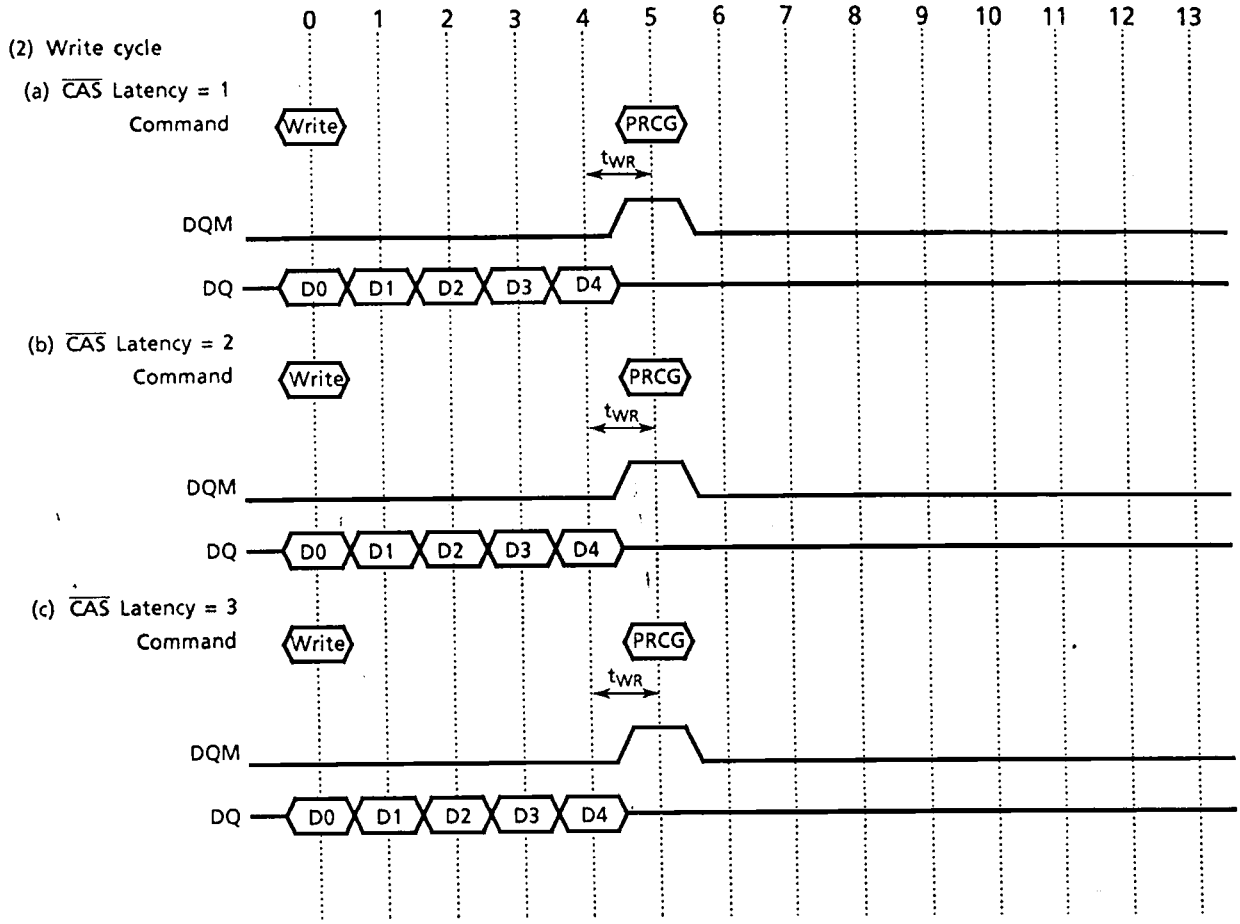


Figure 20-2. Timing chart for Burst Stop cycle (Precharge command)

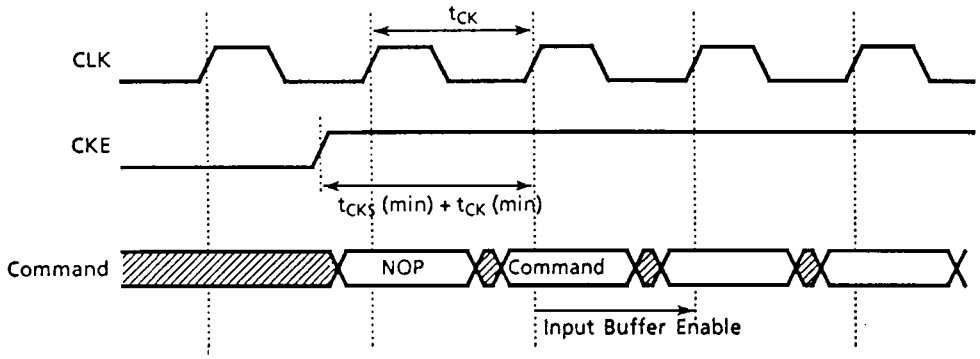


NOTE: • PRCG represents the Precharge command.

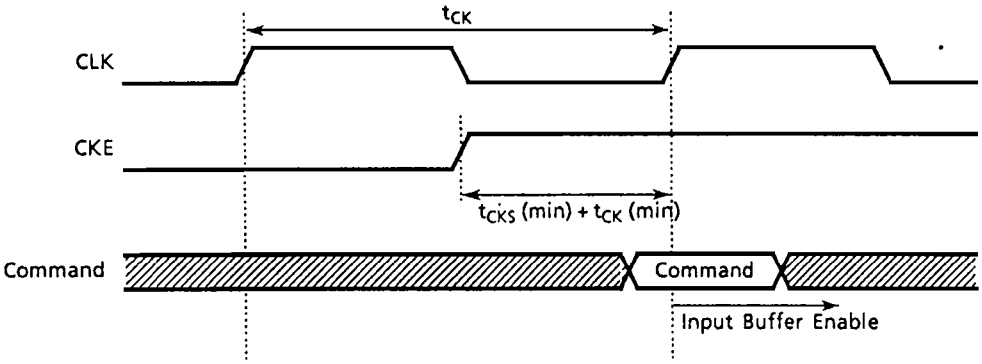
Figure 21. Self-Refresh/Power-down Mode Exit Timing

- Asynchronous Control
  Input Buffer turn-on time (Power-down mode exit time) is specified by t_{CKS} (min) + t_{CK} (min).

A) $t_{CK} < t_{CKS}$ (min) + t_{CK} (min)



B) $t_{CK} \geq t_{CKS}$ (min) + t_{CK} (min)



NOTES:
- All input buffers (including the CLK buffer) are turned off in Power-down mode and Self-Refresh mode.
- NOP represents the No Operation command.
- Command represents a single command.

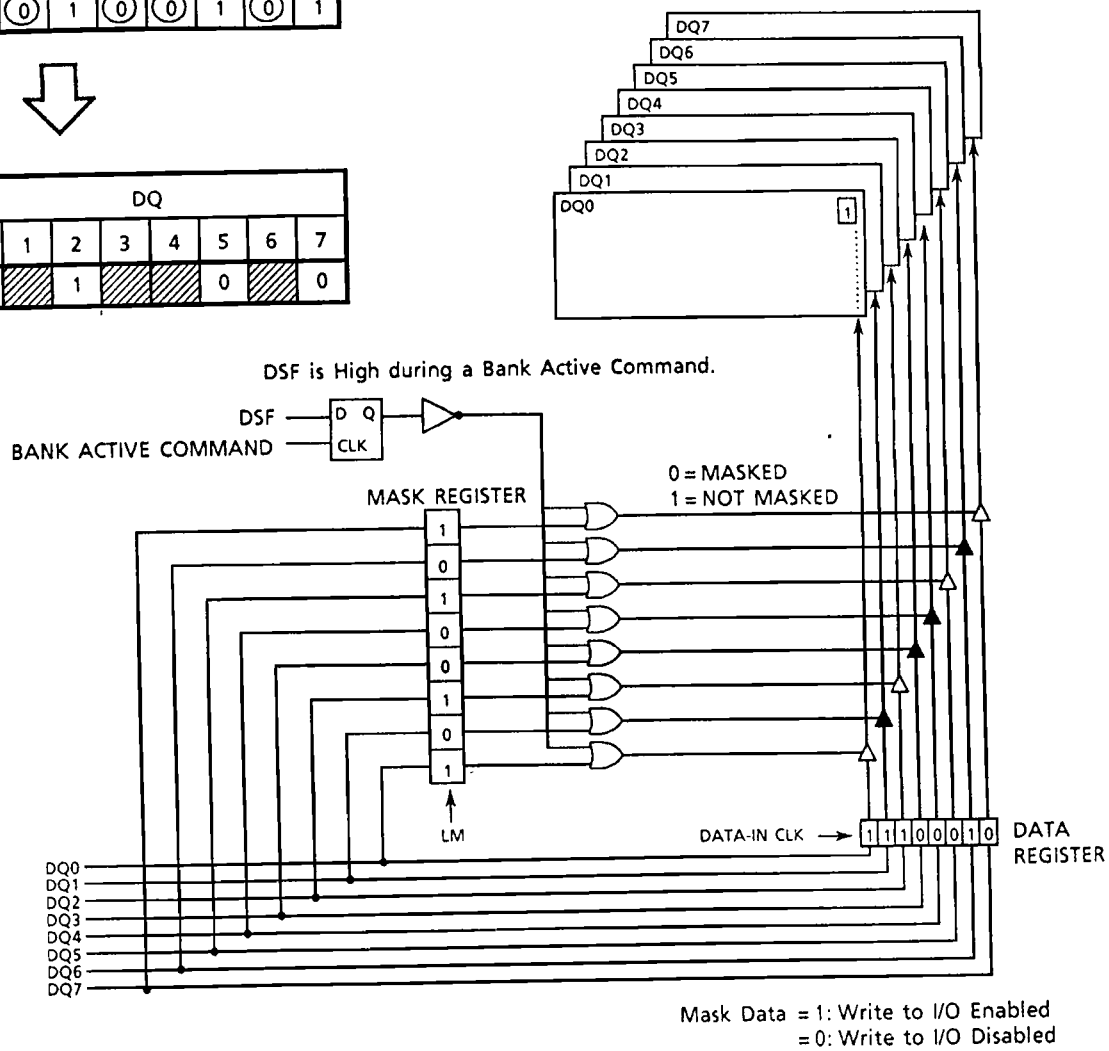
Figure 22. Write-per-Bit

Example (Only the laest significant byte is shown. The operation is identical for all other bytes.)

	DQ							
	0	1	2	3	4	5	6	7
Data - in	1	1	1	0	0	0	1	0
Mask Register (LM)	1	(0)	1	(0)	(0)	1	(0)	1

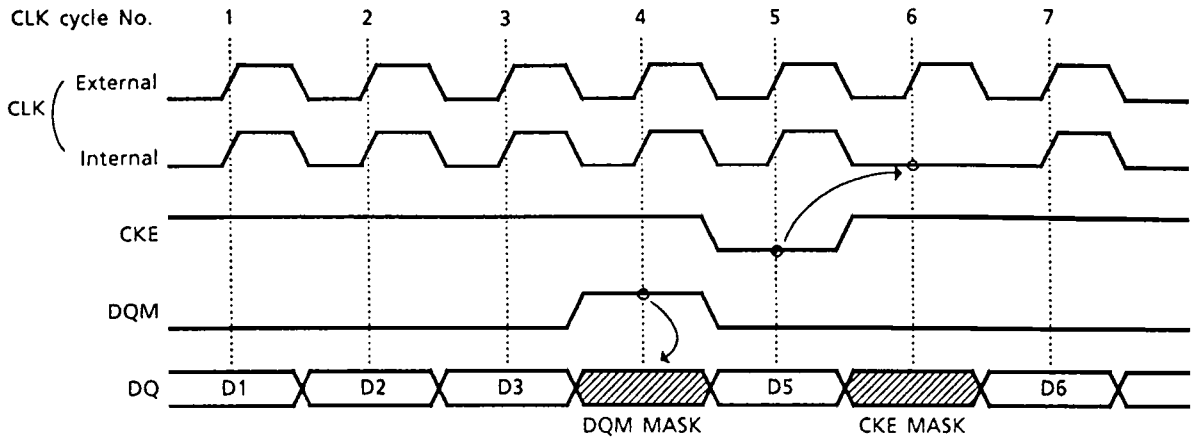
Result

	DQ							
	0	1	2	3	4	5	6	7
Write Data	1		1			0		0

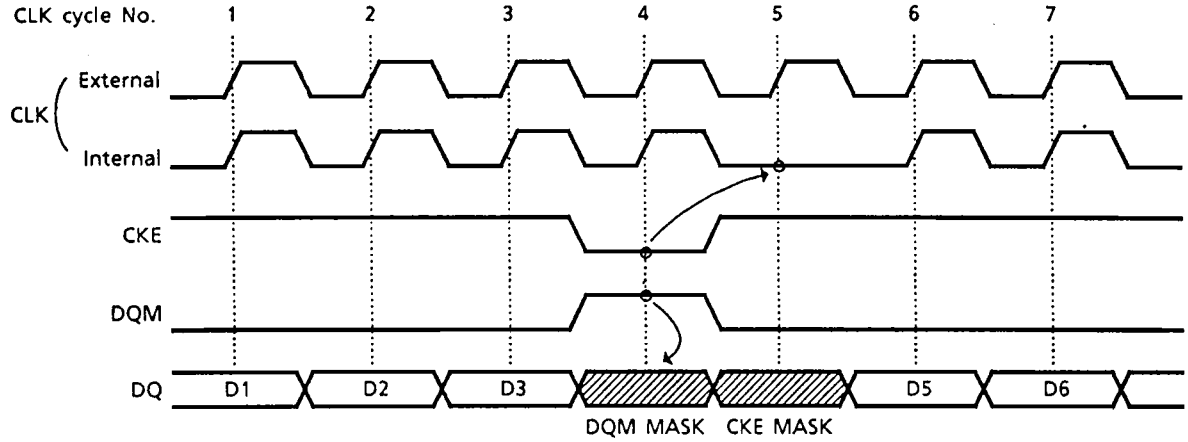


NOTES:
- The Write-per-Bit can be performed in a burst.
- If DSF = L when the Bank Active command is executed, then the I/O Mask is disabled for the active bank.
  If DSF = H when the Bank Active command is executed, then the I/O Mask is enabled for the active bank.
- Mask Data = Mask Register + DQMi (i = 0 to 3)

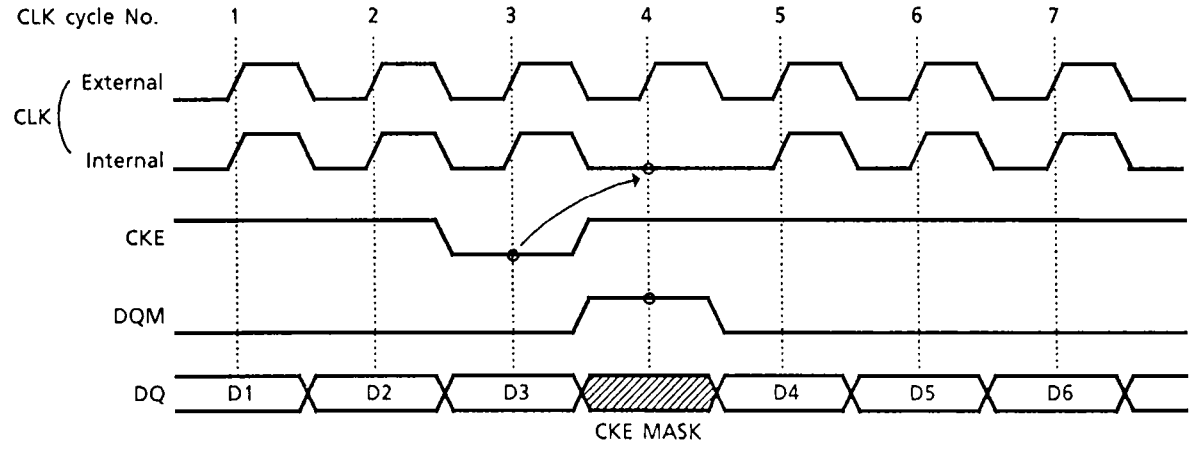
Figure 23 (a). CKE/DQM input timing (Write cycle)



(1)

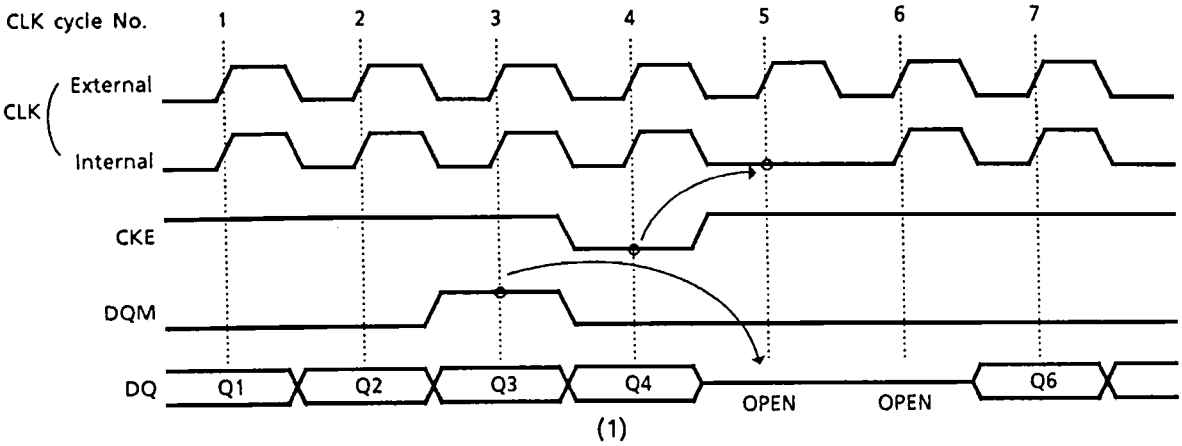


(2)

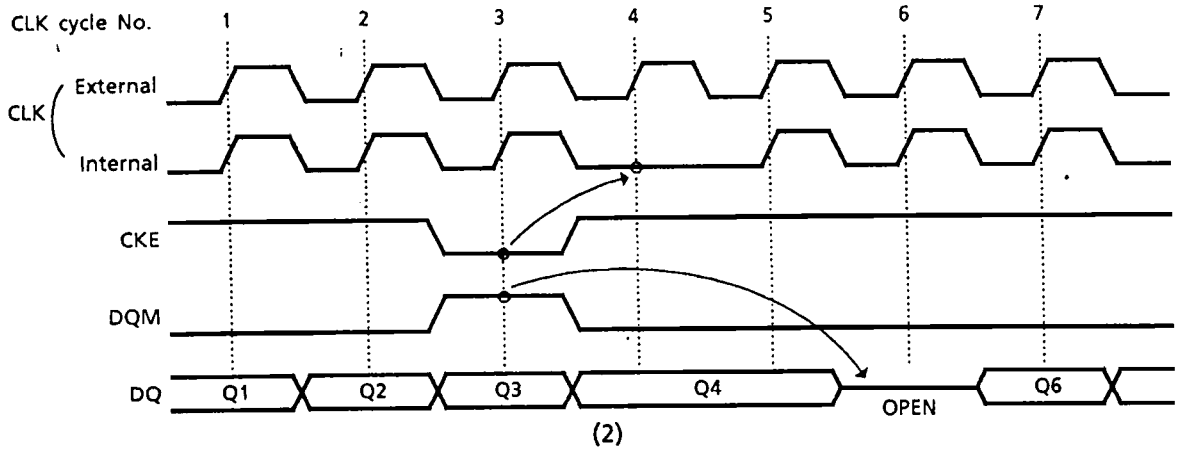


(3)

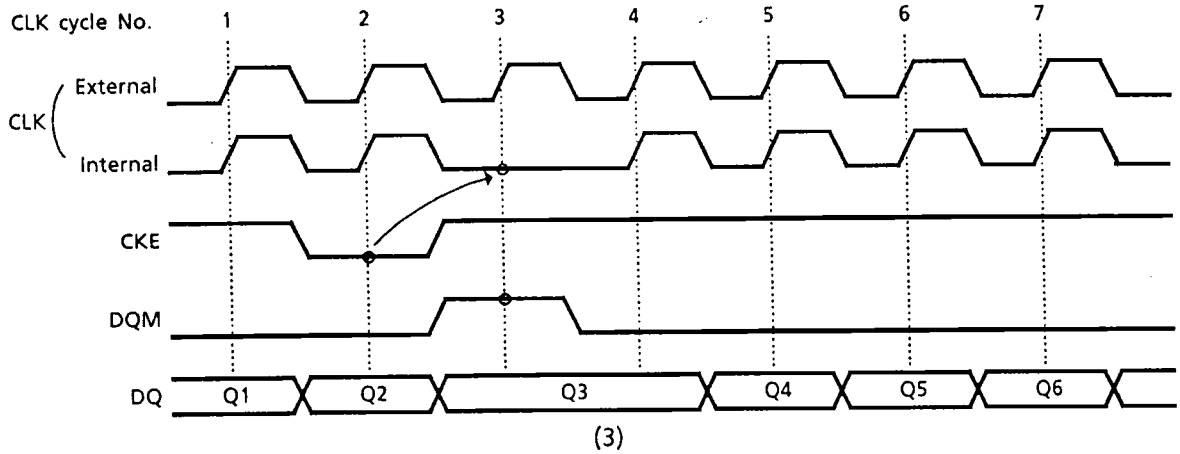
Figure 23 (b). CKE, DQM input timing (Read cycle)



(1)



(2)



(3)

PACKAGE DIMENSIONS (TQFP100-P-1420-0.65A)

Units : mm