M74HC173P/FP/DP

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

DESCRIPTION

The M74HC173 is a semiconductor integrated circuit consisting of a 4-bit register with 3-state output.

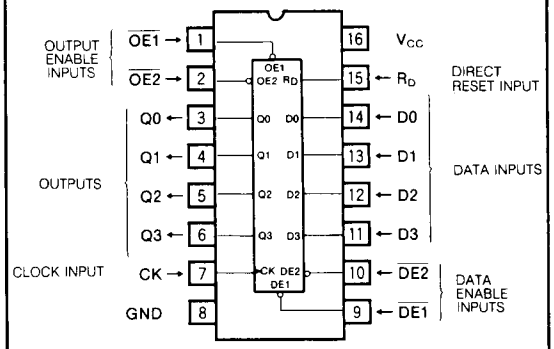
FEATURES

- High-speed: (clock frequency) 60MHz typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation: 20μW/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin: 30% of V_{CC}, min (V_{CC}=4.5V, 6V)
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range: V_{CC}=2~6V
- Wide operating temperature range: T_a=−40~+85℃

APPLICATION

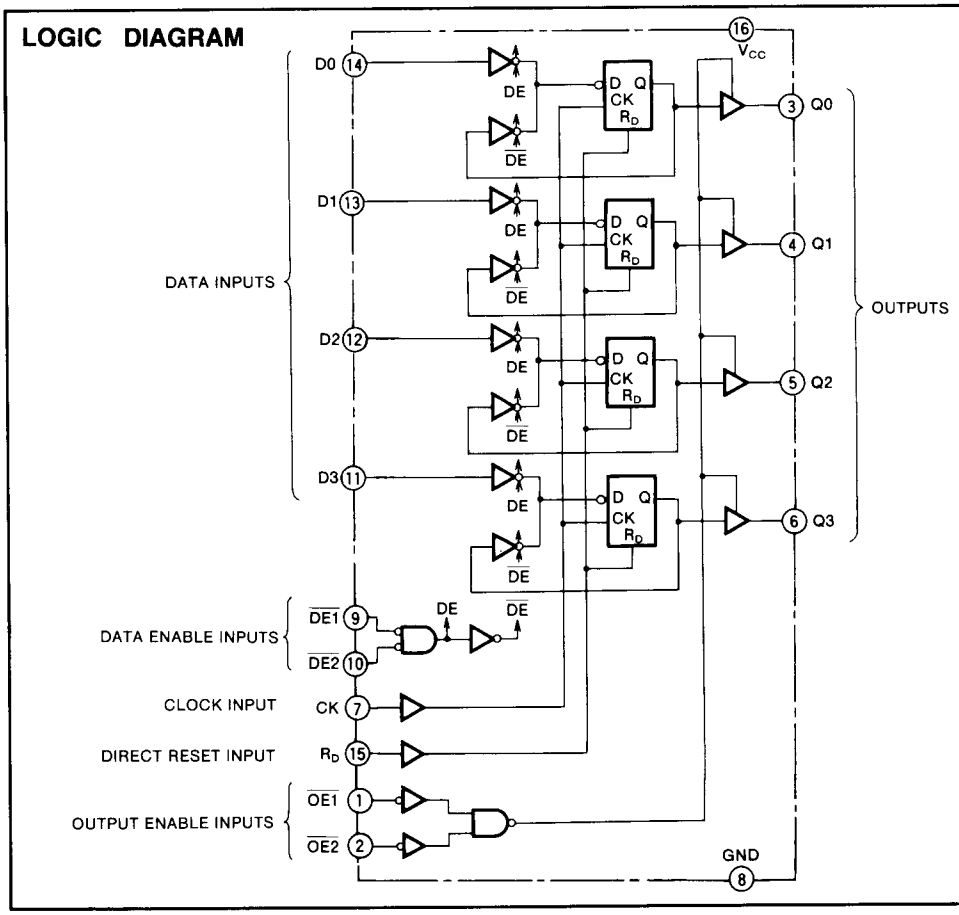
General purpose, for use in industrial and consumer digital equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4, 16P2N, 16P2P

LOGIC DIAGRAM



QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC173 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS173.

The M74HC173 contains four edge-triggered D-type flip-flops with common direct reset input R_D and common clock input CK.

When CK changes from low-level to high-level, the signals just previously input at D appears at outputs Q in accordance with the function table given.

When R_D becomes high while output enable inputs $\overline{OE1}$ and $\overline{OE2}$ are held low, all outputs Q become low-level irrespective of other inputs.

When one of data enable inputs $\overline{DE1}$ or $\overline{DE2}$ is high, while $\overline{OE1}$, $\overline{OE2}$ and R_D are held low, output Q is maintained.

When either $\overline{OE1}$ or $\overline{OE2}$ is high, all outputs Q will become the high-impedance state, and the contents of the flip-flop are not affected even when $\overline{OE1}$ and $\overline{OE2}$ are changed.

When used as a D-type flip-flop, $\overline{OE1}$, $\overline{OE2}$, R_D, $\overline{DE1}$ and $\overline{DE2}$ should all be maintained at low-level.

FUNCTION TABLE (Note 1)

Inputs							Output
$\overline{OE1}$	$\overline{OE2}$	R_D	CK	$\overline{DE1}$	$\overline{DE2}$	D	Q
L	L	H	X	X	X	X	L
L	L	L	L	X	X	X	Q^0
L	L	L	H	X	X	X	Q^0
L	L	L	↑	H	X	X	Q^0
L	L	L	↑	X	H	X	Q^0
L	L	L	↑	L	L	L	L
L	L	L	↑	L	L	H	H
L	L	L	↓	X	X	X	Q^0
L	H	X	X	X	X	X	Z
H	L	X	X	X	X	X	Z
H	H	X	X	X	X	X	Z

Note 1 : Z : High impedance
X : Irrelevant
↑ : Change from low to high level
↓ : Change from high to low level
Q_0 : Output state Q before clock input changed.

ABSOLUTE MAXIMUM RATINGS (T_a = −40∼+85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5∼+7.0	V
V_I	Input voltage		−0.5∼V_{CC}+0.5	V
V_O	Output voltage		−0.5∼V_{CC}+0.5	V
I_{IK}	Input protection diode current	V_I < 0V	−20	mA
		V_I > V_{CC}	20	
I_{OK}	Output parasitic diode current	V_O < 0V	−20	mA
		V_O > V_{CC}	20	
I_O	Output current per output pin		±35	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±75	mA
P_d	Power dissipation	(Note 2)	500	mW
Tstg	Storage temperature range		−65∼+150	℃

Note 2 : M74HC173FP, T_a = −40∼+70℃ and T_a = 70∼85℃ are derated at −7mW/℃
M74HC173DP, T_a = −40∼+50℃ and T_a = 50∼85℃ are derated at −5mW/℃

RECOMMENDED OPERATING CONDITIONS (T_a = −40∼+85℃)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature range		−40		+85	℃
t_r, t_f	Input risetime, falltime	V_{CC} = 2.0V	0		1000	ns
		V_{CC} = 4.5V	0		500	
		V_{CC} = 6.0V	0		400	

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits					Unit
					25℃		−40～+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
V_{IH}	High-level input voltage	V_O = 0.1V, V_{CC}−0.1V I_O = 20μA	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	V_O = 0.1V, V_{CC}−0.1V I_O = 20μA	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	V_I = V_{IH}, V_{IL}	I_{OH} = −20μA	2.0	1.9			1.9		V
			I_{OH} = −20μA	4.5	4.4			4.4		
			I_{OH} = −20μA	6.0	5.9			5.9		
			I_{OH} = −6.0mA	4.5	4.18			4.13		
			I_{OH} = −7.8mA	6.0	5.68			5.63		
V_{OL}	Low-level output voltage	V_I = V_{IH}, V_{IL}	I_{OL} = 20μA	2.0		0.1		0.1	V
			I_{OL} = 20μA	4.5		0.1		0.1	
			I_{OL} = 20μA	6.0		0.1		0.1	
			I_{OL} = 6.0mA	4.5		0.26		0.33	
			I_{OL} = 7.8mA	6.0		0.26		0.33	
I_{IH}	High-level input current	V_I = 6V		6.0		0.1		1.0	μA
I_{IL}	Low-level input current	V_I = 0V		6.0		−0.1		−1.0	μA
I_{OZH}	Off-state high-level output current	V_I = V_{IH}, V_{IL}, V_O = V_{CC}		6.0		0.5		5.0	μA
I_{OZL}	Off-state low-level output current	V_I = V_{IH}, V_{IL}, V_O = GND		6.0		−0.5		−5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC}, GND, I_O = 0μA		6.0		4.0		40.0	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 50pF (Note 4)	30			MHz
t_{TLH}	Low-level to high-level and high-level to low-level output transition time				10	ns
t_{THL}					10	ns
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)				31	ns
t_{PHL}					31	ns
t_{PHL}	High-level to low-level output propagation time (R_D − Q)				27	ns
t_{PLZ}	Low-level, high-level output disable time ($\overline{OE}$ − Q)	C_L = 5 pF (Note 4)			25	ns
t_{PHZ}					25	ns
t_{PZL}	Low-level, high-level output enable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)			28	ns
t_{PZH}					28	ns

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
f_{max}	Maxmum clock frequency	C_L = 50pF (Note 4)	2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	C_L = 50pF (Note 4)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{THL}			2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
t_{PLH}	Low-level to high-level and high-level to low-level output propagation time (CK − Q)	C_L = 50pF (Note 4)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PHL}			2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
t_{PLH}		C_L = 150pF (Note 4)	2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}			2.0			225		284	ns
			4.5			45		57	
			6.0			38		48	
t_{PHL}	High-level to low-level output propagation time (R_D − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PLZ}	Low-level, high-level output disable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PHZ}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}	Low-level, high-level output enable time ($\overline{OE}$ − Q)	C_L = 50pF (Note 4)	2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZH}			2.0			150		189	ns
			4.5			30		38	
			6.0			26		32	
t_{PZL}		C_L = 150pF (Note 4)	2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
t_{PZH}			2.0			200		252	ns
			4.5			40		50	
			6.0			34		43	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{OE}$ = V_{CC}				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				45				pF

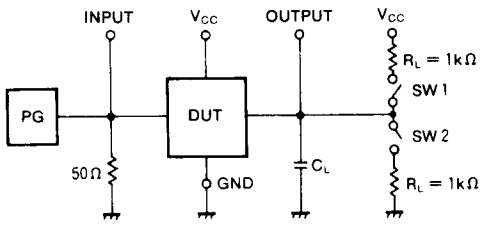
Note 3 : C_{DP} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip-flop)
The power dissipated during operation under no-load conditions is calculated using the following formula:
$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$

QUADRUPLE 3-STATE D-TYPE FLIP-FLOP WITH COMMON CLOCK AND RESET

TIMING REQUIREMENTS (V_{CC} = 2~6V, T_a = −40~+85℃)

Symbol	Parameter	Test conditions		Limits					Unit
				25℃			−40~+85℃		
			V_{CC}(V)	Min	Typ	Max	Min	Max	
t_w	CK, R_D Clock pulse width		2.0	80			101		ns
			4.5	16			20		
			6.0	14			17		
t_{su}	D, $\overline{DE}$ setup time with respect to CK		2.0	100			126		ns
			4.5	20			25		
			6.0	17			21		
t_h	D, $\overline{DE}$ hold time with respect to CK		2.0	0			0		ns
			4.5	0			0		
			6.0	0			0		
t_{rec}	R_D recovery time with respect to CK		2.0	90			113		ns
			4.5	18			23		
			6.0	15			19		

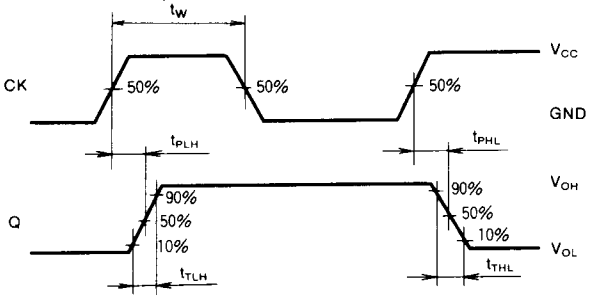
Note 4 : Test Circuit

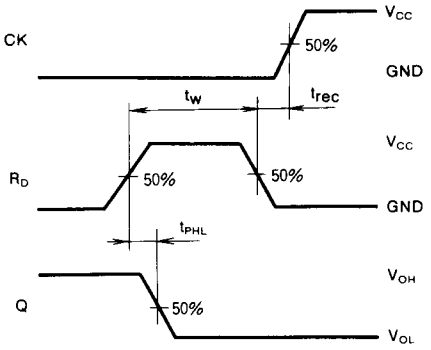


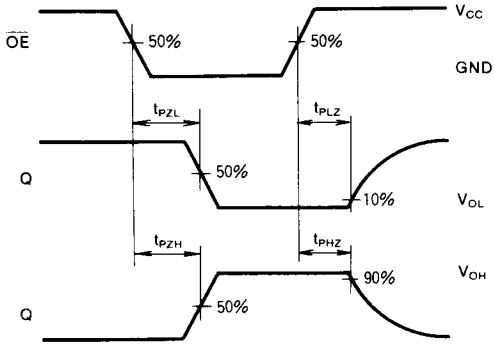
Parameter	SW 1	SW 2
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

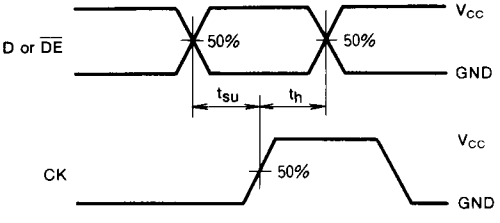
(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r = 6ns, t_f = 6ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM







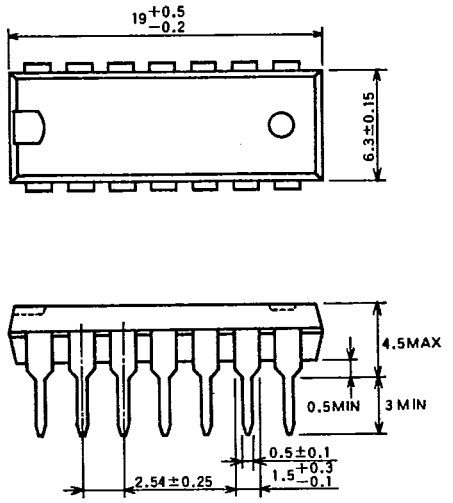


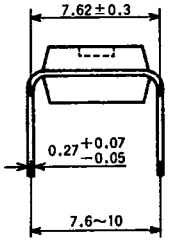
MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

TYPE 14P4 14-PIN MOLDED PLASTIC DIP

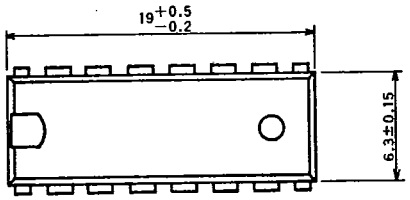
Dimension in mm

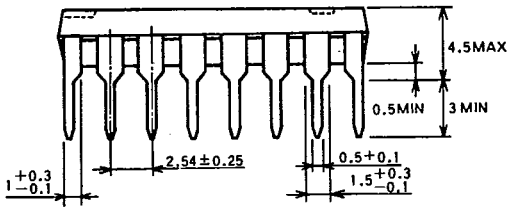


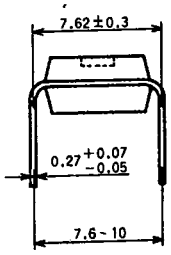


TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm





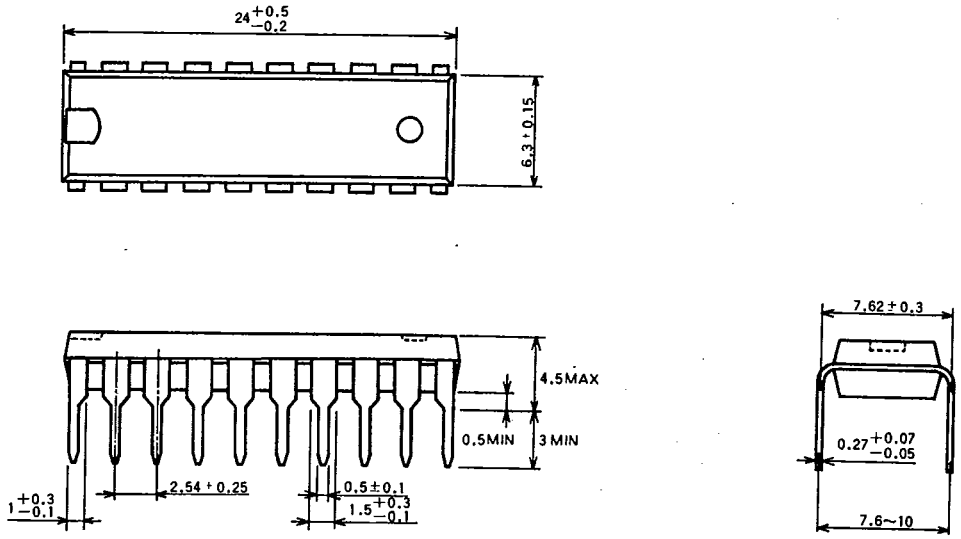


MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

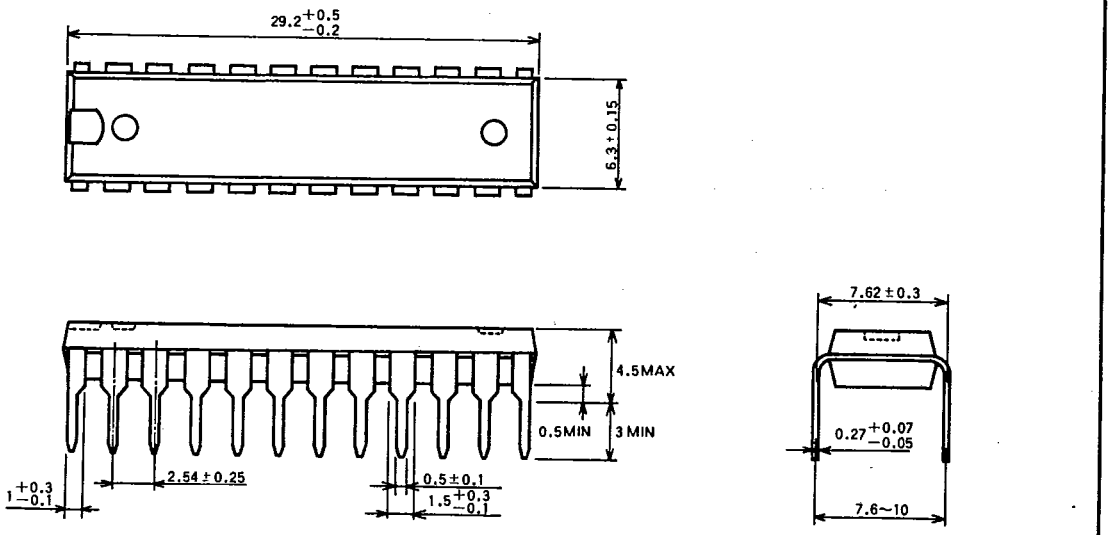
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



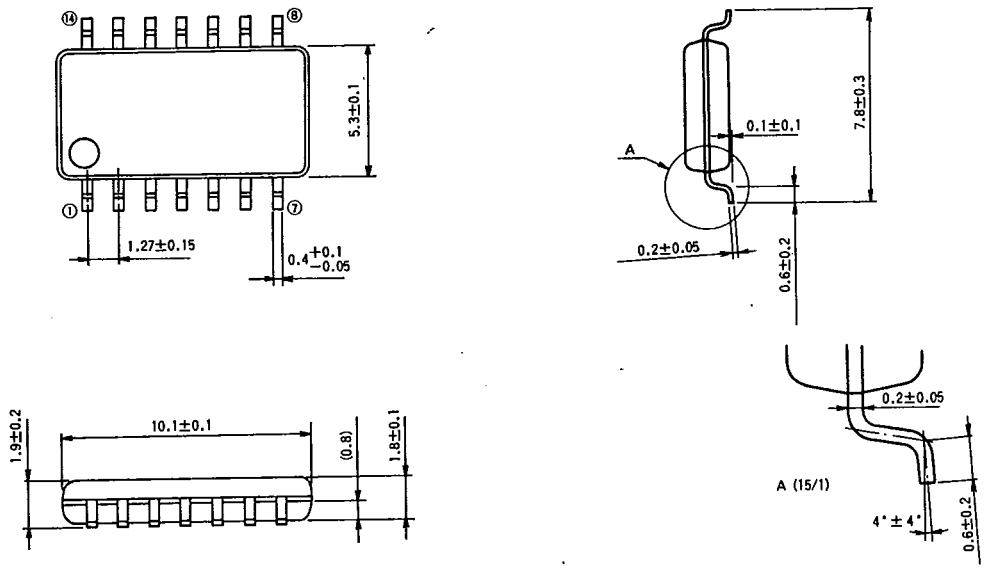
MITSUBISHI ELECTRIC

MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

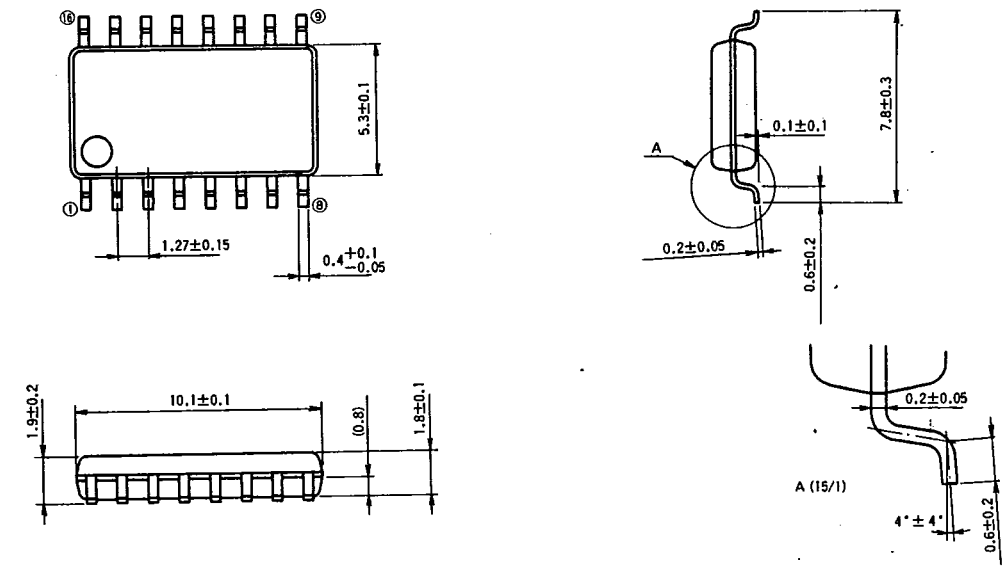
TYPE 14P2N 14PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 16P2N 16PIN MOLDED PLASTIC SOP

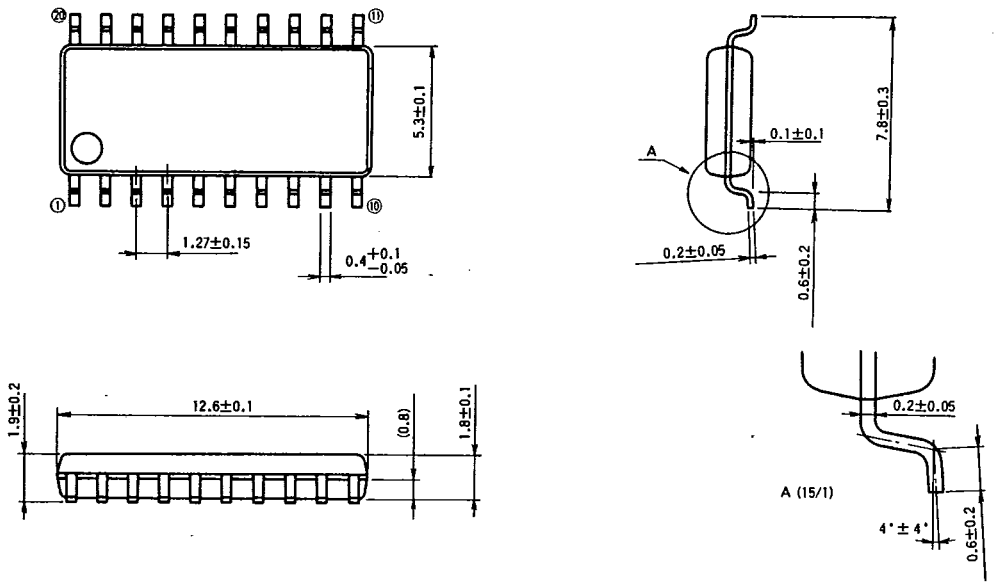
Dimension in mm



PACKAGE OUTLINES

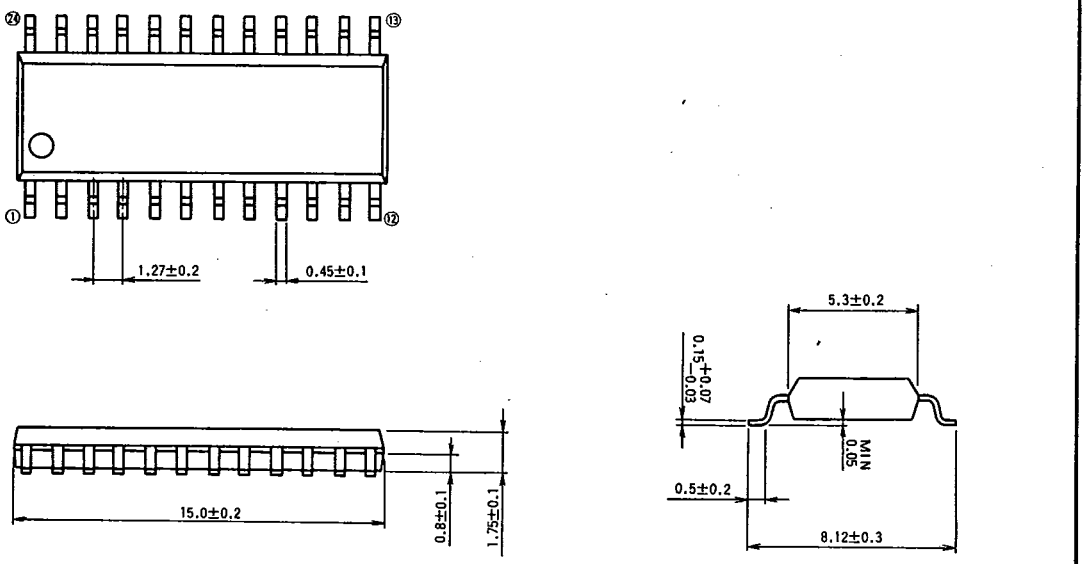
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

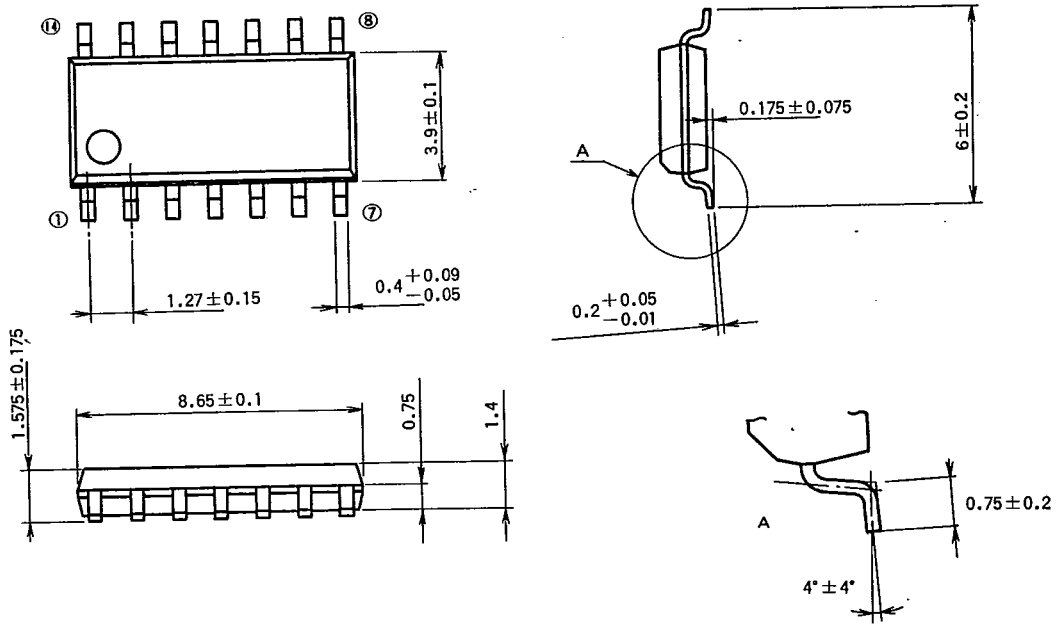


MITSUBISHI ELECTRIC

PACKAGE OUTLINES

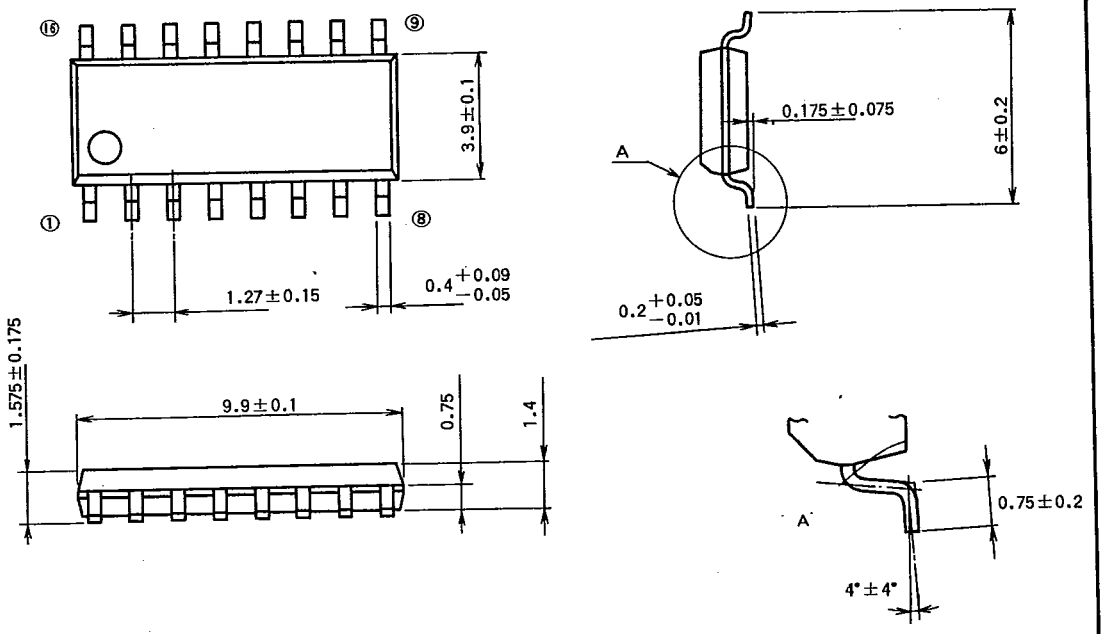
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm