5

ELECTRICAL SPECIFICATIONS

5.1 Operating Range

- Ambient Temperature, ...0°C - 70°C
- Voltages

  V_{dd}5V ± 10%
  V_{ss}0V

5.2 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{dd}	-0.5	+7.0	V
Input Voltage	V_i	-1.5	V_{dd}+1.5	V
Output Voltage	V_o	-0.5	V_{dd}+0.5	V
Output Current	I_o		± 25	mA
Power Dissipation	P_d		1200	mW
Operating Temperature	T_{opr}	0	+70	C
Storage Temperature	T_{stg}	-65	+150	C

5.3 AC Characteristics

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{dd}	4.5	5.5	V
Case Temperature	T_{case}	0	70	C
Max Low Level Output Voltage	V_{ol}		0.8	V
Min High Level Output Voltage	V_{oh}	2.2		V

5.4 DC Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{dd}	V_i=V_{dd} or V_{ss} XTAL at 30.3Mhz	TBD	TBD	mA
Input Voltage (CMOS input)	V_{ih} V_{il}		$0.7V_{dd}$	 $0.3V_{dd}$	V V
Input Voltage (TTL input)	V_{ih} V_{il}		2.0	 0.8	V V
CMOS Schmitt Trigger Input Voltage	V_{t+} V_{t-}	V_{dd}=4.5v-5.5v	2.0 1.5	3.4 2.6	V V
Hysteresis-Schmitt CMOS		V_{dd}=4.5v-5.5v	$0.11V_{dd}$	$0.18V_{dd}$	V
Input Leakage Current	I_{li}	V_i=V_{dd} or V_{ss}	-1.0	1.0	uA
Output Voltage (4mA output type)	V_{oh} V_{ol}	I_o=-4mA,V_{dd}=4.5v I_o=4mA,V_{dd}=4.5v	3.7	 0.4	V V
Output Voltage (8mA output type)	V_{oh} V_{ol}	I_o=-8mA,V_{dd}=4.5v I_o=8mA,V_{dd}=4.5v	3.7	 0.4	V V
Output Voltage (16mA output type)	V_{oh} V_{ol}	I_o=-16mA,V_{dd}=4.5v I_o=16mA,V_{dd}=4.5v	3.7	 0.4	V V
Output Leakage Current	I_{oz}		-5.0	5.0	uA
Input Capacitance	C_{in}	V_{dd}=V_i=0v		10	pF
Output Capacitance	C_{out}			12.5	pF

CMOS input: XTAL, XTAL1, XTAL2

CMOS Schmitt input: $\overline{\text{RSTIN}}$

TTL input: all inputs except XTAL, XTAL1, XTAL2, $\overline{\text{RSTIN}}$

4mA output: $\overline{\text{RSTOUT}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, $\overline{\text{INT}}$, MD0 - MD15, MA0 - MA9, $\overline{\text{WR}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{VSD}}$, TDO, $\overline{\text{AS}}$, A0 - A23, R/$\overline{\text{W}}$, $\overline{\text{UDS}}$, $\overline{\text{LDS}}$, $\overline{\text{DS}}$, SIZ0

8mA output: D0 - D15, R_YA_0-7, G_Y_0-7, B_YB_0-7, $\overline{\text{XT2}}$, $\overline{\text{CSROM}}$, $\overline{\text{DTACK}}$

16mA output: $\overline{\text{RAS}}$, $\overline{\text{UCAS1}}$, $\overline{\text{UCAS2}}$, $\overline{\text{LCAS1}}$, $\overline{\text{LCAS2}}$, XTALOUT

Signal Name	Capacitive Output Load	Resistive Output Load
$\overline{\text{DTACK}}$ $\overline{\text{INT}}$	130 pF	1000 ohms
D0 - D15 A0 - A23 $\overline{\text{AS}}$ R/$\overline{\text{W}}$ $\overline{\text{DS}}$ $\overline{\text{UDS}}$ $\overline{\text{LDS}}$ SIZ0 $\overline{\text{BERR}}$	130 pF	
$\overline{\text{HALT}}$ $\overline{\text{RSTOUT}}$	130pF	1000 ohms
TDO $\overline{\text{CSROM}}$ MD0 - MD15	50 pF	
MA0 - MA9 $\overline{\text{RAS}}$ $\overline{\text{U/LCAS1}}$ $\overline{\text{U/LCAS2}}$ XTALOUT	100 pF	
$\overline{\text{XT2}}$ $\overline{\text{HSYNC}}$ $\overline{\text{VSYNC}}$ $\overline{\text{WR}}$ R_YA_0 - 7 G_Y_0 - 7 B_YB_0 - 7 $\overline{\text{VSD}}$	ALL 75 pF	NIL

Ref.	Parameter	Symbol	Min	Max	Unit	Note
1	XTAL period		32		ns	
2	XTAL high time		13		ns	
3	XTAL low time		13		ns	
5	XTAL high to $\overline{XT2}$		0	25	ns	
11	$\overline{XT2}$ high to R0-R7,G0-G7,B0-B7, $\overline{VSYNC}$, $\overline{HSYNC}$ (RGB mode only)		5	27	ns	
11a	XTAL high to Y0-Y7, $\overline{VSYNC}$, $\overline{HSYNC}$. (CCIR-601 mode only)		5	25	ns	
13	$\overline{XT2}$ high to $\overline{VSD}$ (RGB mode only)		5	25	ns	
13a	XTAL high to $\overline{VSD}$ (CCIR-601 mode only)		5	25	ns	
14	$\overline{VSD}$ low to R0-R7,G0-G7,B0-B7 triple states		5	18	ns	
15	$\overline{VSD}$ high to R0-R7,G0-G7,B0-B7 active		5	18	ns	
16	Address to ($\overline{U/L}$)$\overline{DS}$ low (read)		0		ns	6,7
17	($\overline{U/L}$)$\overline{DS}$ high to Address invalid (read)		3		ns	6,7
18	($\overline{U/L}$)$\overline{DS}$ low to R/$\overline{W}$ high (read)			25	ns	6,7
18a	($\overline{U/L}$)$\overline{DS}$ low to $\overline{CS}$ low (read)			25	ns	6,7
19	($\overline{U/L}$)$\overline{DS}$ high to R/$\overline{W}$ hold (read)		-5		ns	6,7
19a	($\overline{U/L}$)$\overline{DS}$ high to $\overline{CS}$ high(read)		-20		ns	5
20	($\overline{U/L}$)$\overline{DS}$ low to $\overline{DTACK}$ (DRAM read)		235	320	ns	1,6,7
20a	($\overline{U/L}$)$\overline{DS}$ low to $\overline{DTACK}$ low (register read)		75	135	ns	1,6,7
21	($\overline{U/L}$)$\overline{DS}$ high to $\overline{DTACK}$ triple state(read)		5	43	ns	6,7
21a	$\overline{DTACK}$ active high time				ns	6,7
22	$\overline{DTACK}$ low to Data valid (read) DTACKSEL low			40	ns	3
22a	$\overline{DTACK}$ low to Data valid (read) DTACKSEL high			32	ns	3
23	($\overline{U/L}$)$\overline{DS}$ high to Data invalid (read)		5	25	ns	6,7
23a	($\overline{U/L}$)$\overline{DS}$ high to Data triple state (read)		5	40	ns	6,7
24	Address to ($\overline{U/L}$)$\overline{DS}$ low (write)		0		ns	6,7
25	($\overline{U/L}$)$\overline{DS}$ high to Address invalid (write)		0		ns	6,7
26	($\overline{U/L}$)$\overline{DS}$ low to R/$\overline{W}$ low (write)			25	ns	6,7
26a	($\overline{U/L}$)$\overline{DS}$ low to $\overline{CS}$ low (write)			25	ns	6,7
27	($\overline{U/L}$)$\overline{DS}$ high to R/$\overline{W}$ high (write)		-8		ns	5,6,7
27a	($\overline{U/L}$)$\overline{DS}$ high to $\overline{CS}$ high (write)		-20		ns	5
28	Data valid to ($\overline{U/L}$)$\overline{DS}$ low (write)		-8		ns	6,7
29	($\overline{U/L}$)$\overline{DS}$ high to Data invalid (write)		-8		ns	6,7
30	($\overline{U/L}$)$\overline{DS}$ low to $\overline{DTACK}$ low (DRAM write)		45	105	ns	1,6,7
30a	($\overline{U/L}$)$\overline{DS}$ low to $\overline{DTACK}$ low (register write)		75	135	ns	1,6,7

Ref.	Parameter	Symbol	Min	Max	Unit	Note
31	(U/L)DS high to DTACK high (write)		5	43	ns	6,7
32	(U/L)DS low to CSROM low			17	ns	
33	(U/L)DS high to CSROM high			13	ns	
34	(U/L)DS low to (DTACK for ROM) low		d+11	d+43	ns	2
35	(U/L)DS high to (DTACK high for ROM) high		0	50	ns	
36	RAS high pulse duration	tRP	65		ns	
37	RAS low pulse duration	tRAS	90		ns	
38	U/LCAS high pulse duration	tCP	20		ns	
39	U/LCAS low pulse duration	tCAS	30		ns	
40	U/LCAS high to RAS low delay	tCRP	50		ns	
41	RAS low to U/LCAS low delay	tRCD	60		ns	
42	U/LCAS low to RAS high delay	tRSH	25		ns	
43	RAS low to U/LCAS high delay	tCSH	95		ns	
44	RAS low to column address delay	tRAD	30		ns	
45	Row address set-up time	tASR	15		ns	
46	Row address hold time	tRAH	30		ns	
47	Column address set-up time	tASC	20		ns	
48	Column address hold time	tCAH	25		ns	
49	Data set-up time to U/LCAS low	tDS	100		ns	
50	Data hold time to U/LCAS low	tDH	40		ns	
51	Read set-up time to U/LCAS low	tRCS	75		ns	
52	Read hold time to U/LCAS high	tRCH	35		ns	
53	Write set-up time to U/LCAS low	tWCS	70		ns	
54	Write hold time to U/LCAS low	tWCH	75		ns	
55	RAS low to data valid	tRAC		90	ns	
56	U/LCAS low to data valid	tCAC		21	ns	
57	Column address to data valid	tAA		45	ns	
58	U/LCAS high to data invalid	tOFF	0		ns	
59	Refresh period 1Mx4	tRFSH	9		ms	
60	Refresh period 256Kx4 and 256Kx16	tRFSH	5		ms	
61	RSTIN low to RSTOUT/HALT low		75	140	ns	4
62	RSTIN low time		2		us	
63	RSTIN high to RSTOUT high		150	160	ms	
64	RSTOUT high to HALT high		59	64	us	
65	HSYNC/VSYNC low to XTAL high setup (CCIR-601 mode only)		10		ns	

Ref.	Parameter	Symbol	Min	Max	Unit	Note
65a	$\overline{HSYNC}/\overline{VSYNC}$ low to $\overline{XT2}$ high setup (RGB mode only)		10		ns	
66	$\overline{HSYNC}/\overline{VSYNC}$ low after XTAL high hold (C_bYC_rY mode only)		0		ns	
66a	$\overline{HSYNC}/\overline{VSYNC}$ low after XTAL high hold (RGB mode only)		0		ns	
67	$(U/L)\overline{DS}$ high to $\overline{BERR}$ high					
68	DTACKSEL to $\overline{DTACK}$ delay active					
69	$\overline{DTACK}$ low to DATA invalid (write)					
72	$\overline{XT2}$ high time				ns	
73	$\overline{XT2}$ low time				ns	
74	R_YA_(7:0)/R_YB_(7:0) to XTAL high setup (C_bYC_rY mode only)		10		ns	
75	R_YA_(7:0)/R_YB_(7:0) to XTAL high hold (C_bYC_rY mode only)		0		ns	

Notes:

1. These figures are valid for free-run. If video is enabled the maximum delay increases with a maximum of 16 XTAL periods.

2. The delay depends on the XTAL frequency and the programmed value DD, DD1, DD2. In total the delay becomes:

DD	DD1	DD2	XTAL=27MHz		XTAL=28MHz		XTAL=30MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
0	x	x	TBD	TBD	400	470	375	445	ns
1	0	0	TBD	TBD	115	185	110	175	ns
1	0	1	TBD	TBD	185	260	175	240	ns
1	1	0	TBD	TBD	260	330	240	310	ns
1	1	1	TBD	TBD	330	400	310	375	ns

3. This timing is switchable using PIN 99, and is valid for Video Channel and DRAM accesses:
   - PIN 99 = LOW level: 40ns (max) advance (68000/070/340/341-16)
   - PIN 99 = HIGH level: 32ns (max) advance (68340/341-25)
   Timing of DTACK for ROM accesses is unchanged.

4. Timing is 2-3 clock cycles + time specified in table.

5. Calculations based upon estimated 68341 timing values. To be confirmed.

6. For a description of 68000 and 68300 bus protocols see 'Bus Operation' section of 68000 and 68300 user manuals.

7. The MCD214 is specified to be compliant with 68000 and 68300 bus protocols at crystal frequencies of 10 to 16.78Mhz and 25.16MHz.

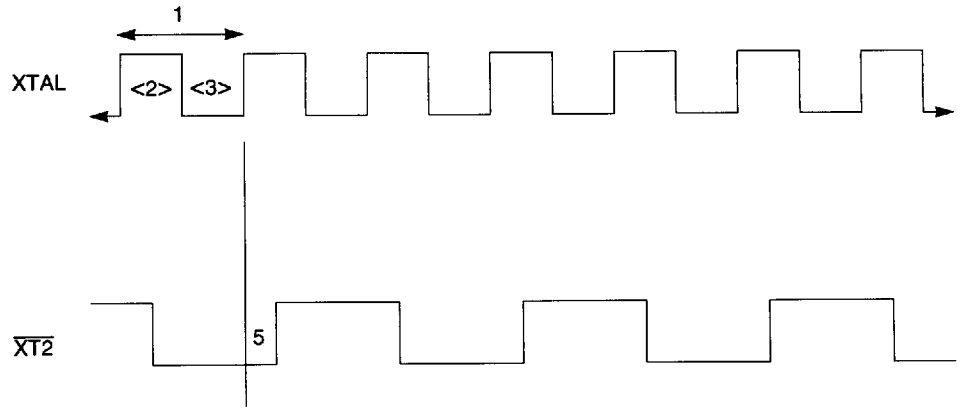


Figure 31 Clock Timing

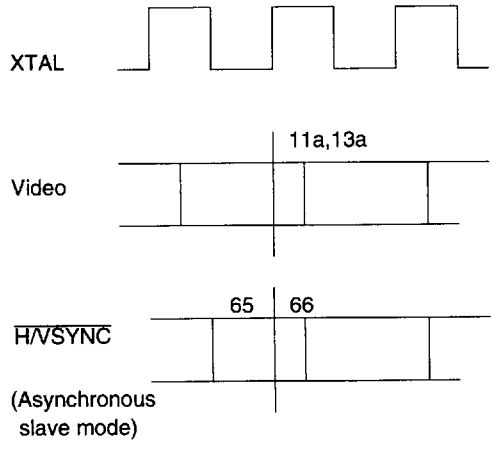
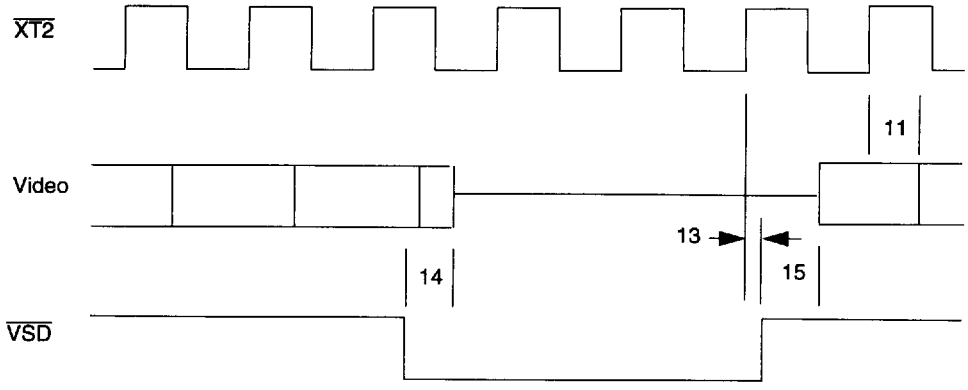


Figure 32 Video Timing - C_bYC_rY Mode



Video : R_YA_(7:0), G_Y_(7:0), B_YB_(7:0), VSYNC, HSYNC

Figure 33 Video Timing - RGB Mode

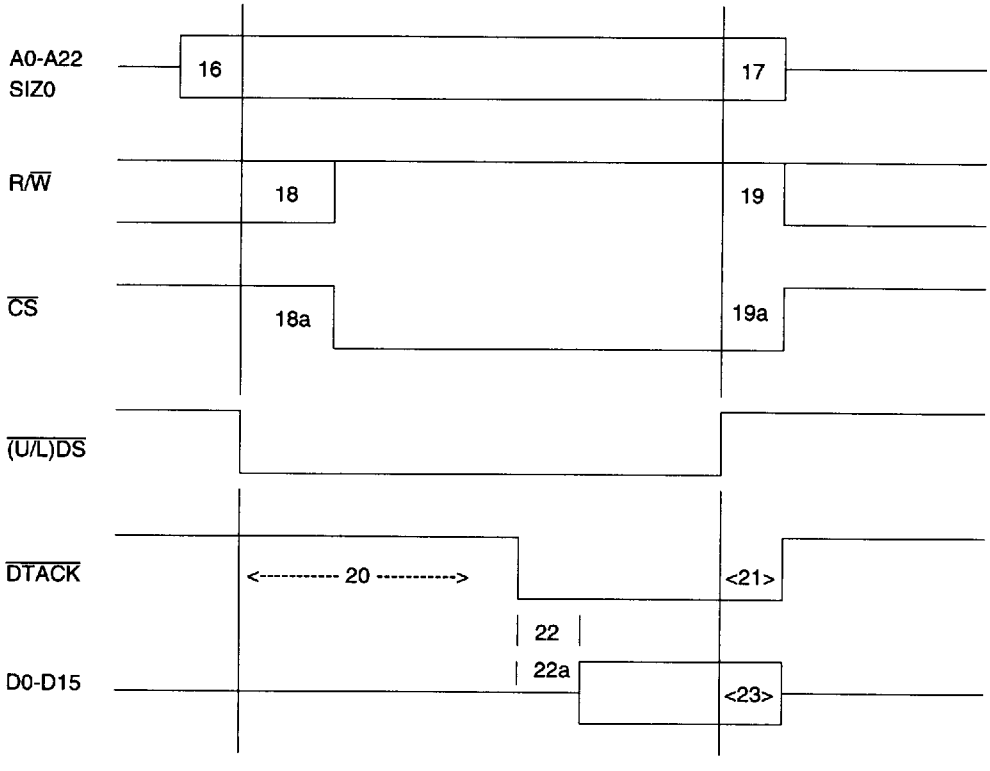


Figure 34 CPU Read Cycle Timing

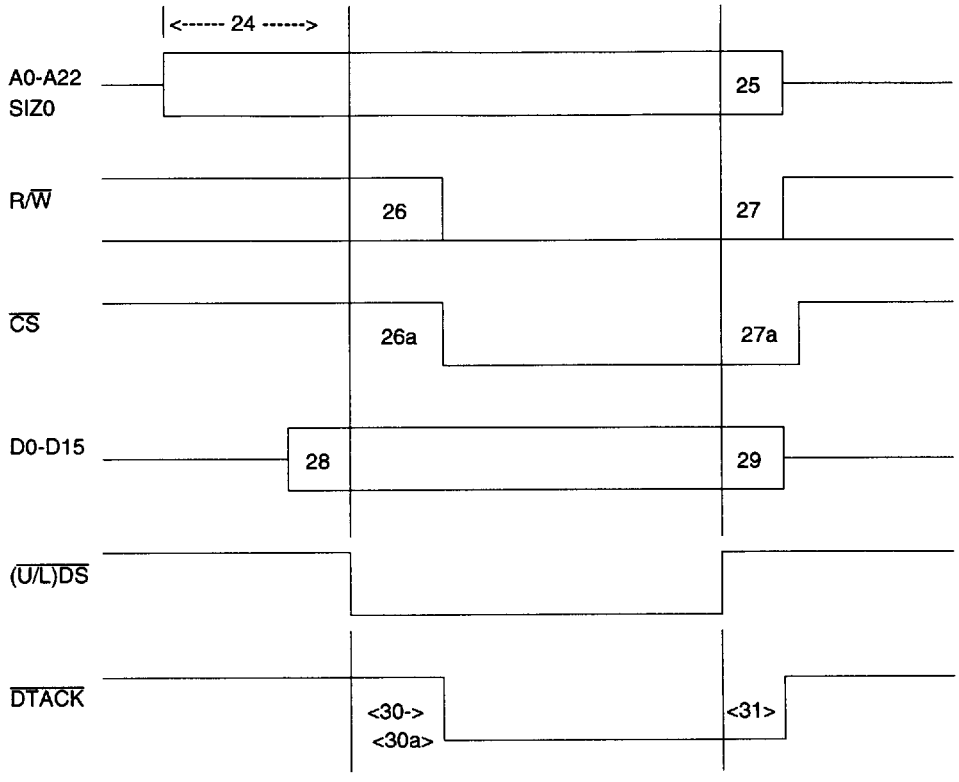


Figure 35 CPU Write Cycle Timing

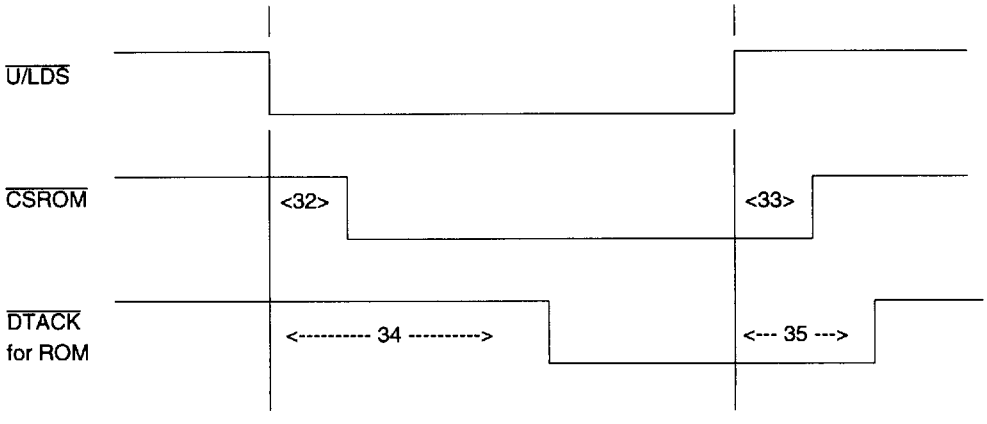


Figure 36 System Timing

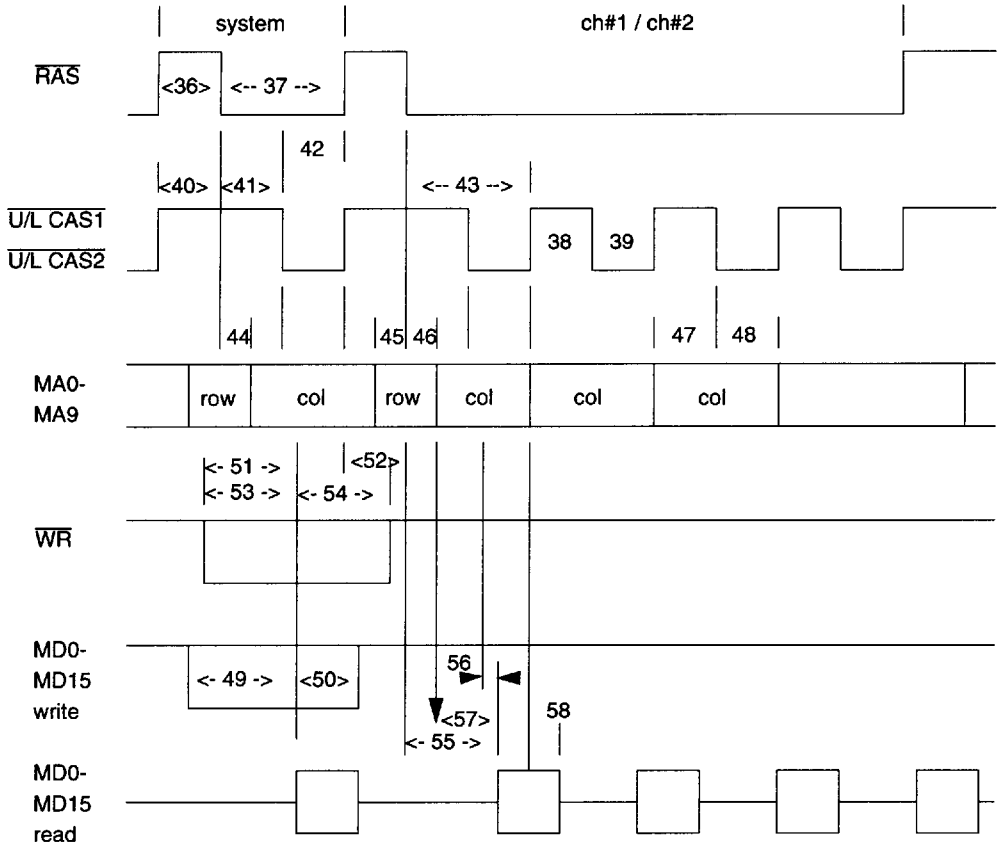


Figure 37 DRAM Timing

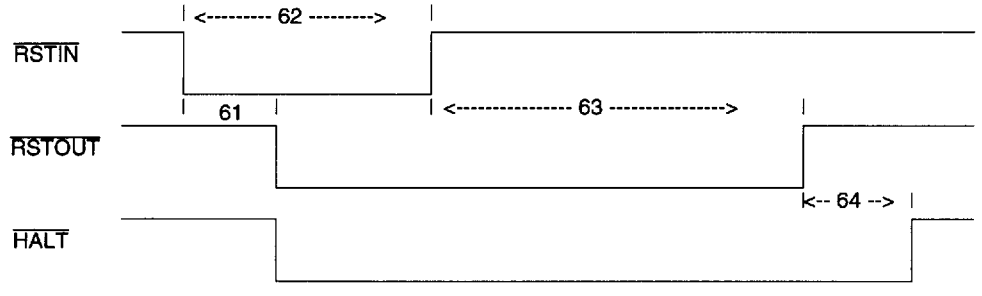


Figure 38 Reset and Halt Timing

6

MECHANICAL DATA

6.1 Pin Reference

No.	Name	No.	Name	No.	Name	No.	Name
1	VSS	41	VDD	81	MD10	121	$\overline{\text{VSYNC}}$
2	$\overline{\text{RSTOUT}}$	42	A22	82	MA3	122	$\overline{\text{HSYNC}}$
3	VDD	43	A21	83	MA2	123	VDD
4	$\overline{\text{CS}}$	44	A20	84	MA1	124	VDD
5	SEN	45	A19	85	$\overline{\text{AS}}$	125	BYB0
6	$\overline{\text{RSTIN}}$	46	A18	86	MA0	126	BYB1
7	$\overline{\text{HALT}}$	47	A17	87	$\overline{\text{WR}}$	127	BYB2
8	$\overline{\text{INT}}$	48	A16	88	$\overline{\text{LCAS1}}$	128	VSS
9	VDD	49	A15	89	$\overline{\text{LCAS2}}$	129	BYB3
10	$\overline{\text{CSROM}}$	50	A14	90	MD9	130	VDD
11	TDO	51	VSS	91	MD8	131	BYB4
12	TDI	52	A13	92	MD7	132	BYB5
13	$\overline{\text{DS}}$	53	A12	93	MD6	133	BYB6
14	$\overline{\text{BERR}}$	54	A11	94	MD5	134	BYB7
15	D0	55	A10	95	VDD	135	GY0
16	D1	56	A9	96	VSS	136	VSS
17	VSS	57	A8	97	MD4	137	GY1
18	D2	58	A7	98	MD3	138	GY2
19	D3	59	A6	99	DTACKSEL	139	VSS
20	D4	60	A5	100	VDD	140	VDD
21	D5	61	VDD	101	MD2	141	GY3
22	D6	62	A4	102	MD1	142	GY4
23	D7	63	A3	103	MD0	143	GY5
24	VSS	64	A2	104	VSS	144	GY6
25	D8	65	A1	105	$\overline{\text{RAS}}$	145	TMS
26	D9	66	VSS	106	M/$\overline{\text{S}}$	146	GY7
27	VDD	67	A23	107	$\overline{\text{UCAS1}}$	147	RYA0
28	D10	68	MA9	108	VSS	148	VDD
29	D11	69	MA8	109	$\overline{\text{UCAS2}}$	149	RYA1
30	D12	70	MA7	110	TST	150	RYA2
31	D13	71	MA6	111	VSS	151	RYA3
32	RGB	72	MA5	112	VDD	152	RYA4
33	D14	73	MA4	113	TCK	153	VSS
34	D15	74	MD15	114	VSS	154	RYA5
35	$\overline{\text{DTACK}}$	75	MD14	115	XTAL	155	RYA6
36	VDD	76	MD13	116	VDD	156	VSS
37	$\overline{\text{RW}}$	77	VSS	117	$\overline{\text{XT2}}$	157	RYA7
38	$\overline{\text{LDS}}$	78	MD12	118	XTALOUT	158	$\overline{\text{VSD}}$
39	$\overline{\text{UDS}}$	79	MD11	119	XTAL2	159	A0
40	VSS	80	VDD	120	XTAL1	160	SIZ0

6.2 Packaging

The MCD214 is packaged in a 160 pin plastic Quad Flat Pack (QFP).

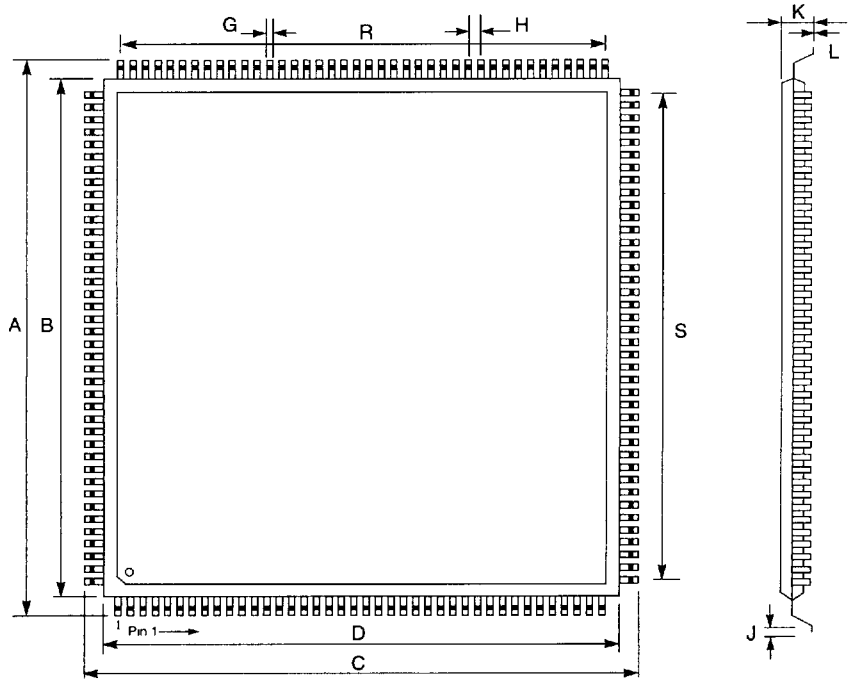


Figure 39 Packaging

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	31.00	31.40	1.220	1.236
B	27.90	28.10	1.098	1.106
C	31.00	31.40	1.220	1.236
D	27.90	28.10	1.098	1.106
G	0.28	0.38	0.011	0.015
H	0.650 typically		0.0256 typically	
J	0.75	0.92	0.030	0.036
K	3.45	3.85	0.136	0.152
L	0.13	0.18	0.005	0.007
R	25.35 Ref.		0.998 Ref.	
S	25.35 Ref.		0.998 Ref.	