



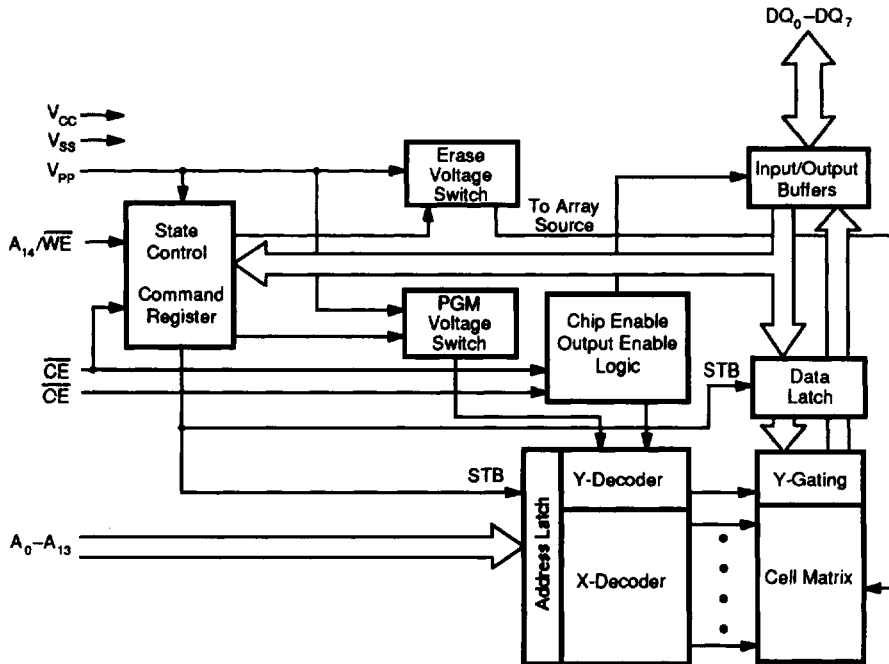
# Am27F256

32,768 x 8-Bit CMOS Windowless EPROM

## DISTINCTIVE CHARACTERISTICS

- **Flasherase™ Electrical Bulk Chip-Erase**
  - One Second Typical Chip-Erase
- **Compatible with JEDEC Standard Byte Wide EPROM pinouts**
  - 28-pin DIP
  - 32-pin PLCC
- **Flashrite™ Programming**
  - 10μS Typical Byte-Program
  - Less than 0.5 Second Typical Chip Program
- **Advanced CMOS Technology**
  - EPROM Compatible Process
  - Extensive Manufacturing Experience
- **Low Power Consumption**
  - 30mA Maximum Active Current
  - 100 μA Maximum Standby Current
- **Command Register Architecture for Microprocessor/Micro-controller Compatible Write Interface**
- **100 Program/Erase Cycles**
- **Program and Erase Voltage**  
+12.75V ± 0.25V V<sub>PP</sub>
- **High Performance**
  - 90ns Maximum Access Time
- **Allows for Auto-Insertion**
- **5V±10% Single Power Supply**

## BLOCK DIAGRAM



11557-001A

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The document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication #	Rev.	Amendment
11557	A	/0
Issue Date: February, 1989		

## GENERAL DESCRIPTION

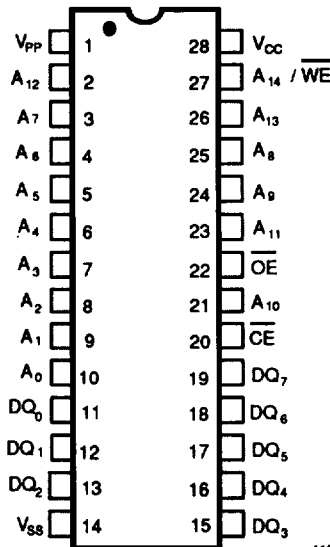
This device is an alternative to the standard U.V. EPROM.

The Am27F256 CMOS windowless EPROM provides the industry's highest performance and most cost-effective alternative for reprogrammable non-volatile memory. It is organized as 32K bytes of 8 bits each. The Am27F256 is pin compatible with the 28 pin byte-wide JEDEC 256K EPROM. The 27F256 is targeted for alterable code- or data-storage applications where ultraviolet erasure is impractical or time consuming. The window-

less EPROM adds electrical Flash chip-erase and reprogrammability in plastic packaging to AMD's EPROM technology. The device may be packaged in plastic DIP or PLCC and is ideal for use in auto-insertion manufacturing systems. The entire memory content may be erased and reprogrammed using AMD's Flasherase™ and Flashrite™ programming algorithms respectively in a standard PROM programmer. Electrical erasure increases the memory's flexibility, while providing time savings over traditional UV erasing.

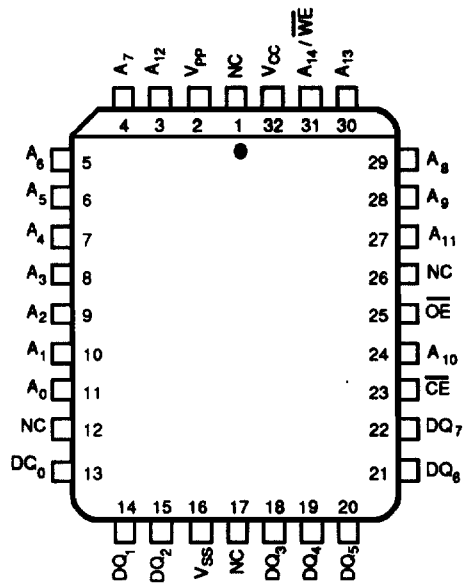
## CONNECTION DIAGRAMS

DIP



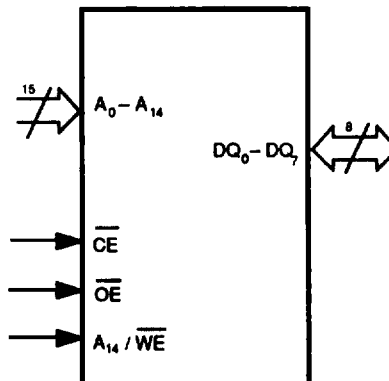
11557-002A

LCC/PLCC



11157-003A

## LOGIC SYMBOL



11557-004A

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## FUNCTIONAL DESCRIPTION

In-circuit electrical erase and reprogramming increases flash memory's flexibility over EPROM. Standard PROM programmers may be used for erasing and programming. A command register in the windowless EPROM manages these functions. The command register allows for fixed power supplies during the erase and programming functions, does not require high voltage on control pins, and provides maximum EPROM compatibility.

### Read Mode

The windowless EPROM device functions as a read only memory when high voltage is not applied to the  $V_{pp}$  pin. In this mode the external memory control signals produce the standard EPROM read, standby, output disable, and Auto-select modes.

### Programming/Read Mode

High voltage on the  $V_{pp}$  pin enables the erase and programming functions of the device. The same EPROM read, standby, and output disable functions are available to the system when high voltage is applied to the  $V_{pp}$  pin. All functions associated with altering memory

contents: erase, erase-verify, program, and program-verify—are accessed via the command register.

Standard microprocessor write timing is used to write commands into the register. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for programming or erase operations. Standard microprocessor read timings are used to access array data, access data for erase and program verification, or access the Auto-select modes.

The command register is alterable only when high voltage is applied to  $V_{pp}$ . When high voltage is removed, the contents of the register default to the read command. The device then functions as a read only memory.

### Performance

AMD's windowless EPROMs offer access times as fast as 90ns which allows operation of high-speed microprocessors and microcontrollers without wait-states. The windowless EPROM architecture supports separate chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) controls in order to eliminate bus contention.

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## OPERATING RANGES

### Commercial (C) Devices

Case Temperature ( $T_c$ ) 0°C to +70°C

### Industrial (I) Devices

Case Temperature ( $T_c$ ) -40°C to +85°C

### Extended (E) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

### Military (M) Devices

Case Temperature ( $T_c$ ) -55°C to +125°C

*Operating ranges define those limits between which the functionality of the device is guaranteed.*