OKI semiconductor
MSM514251RS/ZS

262, 144 words X 4 bits Multi-port DRAM

<Static Column Mode>

DESCRIPTION

The OKI MSM514251 is a high speed 1M bits Multi-port Dynamic Randam Access Memory designed especially for high performance graphics applications. The multiport DRAM consists of a 256K x 4 bits DRAM port with multiplexed address and a 512 x 4 bits serial Read/Write port.

The multi-port DRAM uses OKI's N-well CMOS process combined with silicide technology and a single transister dynamic storage cell. The technology provides wide operating margins as well as high density and low power dissipation.

In addition to the conventional 1 megabit random access port which has static column operation mode, the multi-port DRAM has a second fast serial access read/write port with a clock rate of 33MHz for driving a video-type display.

The multiport DRAM has an internal 512 X 4 bits shift register which can be parallel loaded with an entire row of data from sense amps in a special cycle which is referred to as the Read Data Transfer Cycle. Data is shifted out via the serial port for screen refresh, independent of the random access port. The shift register is also used to write 512 X 4 bits of data to connected sense amps in a special cycle which is referred to as the Write Transfer Cycle. Serial read and random read/write operations can occur simultaneously except when the serial shift register load operation must be synchronized with any random access port operations. Serial write and random read/write operations can occur except in a Write Data Transfer cycle.

The 512 X 4 bits shift register can supply a constant 33 MHz, four-bit wide data stream. The shift register requires no refresh operation because it uses static CMOS flip-flops.

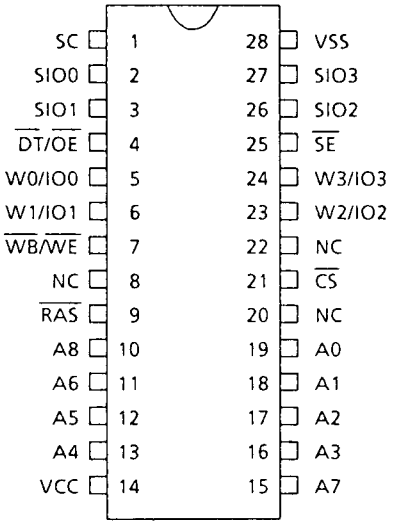
FEATURES

- Dual Port
  - RAM port : 256K words X 4 bits
  - SAM port : 512 words X 4 bits
- Fast Access
  - RAM port :Cycle time 190 ns (MIN)
    :Access time 100 ns (MAX)
  - SAM port :Cycle time 30 ns (MIN)
    :Access time 30 ns (MAX)
- Asynchronous Operation (Except during data transfer period)
- Bidirectional Data Transfer
  - Read Data Transfer:
    From RAM array to data register
  - Write Data Transfer:
    From data register to RAM array
  - Pseudo Write Data Transfer:
    No data transfer from data register to RAM array
- Pointer Control
  - Addressable serial read/write start bit

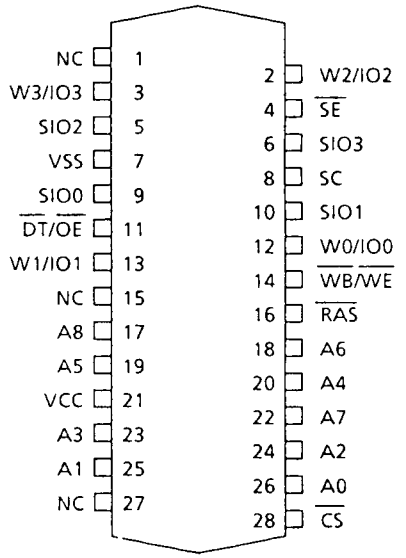
FEATURES (Continued)

- Write Per Bit
  - Write mask to any combination of the 4 bits on the random access pins
- Continuous Serial Read
  - Real time data transfer from the RAM array to the data register
- Static Column Mode
  - Static Column Cycle : 55 ns (MIN)
  - Address Access Time: 50 ns (MAX)
- Refresh Capabilities
  - RAS Only Refresh Mode: 512 cycle/8 ms
  - Hidden Refresh Mode
  - CS before RAS Refresh Mode
- Full TTL Compatibility
- Single Power supply
  - 5V ± 10%
- JEDEC Pinout
  400 mil 28 pin DIP
  400 mil 28 pin ZIP

PIN OUT



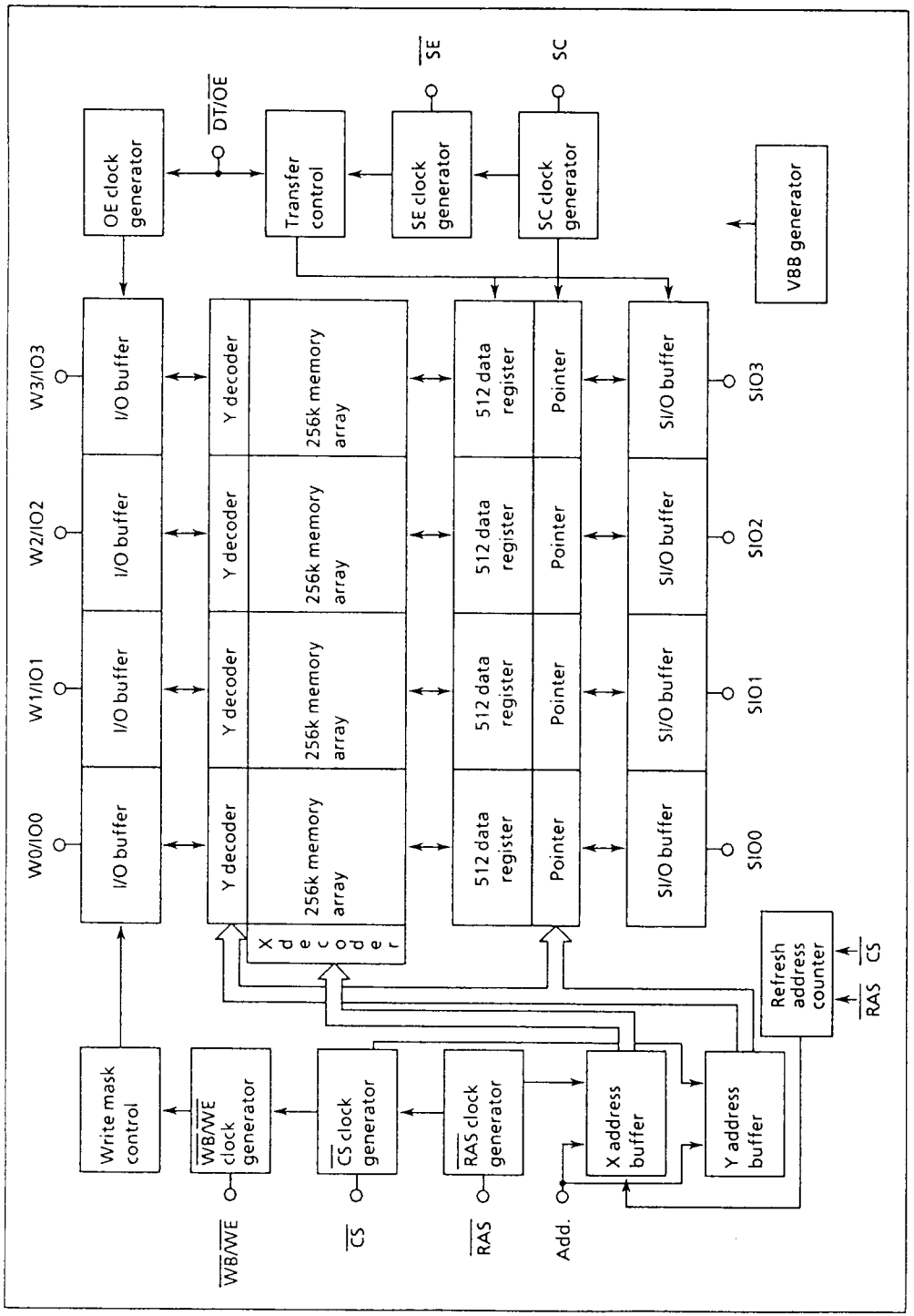
28 PIN DIP



28 PIN ZIP

SC	=	SERIAL CLOCK	RAS	=	ROW ADDRESS STROBE
SIO0-3	=	SERIAL DATA IN, DATA OUT	A0-8	=	ADDRESS INPUT
DT/OE	=	DATA TRANSFER ENABLE, DRAM OUTPUT ENABLE	VCC	=	POWER (+ 5V)
IO0-3	=	DRAM DATA IN, DATA OUT	VSS	=	GROUND
WB/WE	=	WRITE PER BIT/WRITE ENABLE	SE	=	SERIAL ENABLE
NC	=	NO CONNECTION	CS	=	COLUMN ADDRESS STROBE, CHIP SELECT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply Voltage		-1~7	V
Vi	Input Voltage	With respect to Vss	-1~7	V
Vo	Output Voltage		-1~7	V
Io	Output Current		50	mA
Pd	Power dissipation	Ta = 25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-55~150	°C

CAPACITANCE (Ta = 25°C, f = 1MHz, Vi = 25mVrms)

Symbol	Parameter	Min	Max	Unit
C_{IN1}	$\overline{RAS}$, $\overline{CS}$, $\overline{WB/WE}$, SC, $\overline{SE}$, $\overline{DT/OE}$		8	pF
C_{IN2}	A0-A7		5	pF
C_{IO1}	I/O0-3, SIO0-3		7	pF

RECOMMENDED OPERATING CONDITIONS

(Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
Vcc	Supply Voltage	4.5	5	5.5	V
Vss	Supply Voltage	0	0	0	V
V_{IH}	High-level Input voltage, all inputs	2.4		Vcc + 1	V
V_{IL}	Low-level Input voltage, all inputs	-1		0.8	V

*All input voltages are with respect to Vss

DC CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH} = -2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2mA	0		0.4	V
I_{LO}	Off-state output current	Output nonactive, 0V ≦ Vout ≦ 5.5V	-10		10	uA
I_{LI}	Input current	0V ≦ Vin ≦ Vcc, Other input pins = 0V	-10		10	uA

* Current flowing into an IC is positive, out is negative

DC CHARACTERISTICS (Cont'd)

Symbol	Parameter		MSM514251		Unit
			-10	-12	
	RAM port	Serial I/O port	Max	Max	
Icc1(AV)	Random R/W cycle ($\overline{RAS}$, $\overline{CS}$ Address cycling, tRC = tRC (min))	Standby (SC = V_{IL})	70	60	mA
Icc2**	Standby ($\overline{RAS}$ = $\overline{CS}$ = V_{IH}, Dout = HZ)	Standby (SC = V_{IL})	5	5	mA
Icc3(AV)	$\overline{RAS}$ only refresh cycling ($\overline{CS}$ = V_{IH}, tRC = tRC (min))	Standby (SC = V_{IL})	60	50	mA
Icc4(AV)	Static column mode cycle, ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, tSC = tSC(min) Address cycling	Standby (SC = V_{IL})	45	35	mA
Icc5(AV)	$\overline{CS}$ before $\overline{RAS}$ refresh $\overline{RAS}$/$\overline{CS}$ Cycling, (tRC = tRC(min))	Standby (SC = V_{IL})	65	55	mA
Icc6(AV)	Data transfer cycle, ($\overline{DT}$/$\overline{OE}$, $\overline{CS}$ $\overline{RAS}$ cycling, (tRC = tRC(min))	Standby (SC = V_{IL})	75	65	mA
Icc7(AV)	Random R/W cycle ($\overline{RAS}$, $\overline{CS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	120	100	mA
Icc8(AV)	Standby ($\overline{RAS}$ = V_{IH}, Dout = HZ)	Active (tSCC = tSCC(min))	50	40	mA
Icc9(AV)	$\overline{RAS}$ only refresh cycle, ($\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH}, tRC = tRC(min))	Active (tSCC = tSCC(min))	110	90	mA
Icc10(AV)	Static column mode cycle (RAS = V_{IL}, Address cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	100	80	mA
Icc11(AV)	$\overline{CS}$ before $\overline{RAS}$ refresh ($\overline{RAS}$, $\overline{CS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	110	90	mA
Icc12(AV)	Data transfer cycle $\overline{DT}$/$\overline{OE}$, RAS, $\overline{CS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	125	105	mA

* Icc (AV) is obtained with the output open. (AV) specifies average value.
** If $V_{IH} \geqq$ VccX0.9 and $V_{IL} \leqq$ 0.6V, then Icc2 $\leqq$ 1.5mA.

TIMING REQUIREMENTS-Dynamic Access Array (Vcc = 5V ± 10%, Ta = 0-70°C)

Symbol		MSM514251				Unit	Note
		-10		-12			
		MIN.	MAX.	MIN.	MAX.		
tRC	Random read or write cycle time	190	-	220	-	ns	
tRMW	Read/write cycle time	255	-	295	-	ns	
tSC	Static column mode cycle time	55	-	65	-	ns	
tSRMW	Static column mode read/write cycle time	115	-	135	-	ns	
tRAC	Access time from $\overline{RAS}$	-	100	-	120	ns	2, 7
tCAC	Access time from $\overline{CS}$	-	35	-	45	ns	2, 7
tAA	Access time from column address	-	50	-	60	ns	2, 8
tALW	Access time from last write	-	95	-	115	ns	2, 9
tCLZ	Output low impedance time from $\overline{CS}$	5	-	5	-	ns	2
tOFF	Output buffer turn-off delay	0	30	0	35	ns	3
tAOH	Data output hold time reference to column address	5	-	5	-	ns	
tOW	Data output enable time reference to $\overline{WE}$	-	30	-	35	ns	
tT	Transition time	3	50	3	50	ns	1
tRP	$\overline{RAS}$ precharge time	80	-	90	-	ns	
tRAS	$\overline{RAS}$ pulse width	100	10,000	120	10,000	ns	
tRSH	$\overline{RAS}$ hold time	35	-	45	-	ns	
tCSH	$\overline{CS}$ hold time	100	-	120	-	ns	
tCS	$\overline{CS}$ pulse width	35	10,000	45	10,000	ns	
tRCD	$\overline{RAS}$ to $\overline{CS}$ delay time	25	65	25	75	ns	7
tRAD	$\overline{RAS}$ to column address delay time	20	50	20	60	ns	
tCRP	$\overline{CS}$ to $\overline{RAS}$ precharge time	10	-	10	-	ns	
tCPN	$\overline{CS}$ precharge time	15	-	20	-	ns	
tCP	$\overline{CS}$ precharge time (Static column mode)	10	-	15	-	ns	
tASR	Row address set-up time	0	-	0	-	ns	
tRAH	Row address hold time	15	-	15	-	ns	
tASC	Column address set-up time	0	-	0	-	ns	
tCAH	Column address hold time	20	-	25	-	ns	
tRAL	Column address to $\overline{RAS}$ lead time	55	-	60	-	ns	
tRRH	Read command hold time reference to $\overline{RAS}$	0	-	0	-	ns	4
tWH	Write command hold time (Dout disable)	0	-	0	-	ns	6
tWCR	Write command hold time from $\overline{RAS}$	75	-	90	-	ns	
tWP	Write command pulse width	20	-	25	-	ns	

TIMING REQUIREMENTS-Dynamic Access Array (Vcc = 5V ± 10%, Ta = 0-70°C)

Symbol		MSM514251				Unit	Note
		-10		-12			
		MIN.	MAX.	MIN.	MAX.		
tRWL	Write command to $\overline{RAS}$ lead time	25	-	30	-	ns	
tCWL	Write command to $\overline{CS}$ lead time	25	-	30	-	ns	
tDS	Data-in set-up time	0	-	0	-	ns	5
tDH	Data-in hold time	20	-	25	-	ns	5
tREF	Refresh period	-	8	-	8	ns	
tWCS	Write command set-up time	0	-	0	-	ns	6
tCWD	$\overline{CS}$ to $\overline{WE}$ delay	75	-	85	-	ns	6
tAWD	Column address to $\overline{WE}$ delay time	85	-	100	-	ns	6
tCSR	$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before RAS)	10	-	10	-	ns	
tCHR	$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before RAS)	30	-	30	-	ns	
tRPC	$\overline{CS}$ active delay from $\overline{RAS}$ precharge	0	-	0	-	ns	
tOEA	Access time from $\overline{OE}$	-	35	-	45	ns	
tOED	$\overline{OE}$ delay time	25	-	30	-	ns	
tOEZ	$\overline{OE}$ to data output buffer turn-off delay	0	25	0	30	ns	3
tAH	Column address hold time reference to RAS precharge	-	10		15	ns	9
tLWAD	Last write to column address delay	25	45	30	45	ns	
tAHLW	Column address hold time reference to $\overline{WE}$	-	95	-	115	ns	
tRCS	Read command set-up time	0	-	0	-	ns	
tRCH	Read command hold time	0	-	0	-	ns	
tWI	Write invalid time	10	-	15	-	ns	
tOEH	$\overline{OE}$ command hold time	25	-	30	-	ns	

TIMING REQUIREMENTS-Serial Access Array (Vcc = 5V ± 10%, Ta = 0-70°C)

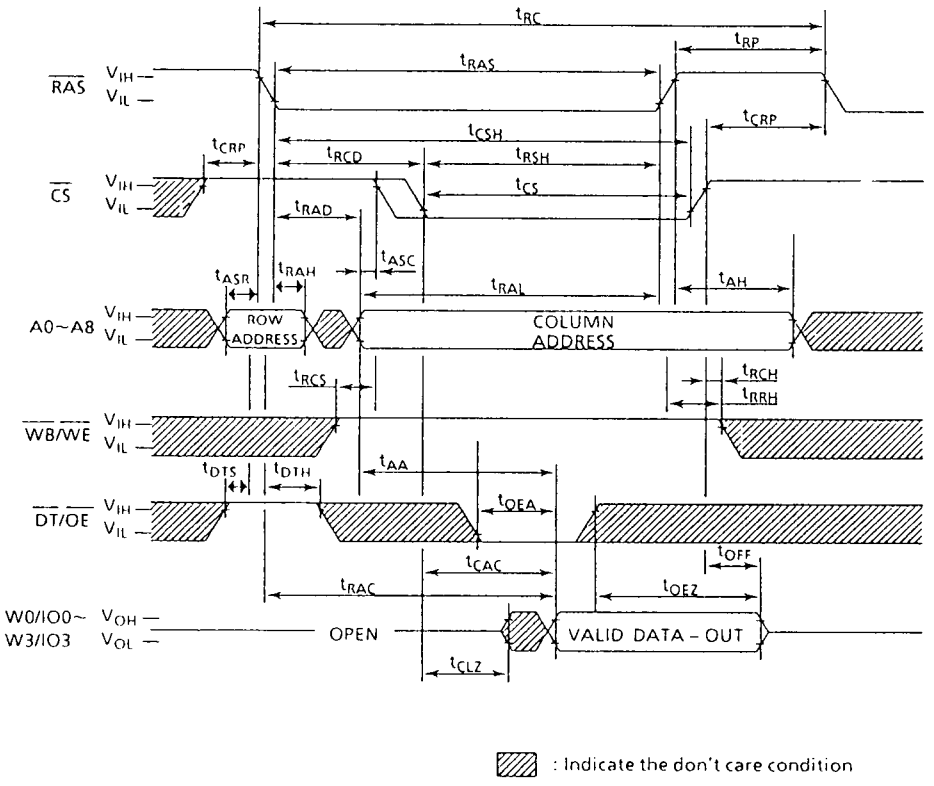
Symbol		MSM514251				Unit	Note
		-10		-12			
		MIN.	MAX.	MIN.	MAX.		
tSCC	Serial clock cycle time	30	-	40	-	ns	
tSCA	Access time from SC	-	30	-	40	ns	10
tSEA	Access time from $\overline{SE}$	-	30	-	40	ns	10
tSP	SC pulse width	10	-	10	-	ns	
tSCP	SC precharge time	10	-	10	-	ns	
tSOH	Serial data-out hold time	10	-	10	-	ns	
tSEZ	$\overline{SE}$ to serial output buffer turn-off delay	0	25	0	25	ns	
tSIS	Serial data-in set-up time	0	-	0	-	ns	
tSIH	Serial data-in hold time	15	-	20	-	ns	
tDTS	$\overline{RAS}$ to $\overline{DT}$ set-up time	0	-	0	-	ns	
tRDH	$\overline{RAS}$ to $\overline{DT}$ hold time (Read transfer cycle)	80	-	100	-	ns	11
tDTH	$\overline{RAS}$ to $\overline{DT}$ hold time	15	-	15	-	ns	
tCDH	$\overline{CAS}$ to $\overline{DT}$ hold time	30	-	40	-	ns	11
tSDD	SC to $\overline{DT}$ delay time	10	-	10	-	ns	
tSDH	$\overline{DT}$ to SC hold time	10	-	10	-	ns	
tDTR	$\overline{DT}$ to $\overline{RAS}$ hold time	10	-	10	-	ns	
tRSD	$\overline{RAS}$ to 1st SC delay time	85	-	105	-	ns	
tCSD	$\overline{CAS}$ to 1st SC delay time	35	-	45	-	ns	
tMWS	$\overline{RAS}$ to $\overline{WE}$ set-up time	0	-	0	-	ns	
tMWH	$\overline{RAS}$ to $\overline{WE}$ hold time	15	-	15	-	ns	
tMS	$\overline{RAS}$ to mask data set-up time	0	-	0	-	ns	
tMH	$\overline{RAS}$ to mask data hold time	15	-	15	-	ns	
tSRZ	$\overline{RAS}$ to serial output buffer turn-off delay	10	50	10	60	ns	
tSRS	$\overline{RAS}$ to SC set-up time	30	-	40	-	ns	
tSRD	$\overline{RAS}$ to SC delay time	25	-	30	-	ns	
tSID	$\overline{RAS}$ to serial data-in delay time	50	-	60	-	ns	
tSZD	Serial data-in to $\overline{DT}$ delay time	0	-	0	-	ns	
tES	$\overline{RAS}$ to $\overline{SE}$ set-up time	0	-	0	-	ns	
tEH	$\overline{RAS}$ to $\overline{SE}$ hold time	15	-	15	-	ns	
tSWS	Serial write enable set-up time	0	-	0	-	ns	
tSWH	Serial write enable hold time	30	-	40	-	ns	
tSWIS	Serial write disable set-up time	0	-	0	-	ns	
tSWIH	Serial write disable hold time	30	-	40	-	ns	
tDLZ	$\overline{DT}$ to serial data-out delay time	5	-	10	-	ns	

NOTE

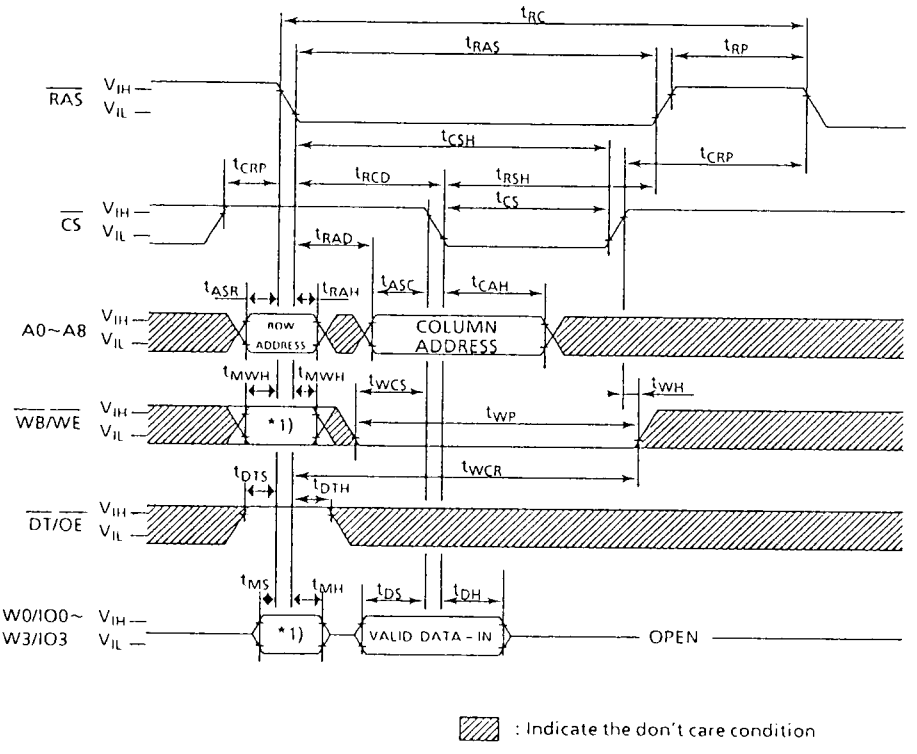
1. It is measured between V_{IH}(min) and V_{IL}(max).
2. Measured with a load circuit equivalent to 100pF and 2TTL.
3. tOFF(max) and tOEZ(max) define the time at which the output achieves the high impedance state (Iout ± 10uA) and are not referenced to V_{OH}(min) or V_{OL}(max)
4. Either tRRH or tRCH must be satisfied for a read cycle.
5. Measured from the $\overline{CS}$ falling edge when the cycle is early write and measured from the $\overline{WB/WE}$ falling edge when read-modify-write.
6. tWS, tWH, tCWD, tRWD and tAWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWS ≧ tWS(min) and tWH ≧ tWH(min), the data out pin will remain open circuit(high inpedance) through the entire cycles ; If tCWD ≧ tCWD(min), tRWD ≧ tRWD(min) and tAWD ≧ tAWD(min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
7. tRCD(max) is specified as a reference point only. When tRCD is less than tRCD(max), access time is tRAC. When tRCD is greater than tRCD(max), access time is tRCD + tCAC.
8. tRAD(max) is specified as a reference point only. When tRAD is less than tRAD(max), access time is tRAC(max). When tRAD is greater than tRAD(max), access time is tRAD + tAA.
9. tAH is the condition to latch column address when $\overline{RAS}$ has risen.
10. Measured with a load equivalent to 50pF and 2 TTL.

TIMING DIAGRAM

Read cycle

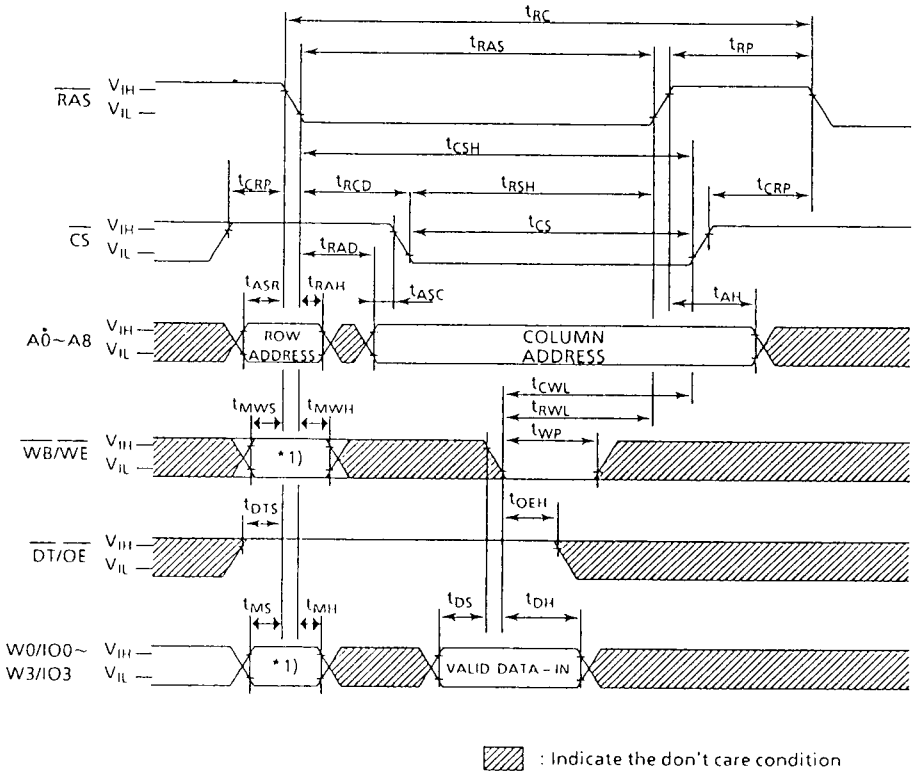


Write cycle (Early Write)



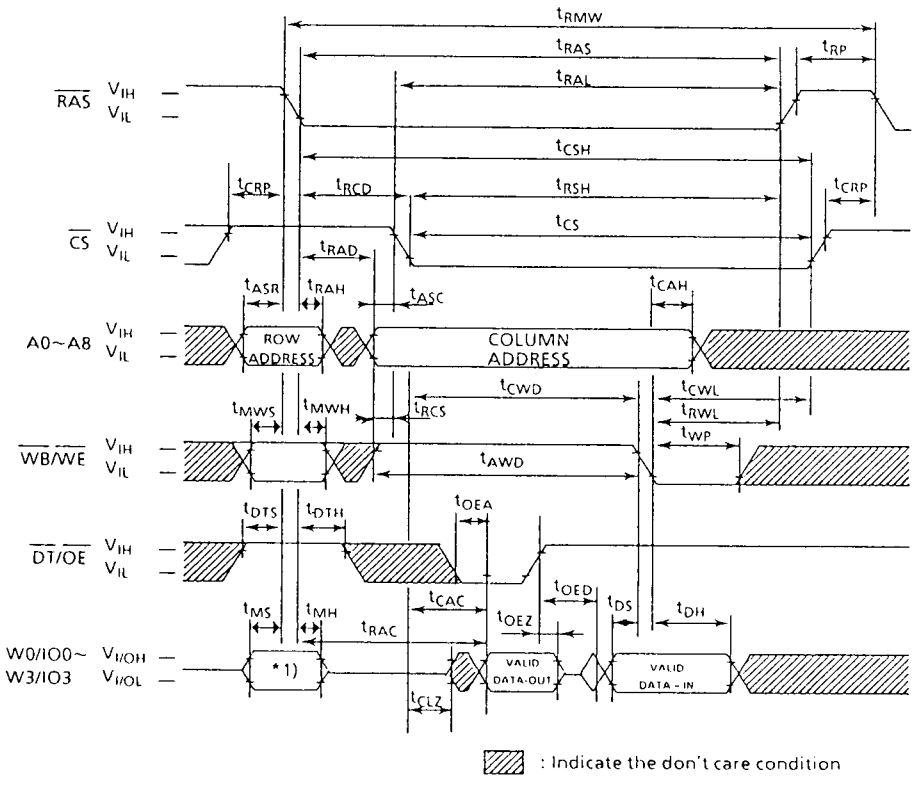
*1) I/O0 – 3 = "H": Non masked
I/O0 – 3 = "L" : Masked

Write cycle ($\overline{DT}/\overline{OE}$ Control Write)



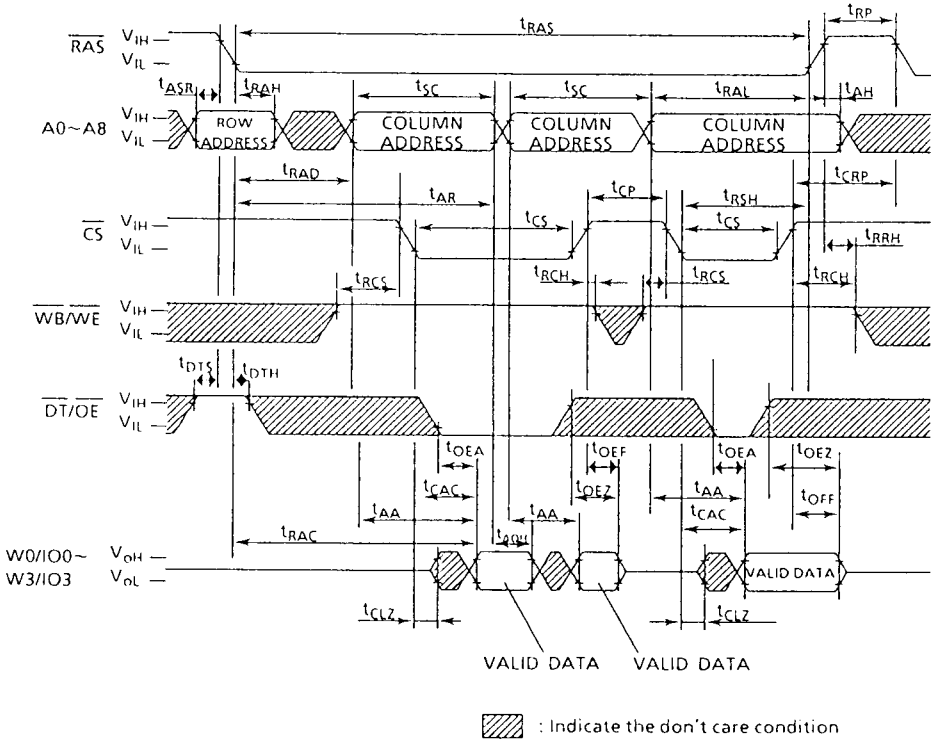
*1) I/O0 – 3 = "H": Non masked
I/O0 – 3 = "L" : Masked

Read Modify Write cycle

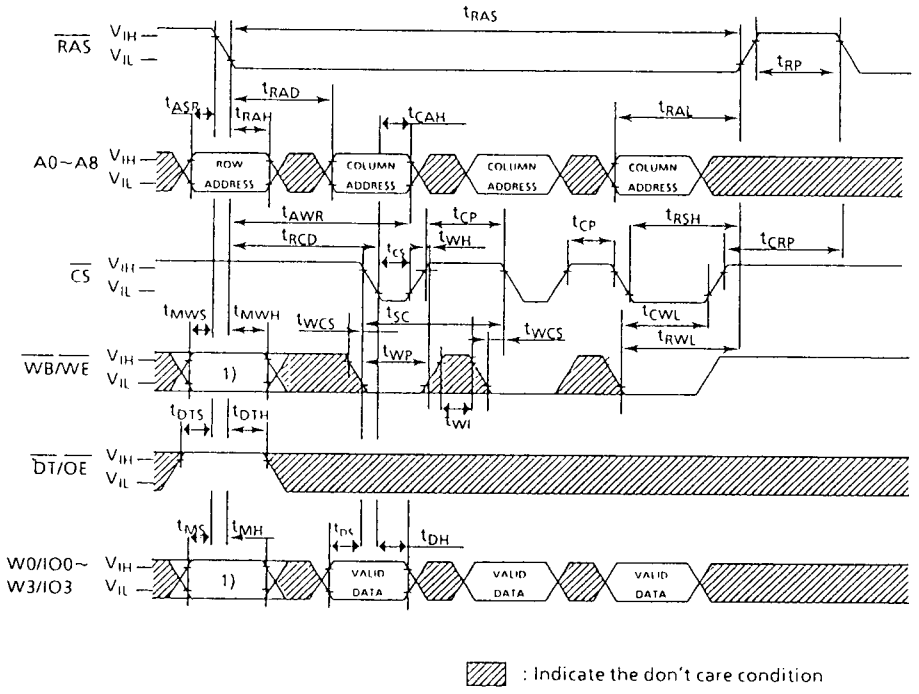


*1) I/O0 – 3 = "H" : Non masked
I/O0 – 3 = "L" : Masked

Static Column Read cycle



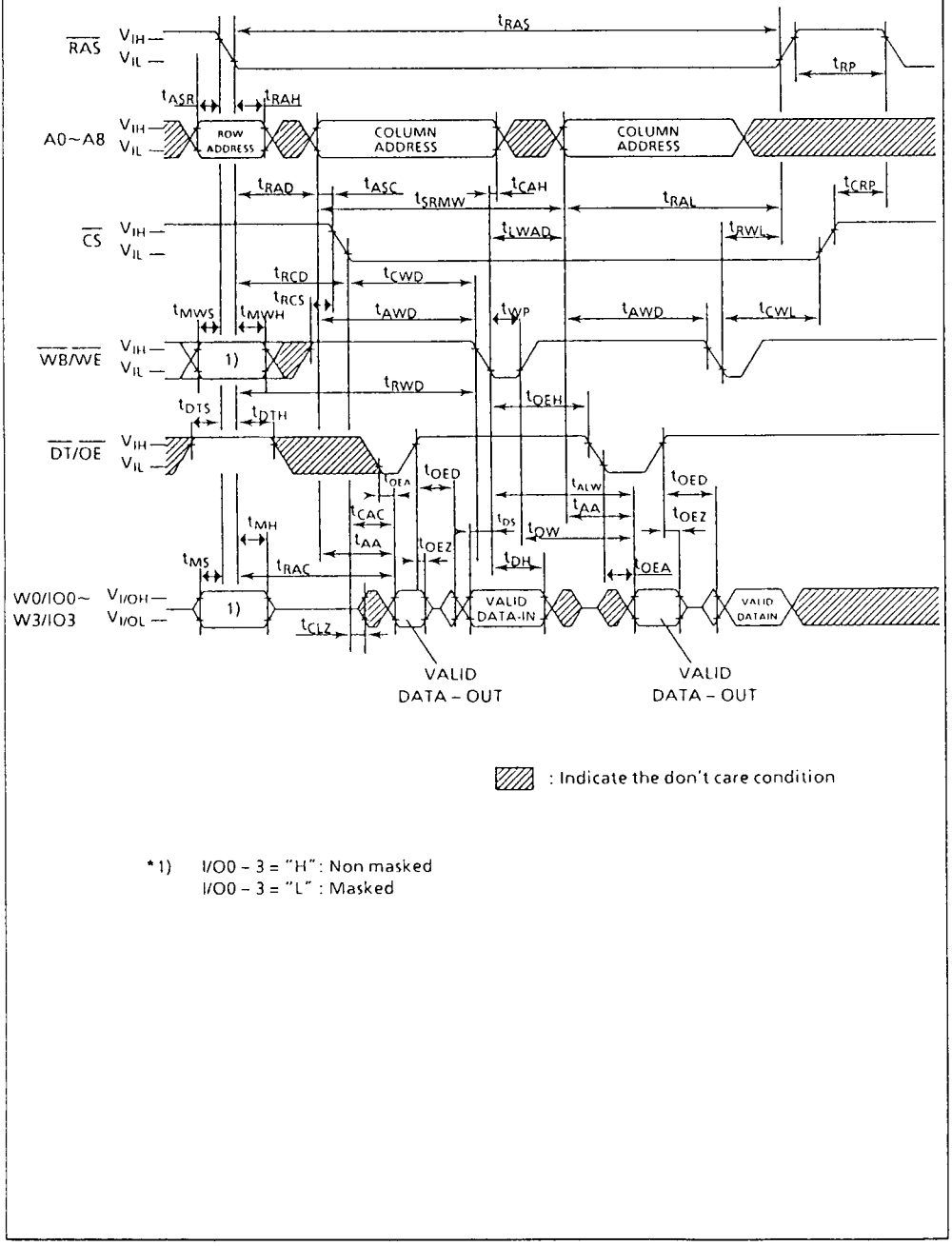
Static Column Write cycle (Early Write)



: Indicate the don't care condition

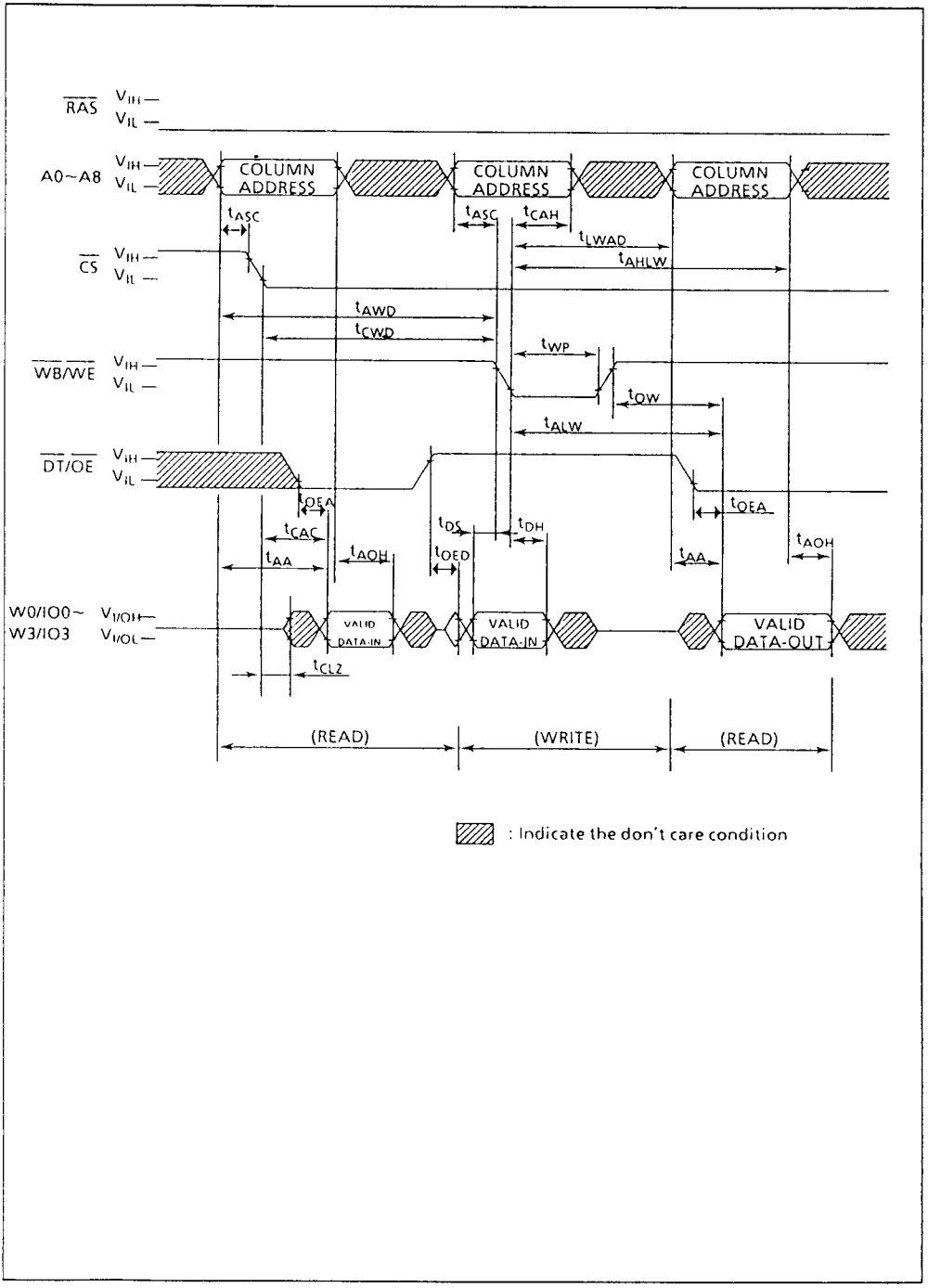
*1) I/O0 – 3 = "H" : Non masked
I/O0 – 3 = "L" : Masked

Static Column Read Modify Write cycle

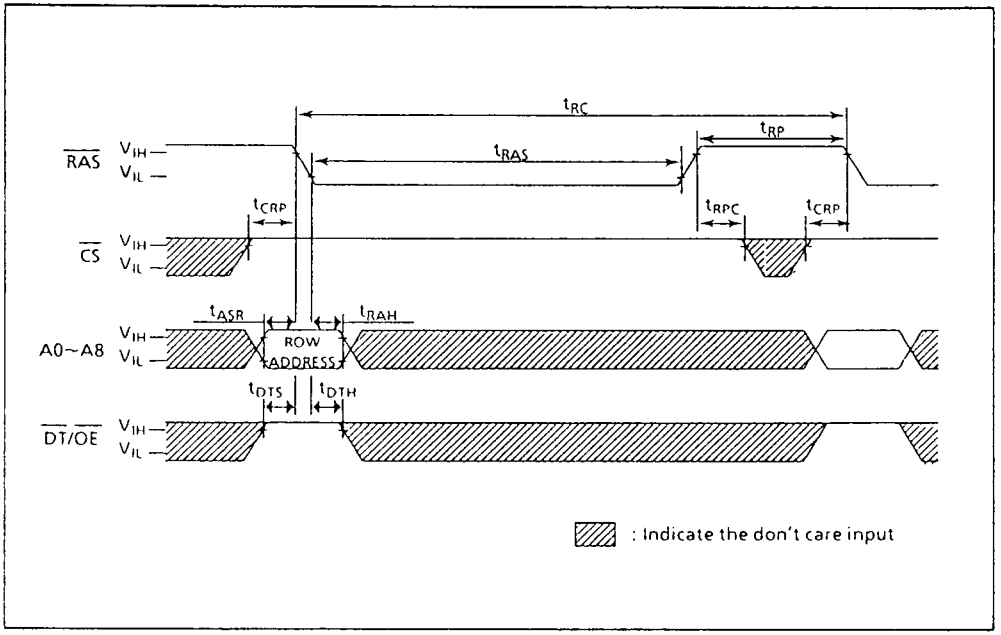


*1) I/O0 – 3 = "H" : Non masked
I/O0 – 3 = "L" : Masked

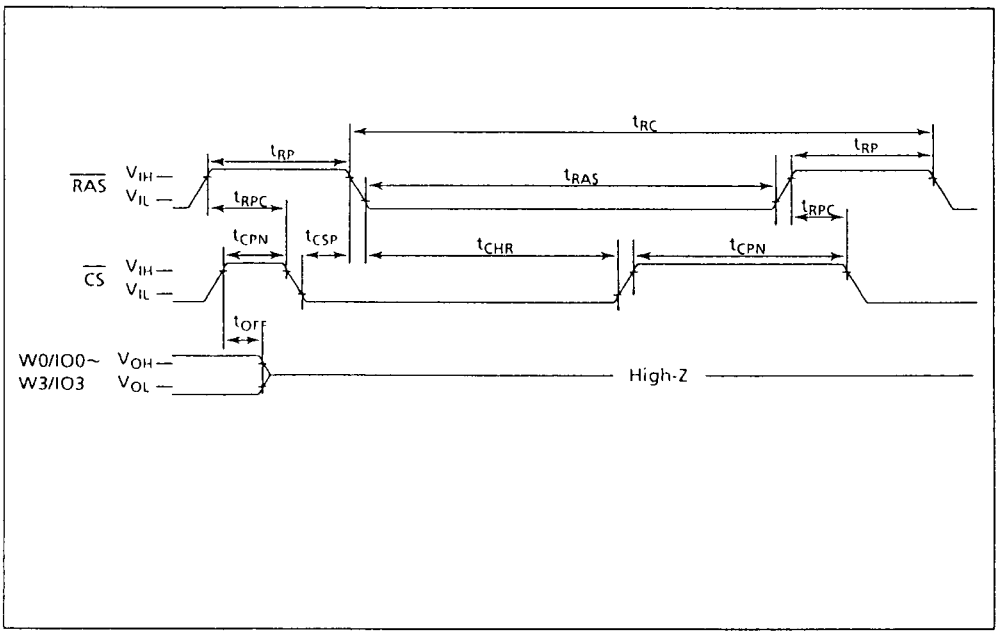
Static Column Read/Write Mix cycle



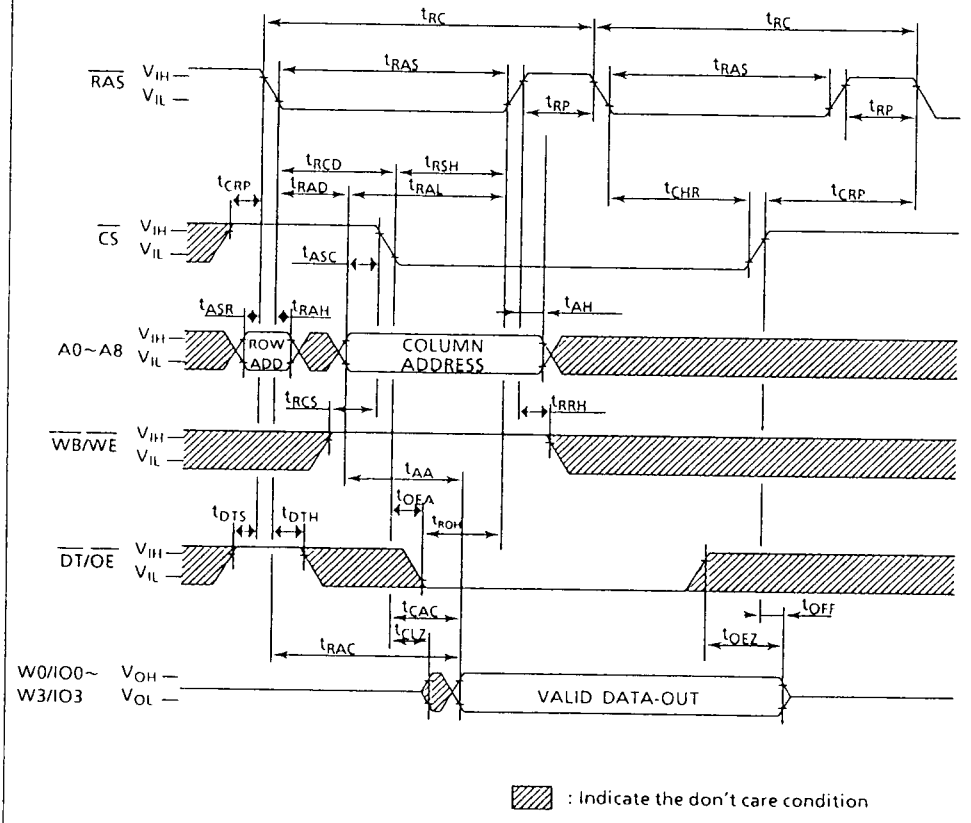
$\overline{RAS}$ Only Refresh cycle



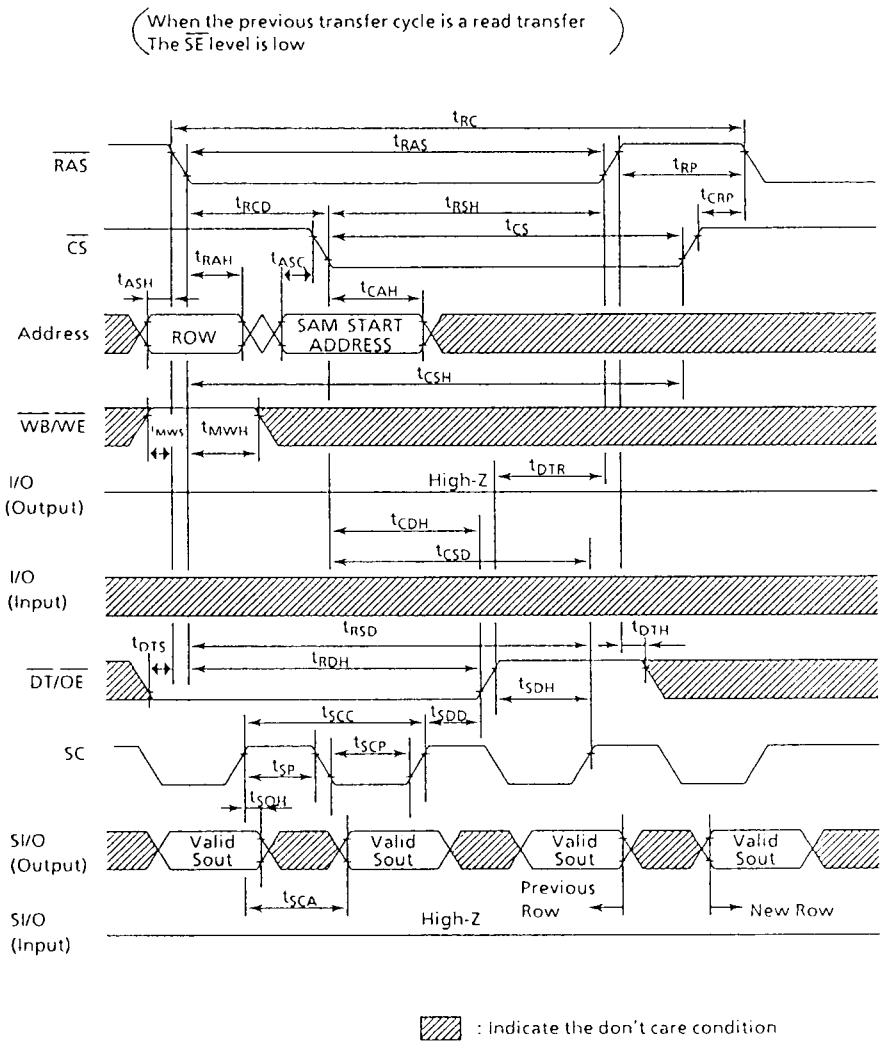
$\overline{CS}$ Before $\overline{RAS}$ Refresh cycle



Hidden Refresh cycle

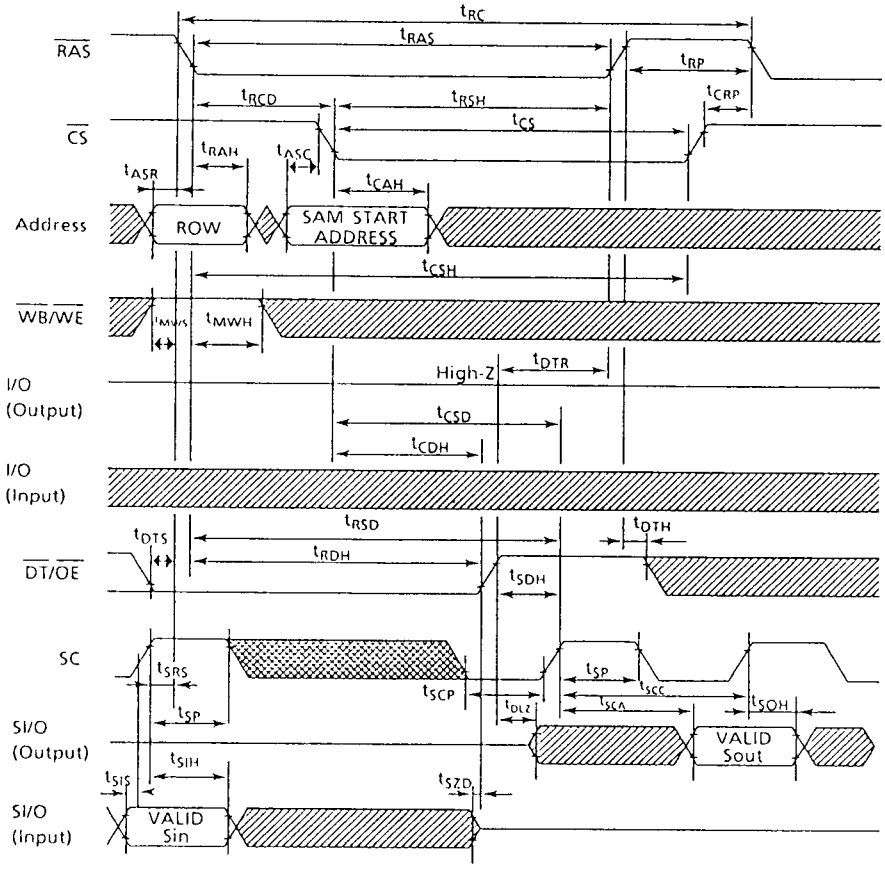


Read Transfer cycle (cycle-1)



Read Transfer cycle (cycle-2)

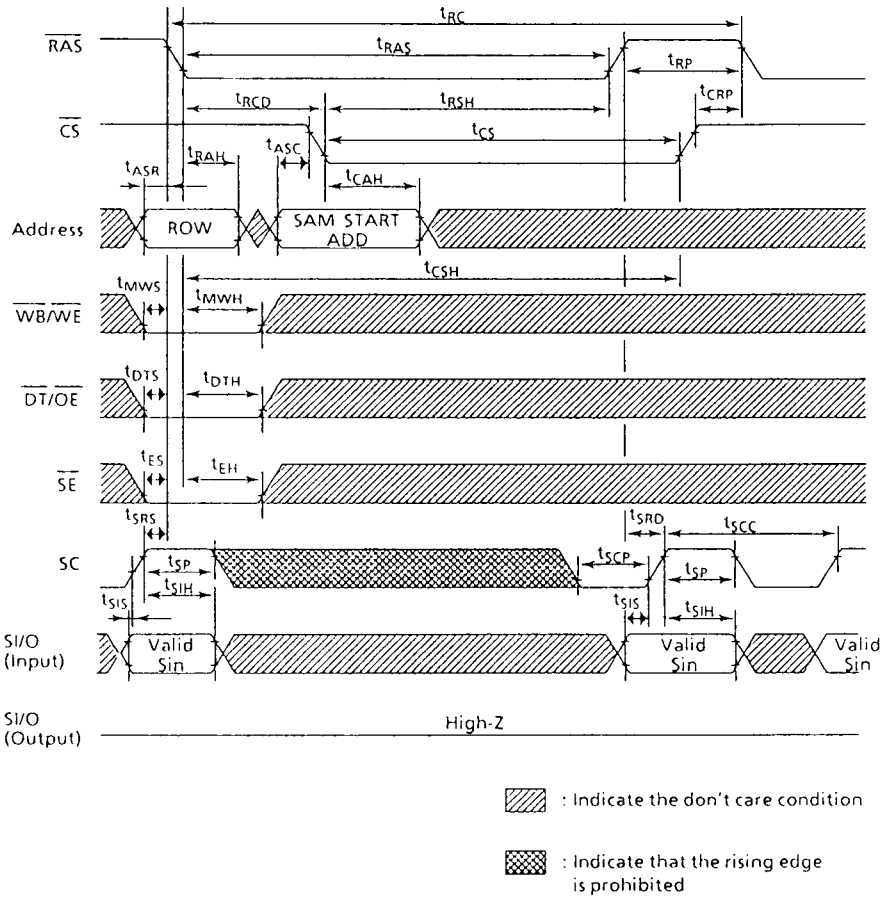
When the previous transfer cycle is a write transfer or a pseudo write transfer
The $\overline{SE}$ level is low



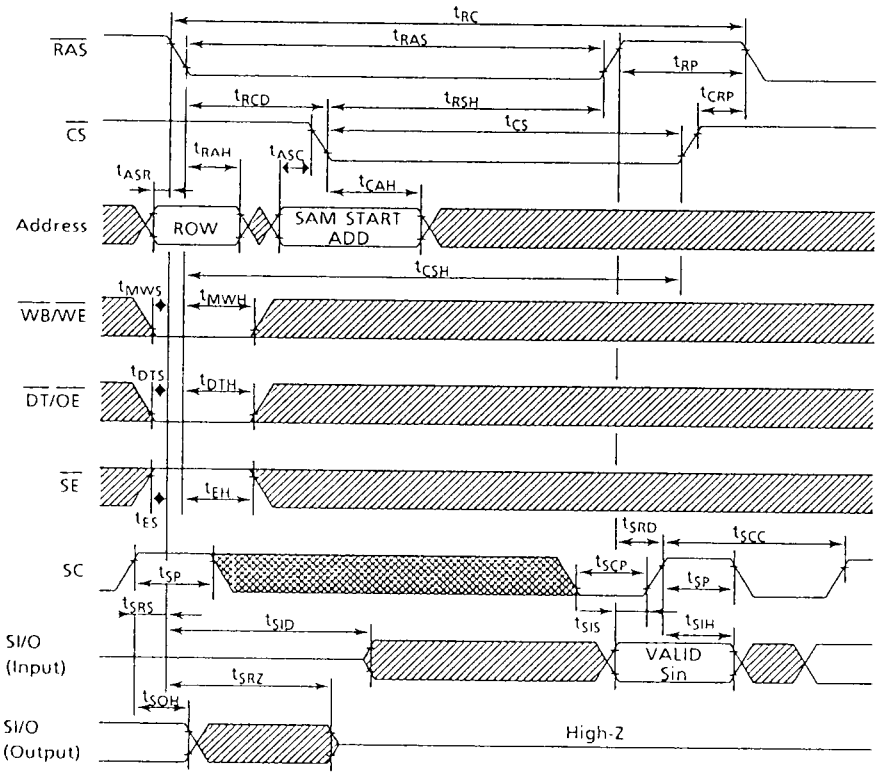
: Indicate the don't care condition

: Indicate that the rising edge is prohibited

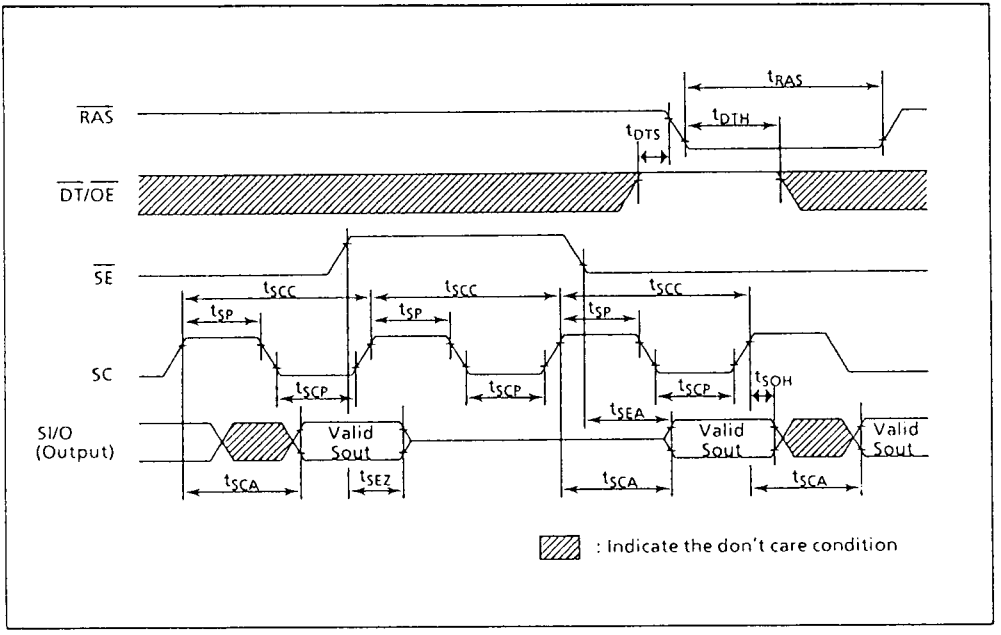
Write Transfer cycle



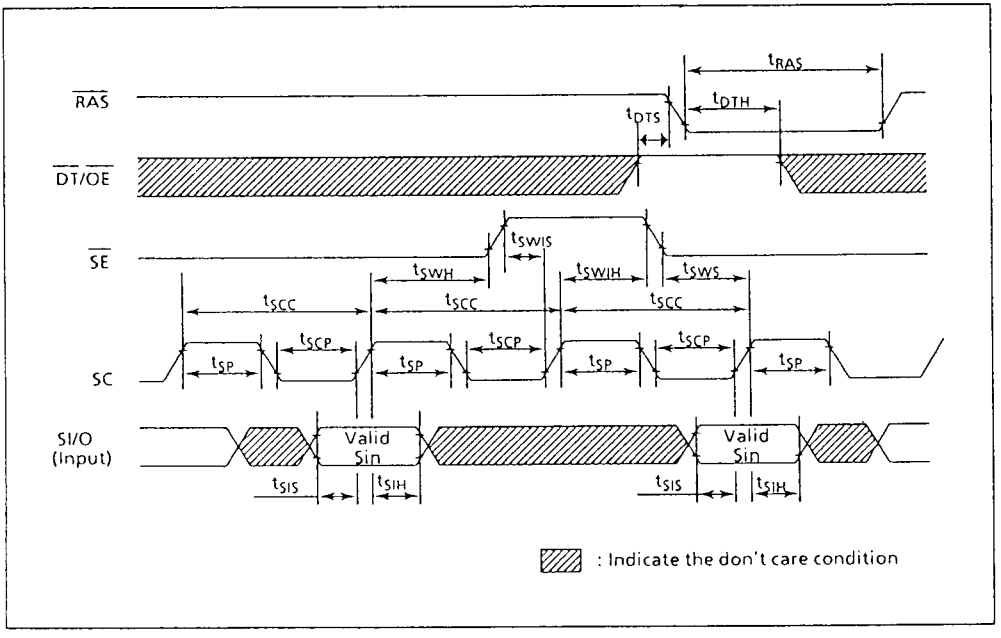
Pseudo Write Transfer cycle



Serial Read cycle



Serial Write cycle



PIN DESCRIPTION

$\overline{RAS}$ (Row Address Strobe-input, active low)
Depending on the states of $\overline{CS}$ and $\overline{DT/OE}$, $\overline{RAS}$ will clock an internal row address (when $\overline{CS}$ before $\overline{RAS}$ mode) or external row address into the row decoder. $\overline{RAS}$ also selects the write-per bit and the data transfer mode.

$\overline{CS}$ (Chip Select-input, active low)
In the data transfer cycle, $\overline{CS}$ will clock an external column address into the column decoder. The selected column address becomes the SAM start address. $\overline{CS}$ is also used as a clock which controls RAM port output impedance. In the static column mode, $\overline{CS}$ is used simply as a Chip Select clock which controls RAM port output impedance.

$\overline{WB/WE}$ (Write per bit/Write Enable-input, active low)
$\overline{WB/WE}$ is sampled when $\overline{RAS}$ falls and decoded in conjunction with $\overline{DT/OE}$ and $\overline{CS}$ according to the Truth Table. When the $\overline{WB/WE}$ level is low at the $\overline{RAS}$ falling edge, the write-per-bit or write transfer cycle is selected. And when $\overline{WB/WE}$ level is high at the $\overline{RAS}$ falling edge, a 4-bit write to the RAM port or a read transfer cycle is selected. That is, if write-per-bit cycle is not selected then $\overline{WB/WE}$ functions as a normal write enable.

$\overline{DT/OE}$ (Data Transfer/Output Enable-input, active low)
The state of $\overline{DT/OE}$ is sampled along with $\overline{WB/WE}$ and $\overline{CS}$ when $\overline{RAS}$ falls. The functions performed are shown in the Truth Table. When the $\overline{DT/OE}$ level at the $\overline{RAS}$ falling edge is low, the data transfer cycle is selected. And when $\overline{DT/OE}$ level is high, the read/write cycle is selected. During random access reads, $\overline{DT/OE}$ functions as the output enable pin.

A0-A8 (Address inputs, active high)
The MSM514251 employs an address-multiplexed-method which inputs the row addresses and the column addresses separately in order to select one word from the 256k words memory cells by using 9 address input pins. In the static column mode, when the $\overline{RAS}$ level is low and the $\overline{CS}$ level is low, various 9 bits column address inputs enable 512 X 4 bits fast column access at a specified row address. In the data transfer cycle, the selected address input is also combined with the serial start address.

I00-I03 (random access data Input and Output-bidirectional, three state)
If the $\overline{WB/WE}$ level is low at the $\overline{RAS}$ falling edge then high level on I00-I03 enables data to be written to the enabled locations ; write-per-bit cycle. I00-I03 also serve as the data I/O pins for the random access port.

SC (Serial Control-input, active high)
Each SC rising edge starts the serial access. In the serial read cycle, the rising edge clocks four bits data from the serial data register to the output pins if $\overline{DT/OE}$ is active. In the serial write cycle, the rising edge clocks four bits data from serial data input pins to the serial data register. If the $\overline{DT/OE}$ level is high, the SC signal is ignored.

$\overline{SE}$ (Serial Enable-input, active low)
$\overline{SE}$ enables serial input/output. When the $\overline{SE}$ level is high at the $\overline{RAS}$ falling edge, the cycle is pseudo-write data transfer cycle. When the $\overline{SE}$ level is low at the $\overline{RAS}$ falling edge, the cycle is write data transfer cycle.

SIO0-SIO3 (Serial access data Input and Output-bidirectional, three state)
Serial data appears if SE is active, otherwise they are high impedance

FUNCTION

RAM Port Operation

The row address is specified by the $\overline{RAS}$ clock. The MSM514251 has a static column capability so that the internal column address is specified directly by the input address, not specified by $\overline{CS}$ as in fast page mode devices.

The MSM514251 read/write cycle is set up by maintaining the $\overline{DT/OE}$ level high, while the RAS clock is falling. Data is read out when the $\overline{DT/OE}$ level is low and is written when the WB/WE level is low.

In the static column cycle, when both the $\overline{RAS}$ level and the $\overline{CS}$ level are low, the column data in one specified row can be read/write continually according to the changes of column address inputs.

When the $\overline{WB/WE}$ clock falls before the $\overline{CS}$ falling edge, it becomes an early write cycle. When the WB/WE clock falls after the $\overline{CS}$ falling edge, it becomes a late write cycle.

In the random write cycle, the write-per-bit function is available.

SAM Port Operation

The data transfer cycle is set up when the $\overline{DT/OE}$ level is low at the $\overline{RAS}$ falling edge. A read data transfer cycle is performed when $\overline{WB/WE}$ is high. A write data transfer cycle is performed when $\overline{WB/WE}$ is low.

In the data transfer cycle, the row/column addresses are specified by the $\overline{RAS/CS}$ clocks, then the row address selests one row of RAM memory array and the column address selects the serial access start address.

- In the cycle which begins when the $\overline{DT/OE}$ level is high at the $\overline{RAS}$ falling edge, RAM and SAM are accessed independently. At the time, if the $\overline{DT/OE}$ level is low, the data transfer between RAM and SAM occurs.
  In one data transfer cycle, 512 X 4 bits data are transferred between the serial data register and any rows in the RAM array.

- The data transfer direction is selected by the WE level at the $\overline{RAS}$ falling edge.
  From RAM to SAM (Read Data Transfer) : $\overline{WB/WE}$ = "H"
  From SAM to RAM (Write Date Transfer) : $\overline{WB/WE}$ = "L"

- Transfer cycle decides the following serial access cycles.
  Read data transfer - - - - → Serial read cycle
  Write data transfer - - - - → Serial write cycle
  (Pseudo write data transfer - - - - → Serial write cycle)

- No data transfer occurs from serial data register to RAM array when the $\overline{SE}$ level is high at the $\overline{RAS}$ falling edge in the write data transfer cycle. The data transfer is referred to as a pseudo write data transfer.

- During a read data transfer, a high speed data transfer execution is started at the $\overline{DT/OE}$ rising edge.

REFRESH OPERATION

Three operation methods for refreshing the MSM514251 dynamic RAM cells are available to users. The refresh operations on all 512 row addresses are required in every 8 ms.

• $\overline{RAS}$ Only Refresh

$\overline{RAS}$ only refresh is similar to a read cycle using any row address, except that $\overline{CS}$ is high throughout the cycle and no column address is required. All the column data in the designated row address are refreshed simultaneously.

• $\overline{CS}$ Before $\overline{RAS}$ Refresh

CS before RAS refresh uses an internal 9 bits refresh counters as the row address specifying the row to be refreshed. One $\overline{CS}$ before $\overline{RAS}$ cycle increments an internal refresh counter one address. The refresh counter will be incremented each subsequent $\overline{CS}$ before $\overline{RAS}$ cycle.

• Hidden Refresh

Hidden refresh is similar to $\overline{CS}$ before $\overline{RAS}$ refresh, except that the $\overline{CS}$ level and the $\overline{DT/OE}$ level remain low. The data which was read in the previous cycle is held throughout the refresh period.

DATA TRANSFER OPERATION

• Read Data Transfer

Depending on the states of the $\overline{DT/OE}$ and $\overline{WB/WE}$ level at the $\overline{RAS}$ falling edge, (see the Truth Table), the Read Data Transfer Cycle is selected. The column data of one row designated by the row address are transferred to the serial shift data register.

At the same time, the decoded column address is set to the secondary serial register or serial address selector which determines the serial read start address. This function is referred to as the pointer control. After the data transfer, every SC rising edge enables a serial data output and the serial address selector moves into the next bit.

As the serial address selector is cyclical in nature, the same data from the start address is output again when the SC clock is input more than 513 times.

$\overline{SE}$ controls the serial output buffers. When the $\overline{SE}$ level is low, the serial register data are output. When the $\overline{SE}$ level is high, the SIO0-SIO3 are at high impedance. The serial address selector has no relation with the $\overline{SE}$ level and shifts one bit at every SC rising edge.

Serial read data transfer can be done when SAM is in operation. That is the data from different rows can be continuously output. This operation is referred to as the Real Time Data Transfer.

• Write Data Transfer

Depending on the states of the $\overline{DT/OE}$, $\overline{WB/WE}$ and $\overline{SE}$ level at the $\overline{RAS}$ falling edge, (see the Truth Table), the Write Data Transfer Cycle is selected. The data on the serial data registers are transferred to the one row of RAM array which is designated by the row address.

At the same time, the decoded column address is set to the secondary serial register or serial address selector which determines the serial write start address. After the data transfer, every SC rising edge enables a serial data input and the serial address selector moves into the next bit. The data input to the SIO0-SIO3 pins are written into the serial data register or SAM.

As the serial address selector is cyclical in nature, the start write address on the serial data register comes again when the SC clock is input more than 513 times.

$\overline{SE}$ controls the serial input buffers. When the $\overline{SE}$ level is low, the input data are written into SAM. The serial address selector is not related to the $\overline{SE}$ level and shifts one bit at every SC rising edge. So when the $\overline{SE}$ level is high, the SC clock only shifts the serial address selector without writing the data in SAM.

• Pseudo Write Transfer

Depending on the states of the $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and SE level at the $\overline{RAS}$ falling edge, (see the Truth Table), the Pseudo Write Data Transfer Cycle is selected. The operation is the same as the write data transfer operation except for the fact that the data on the serial data register are not transferred to the RAM array. The row address which is input is ignored.

When the mode changes from serial read to serial write, pseudo write a transfer is used so that the one row data of RAM designated by the row address are not destroyed and are also used to change the mode of the serial port.

The difference between the read transfer and the write/pseudo-write transfer is that the write transfer and pseudo transfer cannot be done while SAM is operating.

POWER ON

An initial pause of 500 µsec is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles before proper operation is achieved. Note that RAS may be cycled during the initial pause. And $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods (greater than 8msec) of $\overline{RAS}$ inactivity before proper device operation is achieved.

After the above operation, prior to the SAM operation, the serial access mode must be selected by performing a data transfer cycle.

TRUTH TABLE (Mode Selection)

Input pin state at RAS falling				RAM	RAM	SAM
$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	I/O0-3		Bit Mask	SIO1-3
H	X	X	X	READ	-	-
H	X	X	X	WRITE	-	-
H	L	X	H	Write-Per-Bit	Non Masked	-
H	L	X	L	Write-Per-Bit	Masked	-
L	H	X	X	Read Transfer	-	Output Mode
L	L	L	X	Write Transfer	-	Input Mode
L	L	H	X	Pseudo Write Transfer	-	Input Mode