HM621664H/HM621864H Series — Preliminary

65536-word × 16/18-bit High Speed CMOS Static RAM

The HM621664H/HM621864H is an asyncronous high speed static RAM organized as 64 kword × 16/18 bit. It realize high speed access time (15/17/20/25 ns) with employing 0.8 µm CMOS process and high speed circuit designing technology.

It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system.

The HM621664H/HM621864H is packaged in 400-mil 44-pin SOJ & TSOP-II for high density surface mounting.

Features

- Single 5 V supply: 5 V ± 10%
- Access time 15/17/20/25 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- 400-mil 44-pin SOJ & TSOP-II package
- Center V_{CC} and V_{SS} type pinout

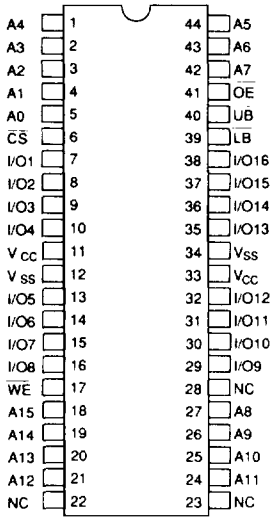
Ordering Information

Type No.	Access time	Package
HM621664HJP-15	15 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM621664HJP-17	17 ns	
HM621664HJP-20	20 ns	
HM621664HJP-25	25 ns	
HM621664HLJP-15	15 ns	
HM621664HLJP-17	17 ns	
HM621664HLJP-20	20 ns	
HM621664HLJP-25	25 ns	
HM621864HJP-15	15 ns	
HM621864HJP-17	17 ns	
HM621864HJP-20	20 ns	
HM621864HJP-25	25 ns	
HM621864HLJP-15	15 ns	
HM621864HLJP-17	17 ns	
HM621864HLJP-20	20 ns	
HM621864HLJP-25	25 ns	
HM621664HTT-15	15 ns	400-mil 44-pin plastic TSOP-II normal bend type (TTP-44DE)
HM621664HTT-17	17 ns	
HM621664HTT-20	20 ns	
HM621664HTT-25	25 ns	
HM621664HLTT-15	15 ns	
HM621664HLTT-17	17 ns	
HM621664HLTT-20	20 ns	
HM621664HLTT-25	25 ns	
HM621864HTT-15	15 ns	
HM621864HTT-17	17 ns	
HM621864HTT-20	20 ns	
HM621864HTT-25	25 ns	
HM621864HLTT-15	15 ns	
HM621864HLTT-17	17 ns	
HM621864HLTT-20	20 ns	
HM621864HLTT-25	25 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

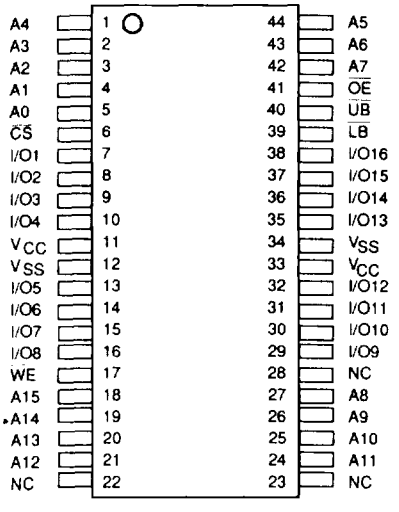
Pin Arrangement

HM621664HJP (SOJ)



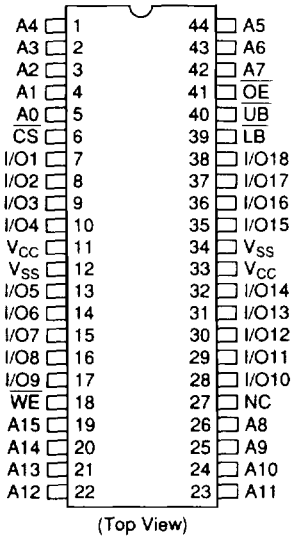
(Top View)

HM621664HTT
(Normal Bend TSOP-II)



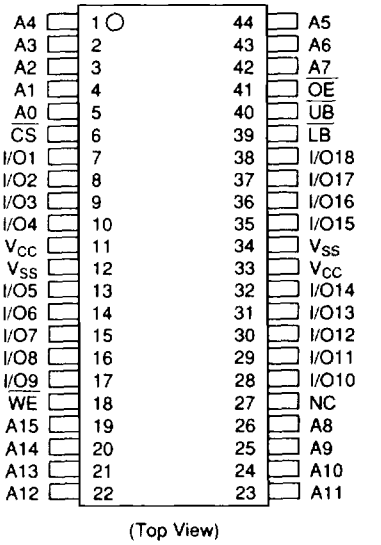
(Top View)

HM621864HJP (SOJ)



(Top View)

HM621864HTT
(Normal Bend TSOP-II)



(Top View)

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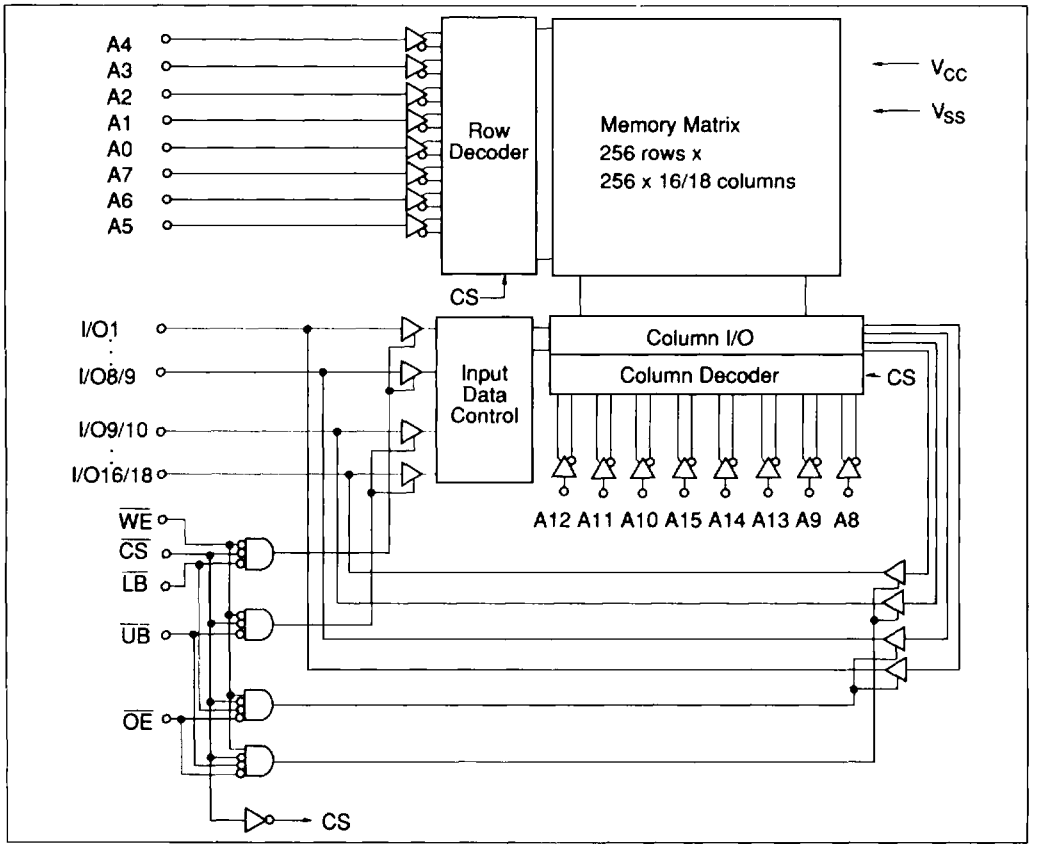
Pin Description

Pin name

HM621664H	HM621864H	Function
A0 – A15	A0 – A15	Address
I/O1 – I/O8	I/O1 – I/O9	Input/output (lower byte)
I/O9 – I/O16	I/O10 – I/O18	Input/output (upper byte)
$\overline{CS}$	$\overline{CS}$	Chip select
$\overline{LB}$	$\overline{LB}$	Lower byte select
$\overline{UB}$	$\overline{UB}$	Upper byte select
$\overline{WE}$	$\overline{WE}$	Write enable
$\overline{OE}$	$\overline{OE}$	Output enable
V_{CC}	V_{CC}	Power supply
V_{SS}	V_{SS}	Ground
NC	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	−0.5 *1 to V_{CC} + 0.5	V
Power dissipation	P_T	1.0*2 / 1.5*3	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −2.5 V for pulse width (under shoot) ≤ 10 ns
2. at still air condition
3. at air flow ≥ 1.0 m/s

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	V_{CC} current	I/O (Lower byte)	I/O (Upper byte)	Ref. cycle
H	X	X	X	X	I_{SB}, I_{SB1}	High-Z	High-Z	—
L	H	H	X	X	I_{CC}	High-Z	High-Z	—
L	L	H	L	L	I_{CC}	Output	Output	Read cycle
L	L	H	L	H	I_{CC}	Output	High-Z	Read cycle
L	L	H	H	L	I_{CC}	High-Z	Output	Read cycle
L	L	H	H	H	I_{CC}	High-Z	High-Z	—
L	X	L	L	L	I_{CC}	Input	Input	Write cycle
L	X	L	L	H	I_{CC}	Input	High-Z	Write cycle
L	X	L	H	L	I_{CC}	High-Z	Input	Write cycle
L	X	L	H	H	I_{CC}	High-Z	High-Z	—

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage*2	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	−0.5 *1	—	0.8	V

Note: 1. −2.0 V for pulse width (under stoot) ≤ 10 ns
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$V_{I/O}$ = V_{SS} to V_{CC}	1
Operating power supply current	I_{CC}	—	190	260	mA	15 ns cycle, $\overline{CS}$ = V_{IL}, Iout = 0 mA, Other inputs = V_{IH}/V_{IL}	
		—	175	240	mA	17 ns cycle	
		—	160	220	mA	20 ns cycle	
		—	145	200	mA	25 ns cycle	
Standby power supply current	I_{SB}	—	70	100	mA	15 ns cycle, $\overline{CS}$ = V_{IH}, Other inputs = V_{IH}/V_{IL}	
		—	60	95	mA	17 ns cycle	
		—	50	90	mA	20 ns cycle	
		—	40	85	mA	25 ns cycle	
Standby power supply current (1)	I_{SB1}	—	—	2	mA	V_{CC} ≥ $\overline{CS}$ ≥ V_{CC} − 0.2 V, 0 V ≤ Vin ≤ 0.2 V or V_{CC} ≥ Vin ≥ V_{CC} − 0.2 V	
		—	—	0.1	mA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

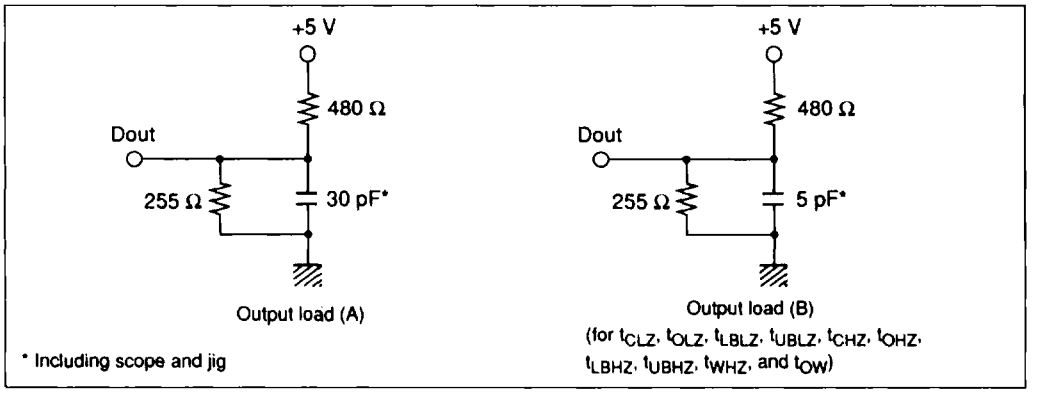
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



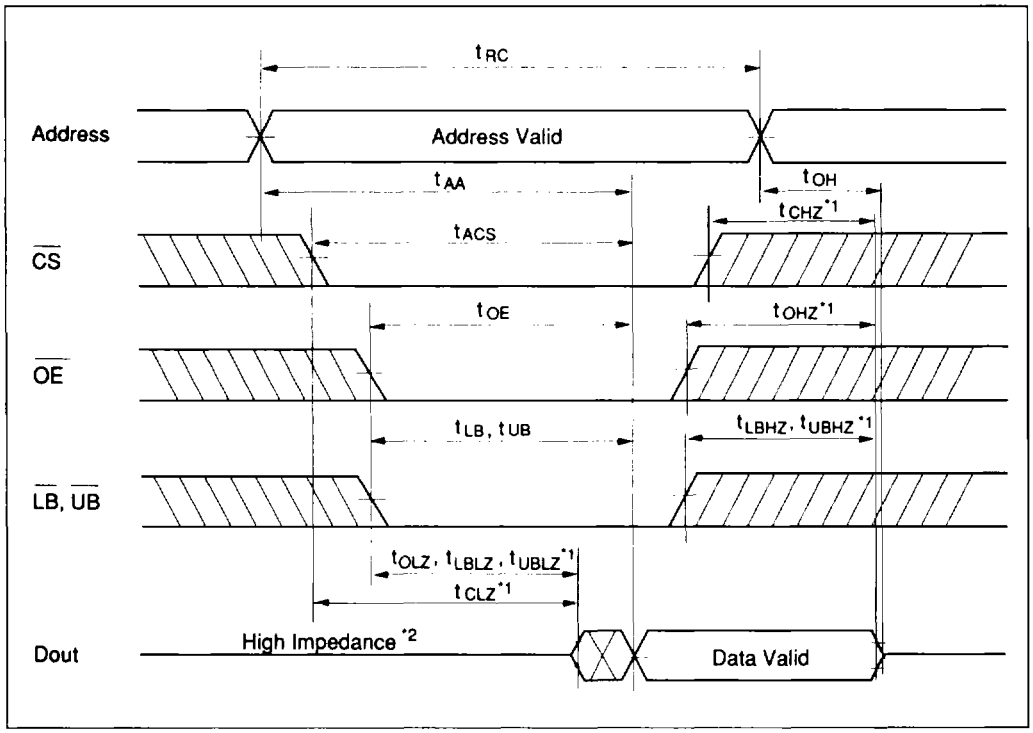
Read Cycle

		HM621664H/HM621864H								
		-15		-17		-20		-25		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	15	—	17	—	20	—	25	—	ns
Address access time	t_{AA}	—	15	—	17	—	20	—	25	ns
Chip select access time	t_{ACS}	—	15	—	17	—	20	—	25	ns
Output enable to output valid	t_{OE}	—	8	—	8	—	10	—	12	ns
Byte select to output valid	t_{LB}, t_{UB}	—	8	—	8	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	5	—	ns
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	3	—	3	—	ns
Output enable to output in low-Z	t_{OLZ}	1	—	1	—	1	—	1	—	ns
Byte select to output in low-Z	t_{LBLZ}, t_{UBLZ}	1	—	1	—	1	—	1	—	ns
Chip deselect to output in high-Z	t_{CHZ}	—	7	—	7	—	7	—	7	ns

Read Cycle (cont)

Parameter	Symbol	HM621664H/HM621864H -15 Min	-15 Max	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max	Unit
Output disable to output in high-Z	t_{OHZ}	—	7	—	7	—	7	—	7	ns
Byte deselect to output in high-Z	t_{LBHZ}, t_{UBHZ}	—	7	—	7	—	7	—	7	ns

Read Timing Waveform *3

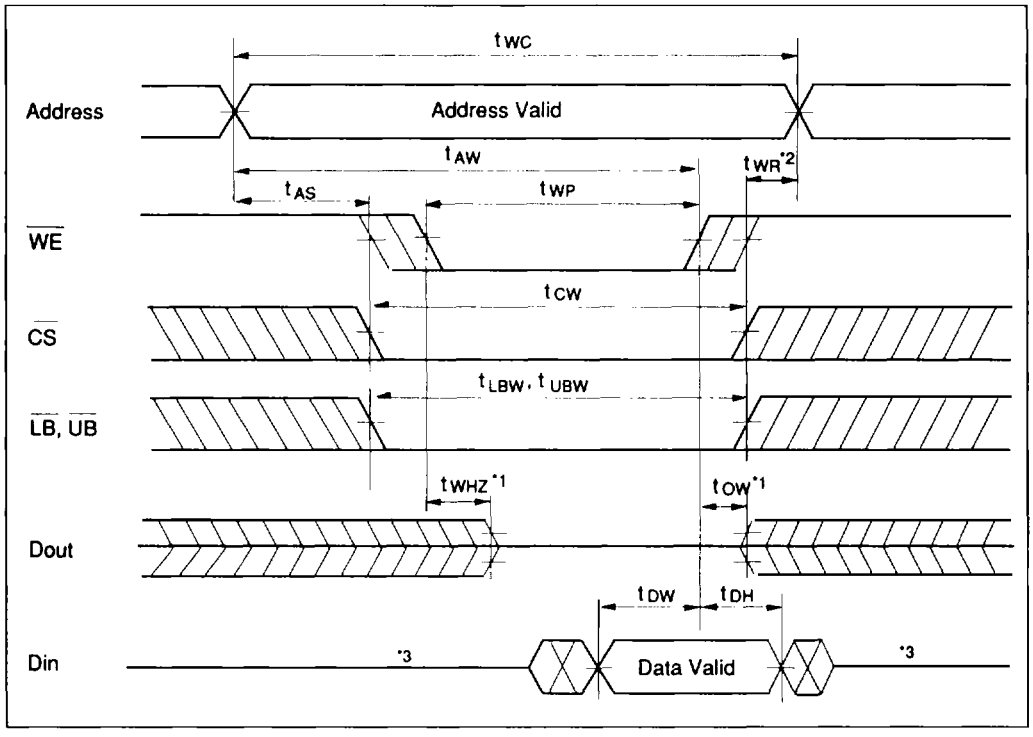


Notes: 1. Transition is measured ±200 mV from steady state's voltage with Load (B). This parameter is sampled and not 100% tested.
2. When $\overline{CS}$, $\overline{OE}$, and $\overline{LB}$ are low, Dout (lower byte) is low impedance.
When $\overline{CS}$, $\overline{OE}$, and $\overline{UB}$ are low, Dout (upper byte) is low impedance.
3. $\overline{WE}$ is high for read cycle.

Write Cycle

		HM621664H/HM621864H								
		-15		-17		-20		-25		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	15	—	17	—	20	—	25	—	ns
Address valid to end of write	t_{AW}	12	—	12	—	15	—	20	—	ns
Chip select to end of write	t_{CW}	10	—	10	—	12	—	15	—	ns
Write pulse width	t_{WP}	10	—	10	—	12	—	15	—	ns
Byte select to end of write	t_{LBW}, t_{UBW}	10	—	10	—	12	—	15	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	0	—	0	—	ns
Data to write time overlap	t_{DW}	8	—	8	—	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write disable to output in low-Z	t_{OW}	3	—	3	—	3	—	3	—	ns
Write enable to output in high-Z	t_{WHZ}	—	7	—	7	—	7	—	7	ns

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



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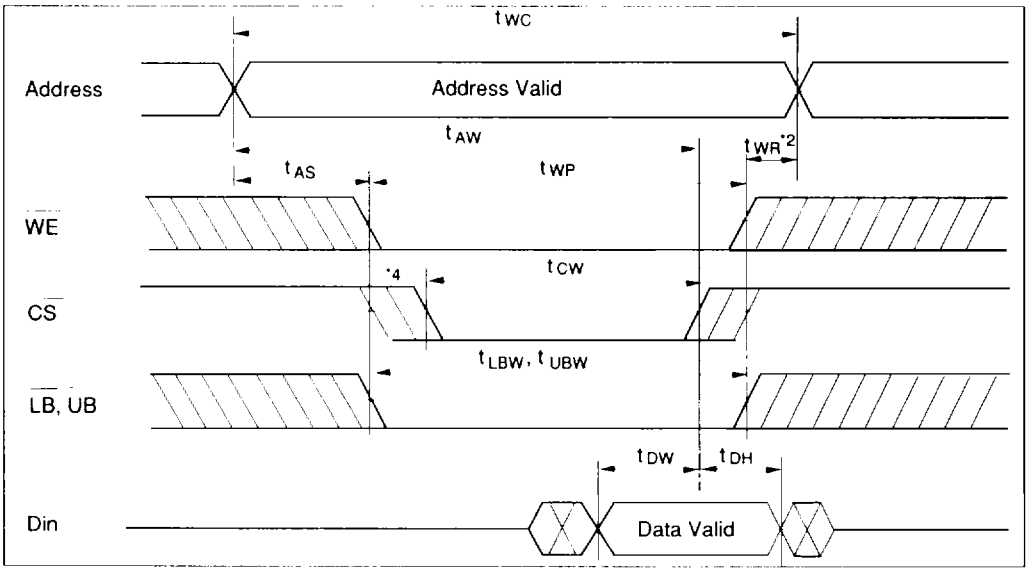
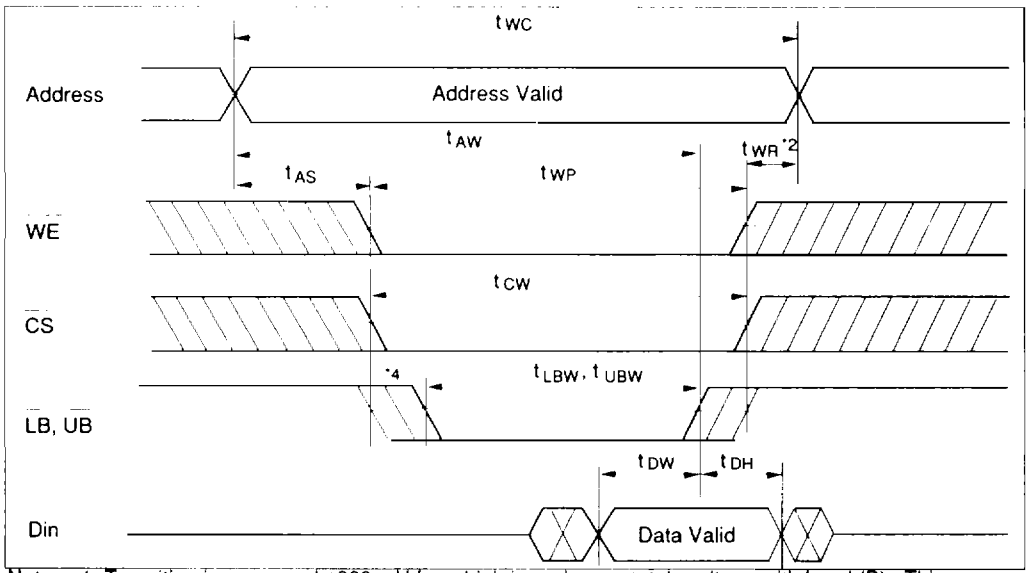
Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Write Timing Waveform (3) ($\overline{LB}$, $\overline{UB}$ Controlled)



Notes: 1. Transition is measured ±200 mV from high impedance state's voltage with Load (B). This parameter is sampeld and not 100% tested.

2. $\overline{WE}$ must be high during address transition except when the device is disabled with $\overline{CS}$, $\overline{LB}$, or $\overline{UB}$.
3. If $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, and $\overline{UB}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
4. If the $\overline{CS}$ or $\overline{LB}$ or $\overline{UB}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.

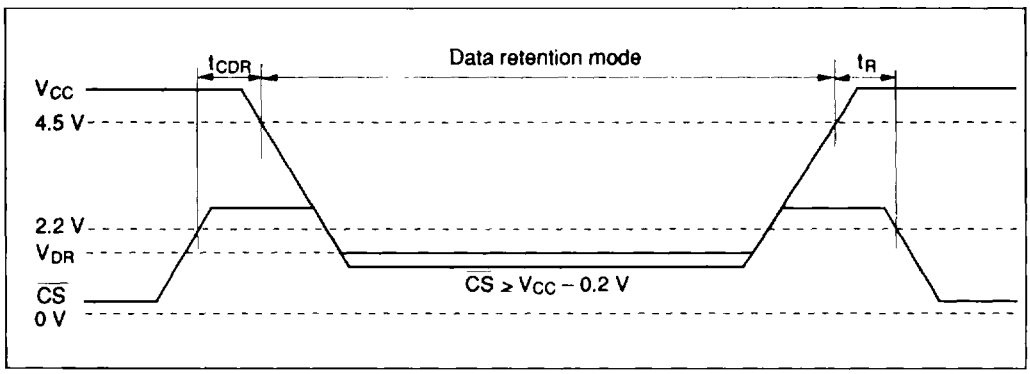
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, $V_{CC} \geq Vin \geq V_{CC} - 0.2$ V or $0\ V \leq Vin \leq 0.2$ V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



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