



SANYO Semiconductors

**DATA SHEET****LV23100AT**

Bi-CMOS IC

For Portable Audio System

**1-chip Tuner IC****Incorporating PLL****Overview**

The LV23100V is a one-chip tuner IC incorporating PLL for portable audio system.

**Functions**

- AM tuner
- FM tuner
- MPX stereo decoder
- PLL frequency synthesizer

**Specifications**

**Maximum Ratings** at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max	V <sub>CC</sub>	4.0	V
	V <sub>DD</sub> max	V <sub>DD</sub>	4.0	V
Maximum input voltage	V <sub>IN1</sub> max	CE, CI, CL	6.0	V
	V <sub>IN2</sub> max	XIN	V <sub>DD</sub> +0.3	V
Allowable power dissipation	Pd max	Ta≤70°C	180	mW
Maximum output voltage	V <sub>O1</sub> max	DO	6.0	V
	V <sub>O2</sub> max	XOUT, PD	V <sub>DD</sub> +0.3	V
	V <sub>O3</sub> max	BO1, BO2, AOUT	12.0	V
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Note : This product should be handled with care because the resistance against electrostatic discharge damage is low.

- CCB is a registered trademark of SANYO Electric Co., Ltd.
- CCB is SANYO Semiconductor's original bus format. All bus addresses are managed by SANYO Semiconductor for this format.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

**SANYO Semiconductor Co., Ltd.**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

**Operating Condition** at  $T_a = 25\text{ }^\circ\text{C}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}$		3.0	V
	$V_{DD}$		3.0	V
Operating supply voltage range	$V_{CC\text{ op}}$		2.2 to 3.6	V
	$V_{DD\text{ op}}$		2.2 to 3.6	V

**PLL block Allowable Operating Range** at  $T_a = -20\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		2.2		3.6	V
Input high level voltage	$V_{IH}$	CE, CL, DI	$0.7V_{DD}$		6.0	V
Input low level voltage	$V_{IL}$	CE, CL, DI	0		$0.3V_{DD}$	-
Output voltage	$V_{O1}$	DO	0		6.0	V
	$V_{O2}$	BO1, BO2, AOUT	0		10	V
Operating frequency	$f_{IN1}$	XIN ; $V_{IN1}$		75		kHz
	$f_{IN2}$	FMIN ; $V_{IN2}$	10		160	MHz
	$f_{IN3}$	AMIN (SNS = 1) ; $V_{IN3}$	2		40	MHz
	$f_{IN4}$	AMIN (SNS = 0) ; $V_{IN4}$	0.5		10	MHz

Note : Due attention must be paid on leak because the XIN pin has an extremely high input impedance.

**Operating Characteristics** at  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = V_{DD} = 3.0\text{V}$ , See the specified circuit.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Current dissipation]						
FM tuner block	$I_{CCFM}$	No input in FM mode	9	12.5	16	mA
AM tuner block	$I_{CCAM}$	No input in AM mode	4	6	8	mA
PLL block	$I_{DDFM}$	$f_r = 98\text{MHz}$ , No input at tuner	1	2	4	mA
[FM-FE characteristics] : $f_c = 98\text{MHz}$ , $f_m = 1\text{kHz}$ , $dev = 22.5\text{kHz}$						
3dB sensitivity	-3dBLS	$V_{IN} = 60\text{dB}\mu\text{V}$ EMF reference, -3dB input		10		$\text{dB}\mu\text{V}$ EMF
Actual sensitivity	QS	S/N = Input at S/N = 30dB		13		$\text{dB}\mu\text{V}$ EMF
[FM-IF characteristics] : $f_c = 10.7\text{MHz}$ , $f_m = 1\text{kHz}$ , $dev = 75\text{kHz}$ (L+R = 90%, Pilot = 10%)						
Demodulation output	$V_O$	$V_{IN} = 100\text{dB}\mu\text{V}$	140	180	210	mVrms
3dB sensitivity	LS	$V_{IN} = 100\text{dB}\mu\text{V}$ reference, -3dB input	26	31	36	$\text{dB}\mu\text{V}$
Signal-to-noise ratio	S/N	$V_{IN} = 100\text{dB}\mu\text{V}$	63	70		dB
IF count sensitivity	IF-C1	0%mod, SDC = 1	42	50	56	$\text{dB}\mu\text{V}$
Total harmonic distortion	THD	$V_{IN} = 100\text{dB}\mu\text{V}$ , MAIN-MOD		0.5	1.5	%
Separation	SEP	$V_{IN} = 100\text{dB}\mu\text{V}$ , L output/R output	25	40		dB
Mute attenuation	MUTE	$V_{IN} = 100\text{dB}\mu\text{V}$ , L output	55	60		dB
[AM characteristics] : $f_c = 1000\text{kHz}$ , $f_m = 1\text{kHz}$ , 30%mod						
Demodulation output	$V_O$	$V_{IN} = 80\text{dB}\mu\text{V}$	30	50	70	mVrms
Signal-to-noise ratio 1	S/N1	$V_{IN} = 23\text{dB}\mu\text{V}$	15	20		dB
Signal-to-noise ratio 2	S/N2	$V_{IN} = 80\text{dB}\mu\text{V}$	47	53		dB
Total harmonic distortion	THD	$V_{IN} = 80\text{dB}\mu\text{V}$		0.5	1.5	%
IF count sensitivity	IF-C	0%mod	20	27	34	$\text{dB}\mu\text{V}$

Continued on next page.

Continued from preceding page.

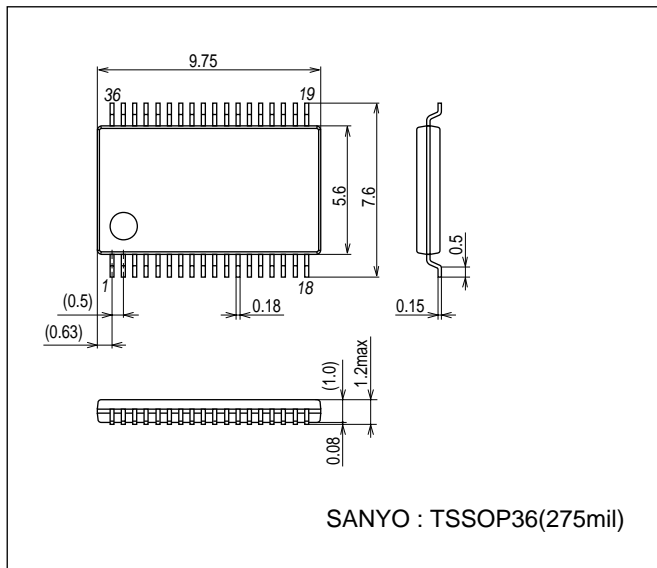
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PLL characteristics]						
Internal return resistance	Rf	XIN		8		MΩ
Built-in output resistance	Rd	XOUT		250		kΩ
Hysteresis width	VHIS	CE, CL, DI		0.1V <sub>DD</sub>		V
Output high level voltage	V <sub>OH</sub>	PD ; I <sub>O</sub> = -1mA	V <sub>DD</sub> -1.0			V
Output low level voltage	V <sub>OL1</sub>	PD ; I <sub>O</sub> = 1mA			1.0	V
	V <sub>OL2</sub>	BO1, BO2 ; I <sub>O</sub> = 1mA			0.25	V
		BO1, BO2 ; I <sub>O</sub> = 5mA			1.25	V
	V <sub>OL3</sub>	DO ; I <sub>O</sub> = 1mA			0.25	V
V <sub>OL4</sub>	AOUT ; I <sub>O</sub> = 1mA, AIN = 2.0V			0.5	V	
Input high level current	I <sub>IH1</sub>	CE, CL, DI ; V <sub>I</sub> = 6.0V			5.0	μA
	I <sub>IH2</sub>	XIN ; V <sub>I</sub> = V <sub>DD</sub>	0.16		0.9	μA
	I <sub>IH3</sub>	AIN ; V <sub>I</sub> = 6.0V			200	nA
Input low level current	I <sub>IL1</sub>	CE, CL, DI ; V <sub>I</sub> = 0V			5.0	μA
	I <sub>IL2</sub>	XIN ; V <sub>I</sub> = 0V	0.16		0.9	μA
	I <sub>IL3</sub>	AIN ; V <sub>I</sub> = 0V			200	nA
Output off-leak current	I <sub>OFF1</sub>	BO1, AOUT, BO2 ; V <sub>O</sub> = 10V			5.0	μA
	I <sub>OFF2</sub>	DO ; V <sub>O</sub> = 6.0V			5.0	μA
"H" level 3-state off-leak current	I <sub>OFFH</sub>	PD ; V <sub>O</sub> = 6.0V		0.01	200	nA
"L" level 3-state off-leak current	I <sub>OFFL</sub>	PD ; V <sub>O</sub> = 0V		0.01	200	NA

Note: For the internal return resistance, internal output resistance, hysteresis width, and output low level voltage (V<sub>OL2</sub>) described in the above PLL characteristics table, the reference value is shown.

## Package Dimensions

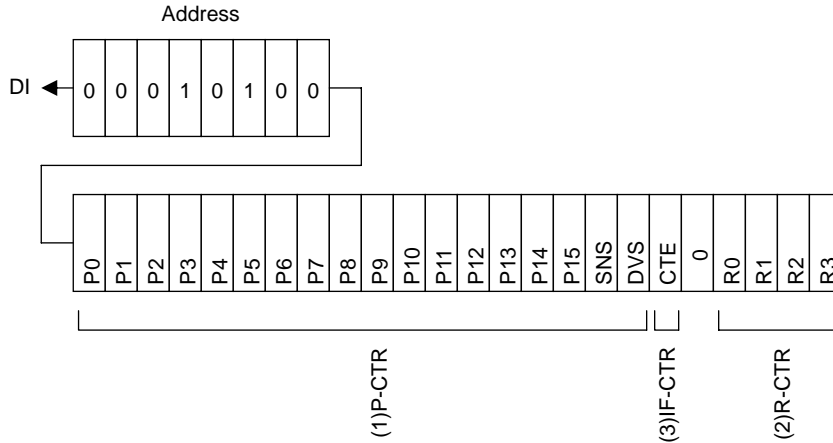
unit : mm (typ)

3247A

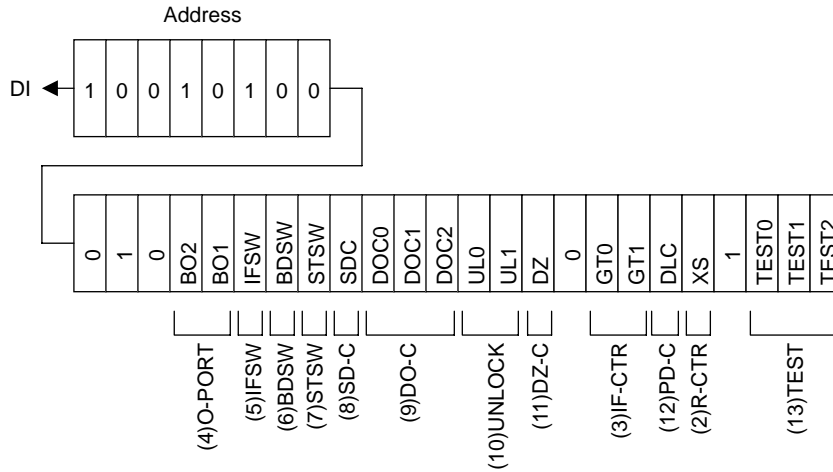


**Composition of DI control data (serial data input)**

(1) IN mode



(2) IN2 mode



**Description of DI control Data**

No.	Control block data	Description	Related data																																				
(1)	DO pin Control data  DOC0 DOC1 DOC2	<ul style="list-style-type: none"> <li>Data to set the dividing number of programmable divider Binary value with P15 assumed to be MSB. LSB varies according to DVS and SNS. (* : don't care)</li> </ul> <table border="1"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>LSB</th> <th>set dividing number (N)</th> <th>actual dividing number</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>P0</td> <td>272 to 65535</td> <td>Twice the set value</td> </tr> <tr> <td>0</td> <td>1</td> <td>P0</td> <td>272 to 65535</td> <td>Set value</td> </tr> <tr> <td>0</td> <td>0</td> <td>P4</td> <td>4 to 4095</td> <td>Set value</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>* P0 to P3 invalid when LSB : P4</li> <li>To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range. (* : don't care)</li> </ul> <table border="1"> <thead> <tr> <th>DVS</th> <th>SNS</th> <th>Input</th> <th>Operation frequency range</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>*</td> <td>FMIN</td> <td>10 to 160MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>AMIN</td> <td>2 to 40MHz</td> </tr> <tr> <td>0</td> <td>0</td> <td>AMIN</td> <td>0.5 to 10MHz</td> </tr> </tbody> </table>	DVS	SNS	LSB	set dividing number (N)	actual dividing number	1	*	P0	272 to 65535	Twice the set value	0	1	P0	272 to 65535	Set value	0	0	P4	4 to 4095	Set value	DVS	SNS	Input	Operation frequency range	1	*	FMIN	10 to 160MHz	0	1	AMIN	2 to 40MHz	0	0	AMIN	0.5 to 10MHz	
DVS	SNS	LSB	set dividing number (N)	actual dividing number																																			
1	*	P0	272 to 65535	Twice the set value																																			
0	1	P0	272 to 65535	Set value																																			
0	0	P4	4 to 4095	Set value																																			
DVS	SNS	Input	Operation frequency range																																				
1	*	FMIN	10 to 160MHz																																				
0	1	AMIN	2 to 40MHz																																				
0	0	AMIN	0.5 to 10MHz																																				

Continued on next page.

Continued from preceding page.

No.	Control block data	Description	Related data																																																																																					
(2)	Reference divider data  R0 to R3 XS	<ul style="list-style-type: none"> <li>Reference frequency (fref) selection data</li> </ul> <table border="1"> <thead> <tr> <th>R3</th> <th>R2</th> <th>R1</th> <th>R0</th> <th>Reference frequency</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25kHz</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25kHz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5kHz</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25kHz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125kHz</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125kHz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5kHz</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1kHz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3kHz</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15kHz</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT+X'tal OSC STOP</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr> </tbody> </table> <ul style="list-style-type: none"> <li>* PLL INHIBIT</li> <li>The programmable divider and IF counter stop, with FMIN, AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.</li> <li>XS must be zero.</li> </ul>	R3	R2	R1	R0	Reference frequency	0	0	0	0	25kHz	0	0	0	1	25kHz	0	0	1	0	25kHz	0	0	1	1	25kHz	0	1	0	0	12.5kHz	0	1	0	1	6.25kHz	0	1	1	0	3.125kHz	0	1	1	1	3.125kHz	1	0	0	0	5kHz	1	0	0	1	5kHz	1	0	1	0	5kHz	1	0	1	1	1kHz	1	1	0	0	3kHz	1	1	0	1	15kHz	1	1	1	0	PLL INHIBIT+X'tal OSC STOP	1	1	1	1	PLL INHIBIT	
R3	R2	R1	R0	Reference frequency																																																																																				
0	0	0	0	25kHz																																																																																				
0	0	0	1	25kHz																																																																																				
0	0	1	0	25kHz																																																																																				
0	0	1	1	25kHz																																																																																				
0	1	0	0	12.5kHz																																																																																				
0	1	0	1	6.25kHz																																																																																				
0	1	1	0	3.125kHz																																																																																				
0	1	1	1	3.125kHz																																																																																				
1	0	0	0	5kHz																																																																																				
1	0	0	1	5kHz																																																																																				
1	0	1	0	5kHz																																																																																				
1	0	1	1	1kHz																																																																																				
1	1	0	0	3kHz																																																																																				
1	1	0	1	15kHz																																																																																				
1	1	1	0	PLL INHIBIT+X'tal OSC STOP																																																																																				
1	1	1	1	PLL INHIBIT																																																																																				
(3)	IF counter control data  CTE GT0, GT1	<ul style="list-style-type: none"> <li>IF counter counting start data CTE = 1 : Counting start = 0 : Counting start</li> <li>Determines the counting time of universal counter</li> </ul> <table border="1"> <thead> <tr> <th>GT1</th> <th>GT0</th> <th>Counting time</th> <th>Wait time</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>4ms</td><td>3 to 4ms</td></tr> <tr><td>0</td><td>1</td><td>8ms</td><td>3 to 4ms</td></tr> <tr><td>1</td><td>0</td><td>16ms</td><td>3 to 4ms</td></tr> <tr><td>1</td><td>1</td><td>32ms</td><td>3 to 4ms</td></tr> </tbody> </table>	GT1	GT0	Counting time	Wait time	0	0	4ms	3 to 4ms	0	1	8ms	3 to 4ms	1	0	16ms	3 to 4ms	1	1	32ms	3 to 4ms																																																																		
GT1	GT0	Counting time	Wait time																																																																																					
0	0	4ms	3 to 4ms																																																																																					
0	1	8ms	3 to 4ms																																																																																					
1	0	16ms	3 to 4ms																																																																																					
1	1	32ms	3 to 4ms																																																																																					
(4)	Output port data  $\overline{BO1}$ , $\overline{BO2}$	<ul style="list-style-type: none"> <li>Data to determine output of output ports <math>\overline{BO1}</math> and <math>\overline{BO2}</math> "Data" = 0 : OPEN 1 : Low</li> </ul>																																																																																						
(5)	MUTE control data  IFSW	<ul style="list-style-type: none"> <li>Data to determine the output of output port IFSW, controlling the MUTE function. "Data" = 0 : at receiving 1 : MUTE</li> </ul>																																																																																						
(6)	FM/AM BAND selection control data BDSW	<ul style="list-style-type: none"> <li>Data to determine the output of output port BDSW, controlling selection of BAND. "Data" = 0 : AM 1 : FM</li> </ul>																																																																																						
(7)	Forced monaural control data  STSW	<ul style="list-style-type: none"> <li>Data to determine the output of output port STSW, controlling the forced stereo functions. "Data" = 0 : MONO 1 : STEREO</li> </ul>																																																																																						
(8)	SD sensitivity control data  SDC	<ul style="list-style-type: none"> <li>Data to determine the output of output port SDC, controlling the FM-SD sensitivity (at IF input).</li> <li>* Setting SDC=1 is recommended.</li> <li>In case of SDC=0, Add resistance 47kΩ between 28 pin (SD) and GND.</li> <li>FM-SD sensitivity (typ) at following SDC=0 is the values when 47KΩ is added.</li> </ul> <table border="1"> <thead> <tr> <th>SDC</th> <th>FM-SD sensitivity</th> </tr> </thead> <tbody> <tr><td>0*</td><td>42dBμV</td></tr> <tr><td>1</td><td>48dBμV</td></tr> </tbody> </table>	SDC	FM-SD sensitivity	0*	42dBμV	1	48dBμV																																																																																
SDC	FM-SD sensitivity																																																																																							
0*	42dBμV																																																																																							
1	48dBμV																																																																																							

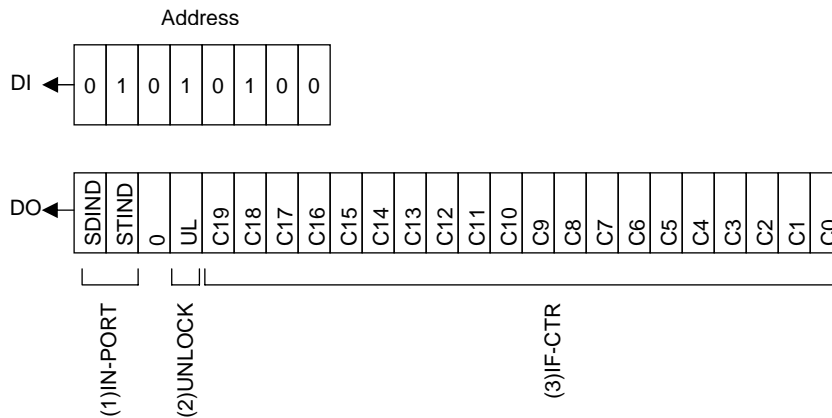
Continued on next page.

Continued from preceding page.

No.	Control block data	Description	Related data																																				
(9)	DO pin control data  DOC0 DOC1 DOC2	<ul style="list-style-type: none"> <li>Data to determine the output of the DO pin.</li> </ul> <table border="1"> <thead> <tr> <th>DOC2</th> <th>DOC1</th> <th>DOC0</th> <th>DO pin condition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Low when unlock is detected.</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>end-UC (See the item with asterisk below)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Open</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>Open</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Low when stereo</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>Low when SDON</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Open</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>The open condition is selected at power ON/reset.</li> <li>* IF counter counting end check</li> </ul> <p>① Counting start      ② Counting end      ③ CE : Hi</p> <p>① With end-UC set and IF counter starting (CTE = 0→1), DO pin opens automatically.          ② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made.          ③ DO pin opens when serial data is entered/output (CE pin : Hi)          Note : DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE : Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).</p>	DOC2	DOC1	DOC0	DO pin condition	0	0	0	Open	0	0	1	Low when unlock is detected.	0	1	0	end-UC (See the item with asterisk below)	0	1	1	Open	1	0	0	Open	1	0	1	Low when stereo	1	1	0	Low when SDON	1	1	1	Open	UL0, UL1 CTE
DOC2	DOC1	DOC0	DO pin condition																																				
0	0	0	Open																																				
0	0	1	Low when unlock is detected.																																				
0	1	0	end-UC (See the item with asterisk below)																																				
0	1	1	Open																																				
1	0	0	Open																																				
1	0	1	Low when stereo																																				
1	1	0	Low when SDON																																				
1	1	1	Open																																				
(10)	Unlock detection data  UL0, UL1	<ul style="list-style-type: none"> <li>Phase error (<math>\phi E</math>) detection width selection data to judge if PLL is locked.</li> <li>Phase error exceeding the detection width is judged that PLL is locked (* : don't care)</li> </ul> <table border="1"> <thead> <tr> <th>UL1</th> <th>UL0</th> <th><math>\phi E</math> Detection width</th> <th>Detection output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Stop</td> <td>Open</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Direct output of <math>\phi E</math></td> </tr> <tr> <td>1</td> <td>*</td> <td><math>\pm 6.67 \mu s</math></td> <td><math>\phi E</math> extended by 1 to 2 ms</td> </tr> </tbody> </table> <p>* DO pin is LOW. Serial data output : UL = 0.</p>	UL1	UL0	$\phi E$ Detection width	Detection output	0	0	Stop	Open	0	1	0	Direct output of $\phi E$	1	*	$\pm 6.67 \mu s$	$\phi E$ extended by 1 to 2 ms	DOC0 DOC1 DOC2																				
UL1	UL0	$\phi E$ Detection width	Detection output																																				
0	0	Stop	Open																																				
0	1	0	Direct output of $\phi E$																																				
1	*	$\pm 6.67 \mu s$	$\phi E$ extended by 1 to 2 ms																																				
(11)	Phase comparator control data  DZ	<ul style="list-style-type: none"> <li>Data to control the dead zone of phase comparator</li> </ul> <table border="1"> <thead> <tr> <th>DZ</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>DZA</td> </tr> <tr> <td>1</td> <td>DZB</td> </tr> </tbody> </table> <p>Dead zone width : DZA&lt;DZB</p>	DZ	Charge pump output	0	DZA	1	DZB																															
DZ	Charge pump output																																						
0	DZA																																						
1	DZB																																						
(12)	Charge pump control data  DLC	<ul style="list-style-type: none"> <li>Data to enforce control of charge pump output</li> </ul> <table border="1"> <thead> <tr> <th>DLC</th> <th>Charge pump output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal</td> </tr> <tr> <td>1</td> <td>Forced to LOW</td> </tr> </tbody> </table> <p>In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to V<sub>CC</sub>. (Dead lock clear circuit)</p>	DLC	Charge pump output	0	Normal	1	Forced to LOW																															
DLC	Charge pump output																																						
0	Normal																																						
1	Forced to LOW																																						
(13)	LSI test data  TEST0 to 2	<ul style="list-style-type: none"> <li>LSI test data</li> </ul> <p>TEST0 }          TEST1 } All to be set to "0"          TEST2 }</p> <p>All set to zero at power ON/reset</p>																																					

## DO control data (serial data output) composition

## (1) OUT mode

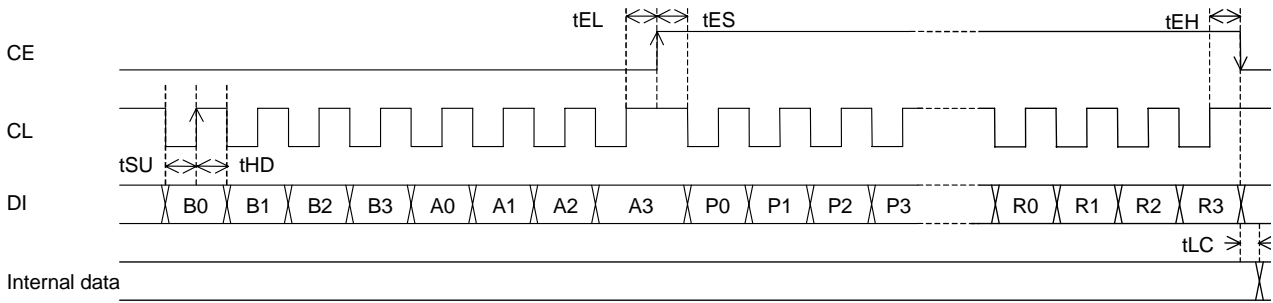


## Description of DO output data

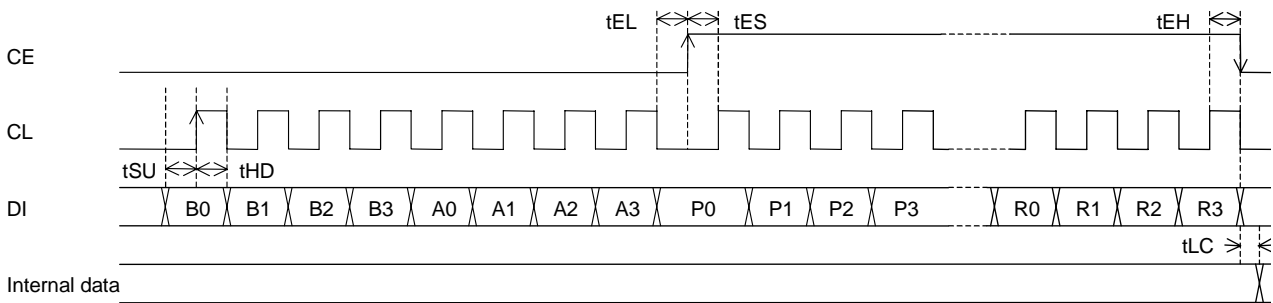
No.	Control block data	Description	Related data
(1)	SD and Stereo indicators control data  STIND, SDIND	<ul style="list-style-type: none"> <li>Data latching SD and stereo indicator conditions. Latching made in the data output (OUT) mode. SDIND←SD indicator condition    0 : SD ON, 1 : SD OFF STIND←Stereo indicator condition    0 : ST ON, 1 : ST OFF</li> </ul>	
(2)	PLL unlock data  UL	<ul style="list-style-type: none"> <li>Data latching the content of unlock detection circuit UL←0 : At unlock 1 : At lock or detection stop mode</li> </ul>	UL0 UL1
(3)	IF counter, binary counter  C19 to C0	<ul style="list-style-type: none"> <li>Data latching the content of IF counter (20-bit binary counter) C19←MSB of binary counter C0 ←MSB of binary counter</li> </ul>	CTE GT0 GT1

**Serial data input (IN1/IN2)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH} \geq 0.75\mu s$   $t_{LC} < 0.75\mu s$**

CL : Normally Hi

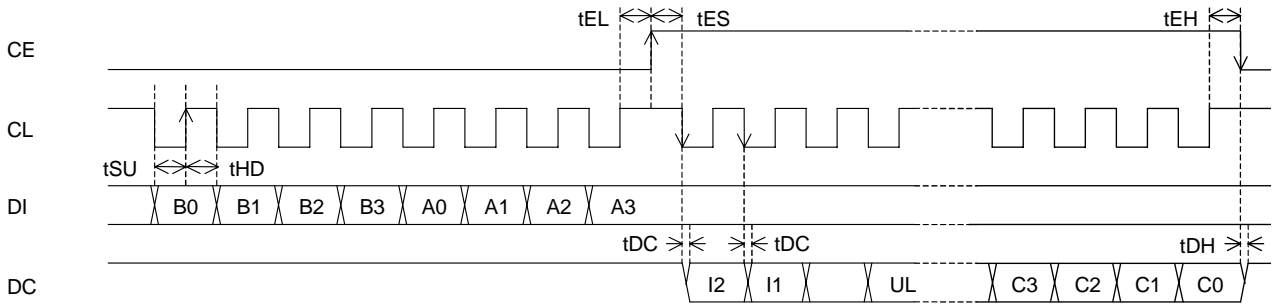


CL : Normally Low

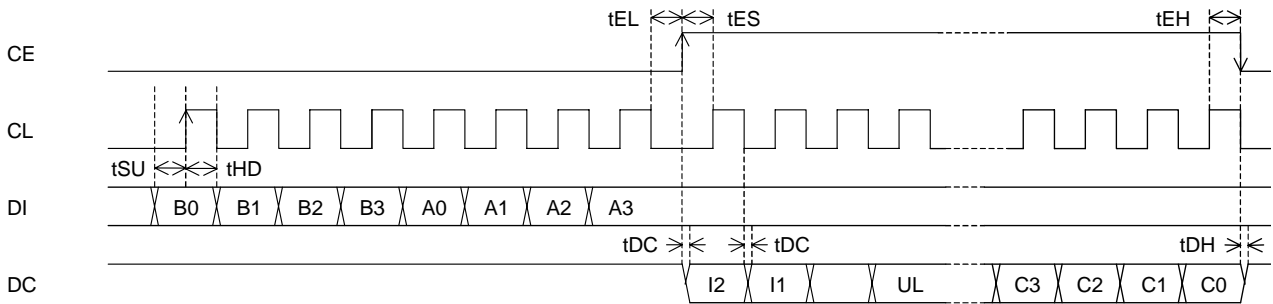


**Serial data output (OUT)  $t_{SU}$ ,  $t_{HD}$ ,  $t_{EL}$ ,  $t_{ES}$ ,  $t_{EH} \geq 0.75\mu s$   $t_{DC}$ ,  $t_{DH} < 0.35\mu s$**

CL : Normally Hi

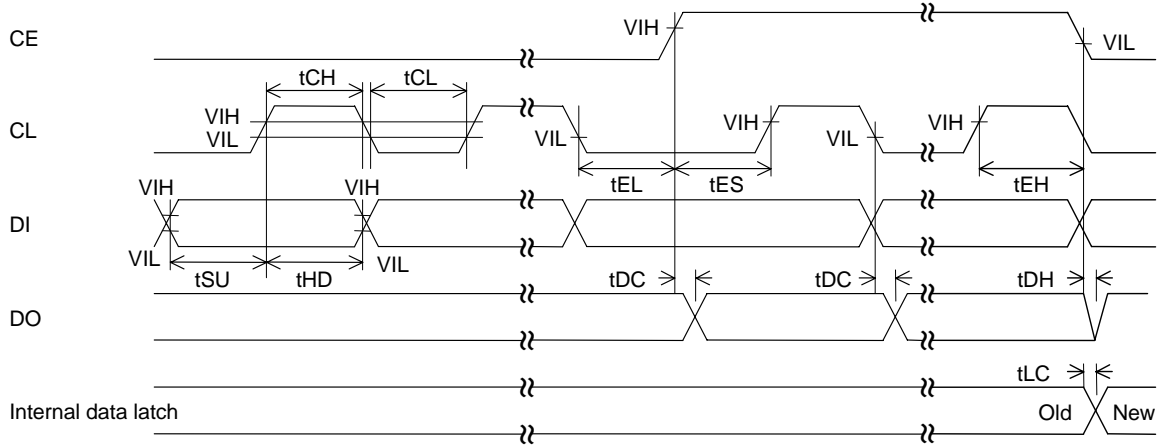


CL : Normally Hi

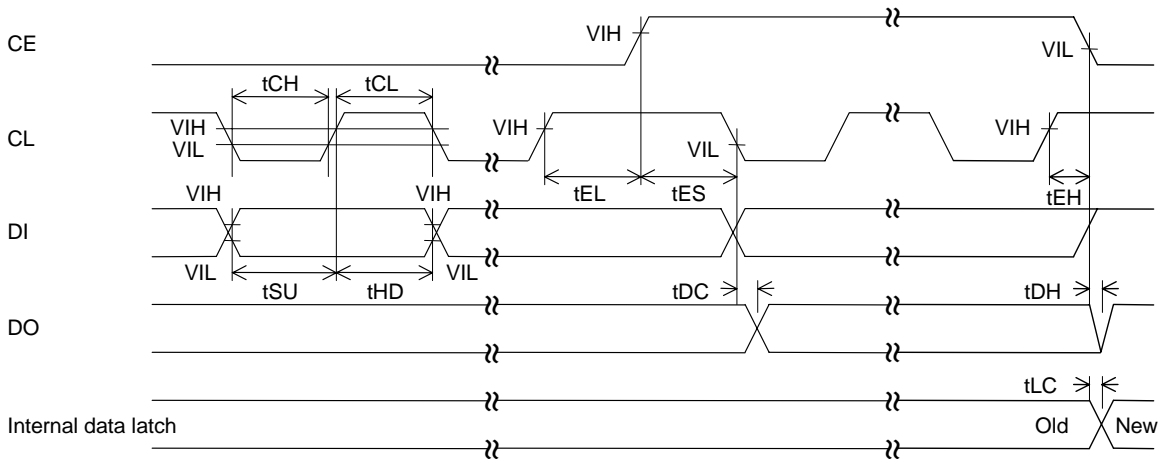


(Note) DO pin is an Nch open drain pin, so that the data varying time ( $t_{DC}$  and  $t_{DH}$ ) differs depending on the pull-up resistance and substrate capacity.

**Serial data timing**



<< When CL stops at the "L" level >>



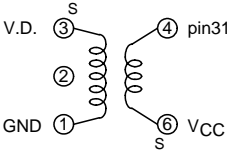
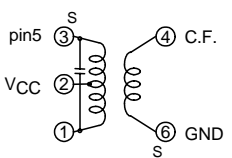
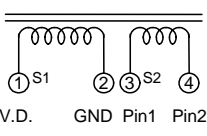
<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI, CL		0.75			μs
Data hold time	tHD	DI, CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE, CL		0.75			μs
CE setup time	tES	CE, CL		0.75			μs
CE hold time	tEH	CE, CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO, CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO, CE					





## Coil specifications (bottom view)

• FM-BPF : GFWB3 (Soshin) 76MHz to 108MHz	
• FM-RF : SA-149 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 4.5T	
• FM-OSC : SA-151 (Sumida) 3.6mm diameter, air core, 0.6mm wire, 3.5T	
• FM-IF Filter : SFELA10M7GA00 (Murata)	
• FM-Discriminator : CDALA10M7GA121 (Murata)	
• AM-OSC : SA-181 (Sumida)	
	6-4 37T 3-1 74T 0.06UEW $f_o = 796\text{kHz}$ $Q_o \geq 80$ $L = 140\mu\text{H}$
• AM-MIX : SA-164 (Sumida)	
	1-2 122T 4-6 9T 2-3 62T 0.06UEW $f_o = 450\text{kHz}$ , $Q_o \geq 65$ $C = 180\text{pF}$
• AM-IF Filter : SFULA450KU2B (Murata)	
• MW Bar-antenna : C8E-A0105 (Toko)	
	1-2 67T 3-4 9T $f_o = 796\text{kHz}$ $Q_o = 180\text{min}$ $L = 260\mu\text{H}$
• Crystal oscillator : CFV-206 (Citizen)	

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of April, 2008. Specifications and information herein are subject to change without notice.