VITESSE

VSP947/VSP948

High Performance Pentium™ Processor Cache Controller for Multiprocessor Systems

FEATURES

- Optimizes Pentium™ and P54C/CM Multiprocessor Performance
- Zero Wait States — 1-1-1-1 Pipelined Bursting or 2-1-1-1 Non-Pipelined Bursting Read & Write Cycles
- Zero Wait State Snoop
- 66-MHz Operation with Migration Path to 80-MHz
- Cache Sizes: 512 KB, 1 MB, 2 MB, 4 MB, and 8 MB
- Asynchronous SRAMs for Tag Entries
- Direct-Mapped or Two-Way Set Associative
- Copy Back to Reduce Bus Traffic
- Byte Gathering to Reduce System Bus Traffic
- 8-Deep Write Back Buffer to Reduce Penalty for Cache Misses
- Write Allocation to Increase Cache Hit Rate
- MESI Protocol for Data Consistency
- Cache to Cache Transfers
- TTL or GTL I/O Signal Levels
- Low Power/High Integration Solution
- Incorporates JTAG and Logic to Test Tag SRAM

FUNCTIONAL DESCRIPTION

Vitesse's VSP947/948 is a high performance serial cache controller chipset specifically designed for use in multiprocessor systems based on the Intel Pentium™ CPU or P54C/P54CM CPUs. The complete chipset provides all of the control functions necessary to implement a second-level, direct-mapped or two-way set associative, copy-back cache sub-system up to 8MByte in size.

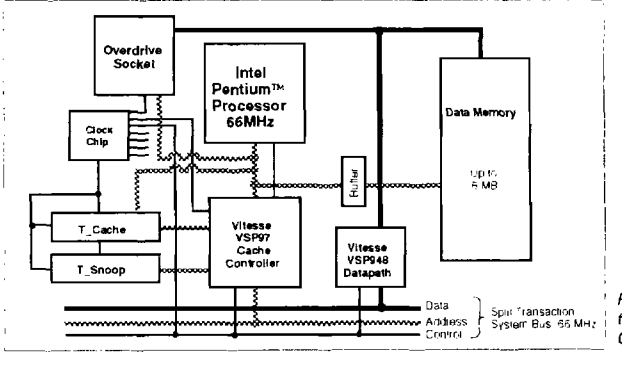
The high speed VSP947 permits the system designer to use standard asynchronous SRAMs for tag entries and standard burst SRAM for data storage, while allowing the microprocessors to run at full speed (zero-wait-states).

An 8-deep write back buffer supports zero-wait-state operation on the write-miss cycle as well as supporting concurrent copy-back & write allocation.

The system bus, V-bus, is a split transaction bus with up to 66 MHz performance. The bus provides 500 MB/s sustained data throughput.

The VSP947/948 provides the highest system performance and greatest scalability at the lowest cost. For 66 MHz multiprocessor systems, the VSP947/948 cache controller is the best solution. Planned upgrades will offer the same solution for systems operating at 80-MHz and beyond.

1-MByte Cache Simplified System Diagram (66-MHz)



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