

## N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

### Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

### QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Total power dissipation up to $T_{amb} = 25^\circ C$	$P_{tot}$	max.	1 W
Drain-source ON-resistance $I_D = 250 \text{ mA}; V_{GS} = 10 \text{ V}$	$R_{DSon}$	typ.	6 $\Omega$
		max.	12 $\Omega$
Transfer admittance $I_D = 250 \text{ mA}; V_{DS} = 15 \text{ V}$	$ y_{fs} $	typ.	250 mS

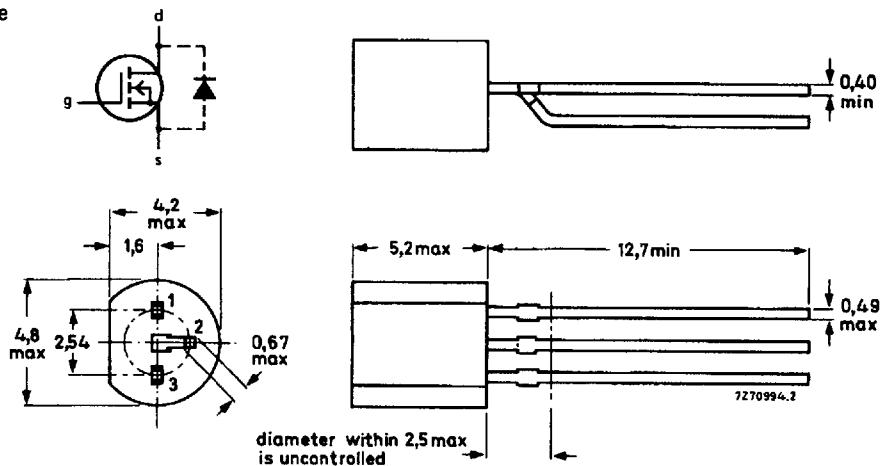
### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

#### Pinning:

- 1 = source  
2 = gate  
3 = drain



Note: Various pinout configurations available.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$I_D$	max.	250 mA
Drain current (peak)	$I_{DM}$	max.	800 mA
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (note 1)	$P_{tot}$	max.	1 W
Storage temperature range	$T_{stg}$		-65 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

**THERMAL RESISTANCE**

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125 K/W
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**CHARACTERISTICS**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current $V_{DS} = 160\text{ V}; V_{GS} = 0$	$I_{DSS}$	max.	10 $\mu\text{A}$
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0$	$I_{GSS}$	max.	100 nA
Gate threshold voltage $I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig. 4) $I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	$R_{DSon}$	typ. max.	6 $\Omega$ 12 $\Omega$
Transfer admittance $I_D = 250\text{ mA}; V_{DS} = 15\text{ V}$	$ y_{fs} $	typ.	250 mS
Input capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{iss}$	typ. max.	70 pF 90 pF
Output capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{oss}$	typ. max.	20 pF 30 pF
Feedback capacitance at $f = 1\text{ MHz}$ $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rss}$	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $I_D = 250\text{ mA}; V_{DD} = 50\text{ V}; V_{GS} = 0\text{ to }10\text{ V}$	$t_{on}$	typ. max.	4 ns 10 ns
	$t_{off}$	typ. max.	15 ns 25 ns

**Note**

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

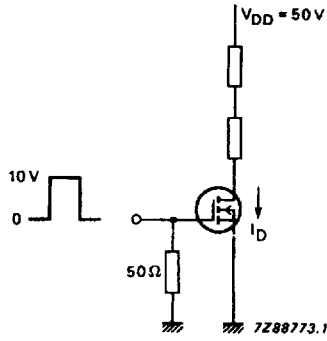


Fig. 2 Switching times test circuit.

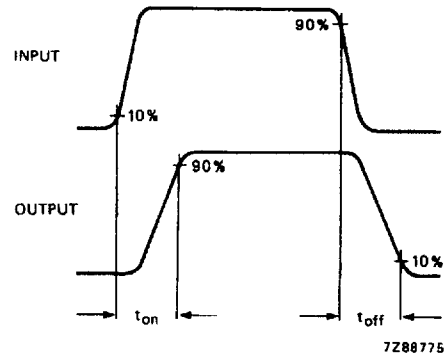


Fig. 3 Input and output waveforms.

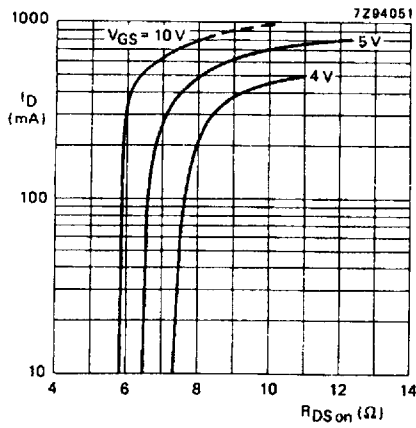


Fig. 4  $T_j = 25^\circ\text{C}$ ; typical values.

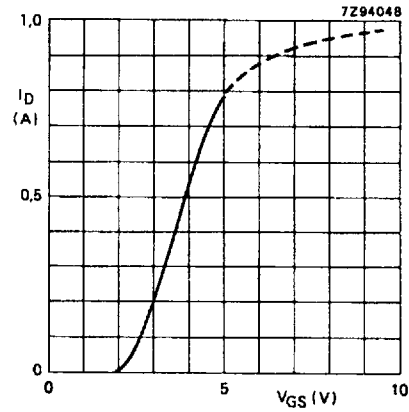


Fig. 5  $T_j = 25^\circ\text{C}$ ;  $V_{DS} = 10\text{ V}$ ; typical values.

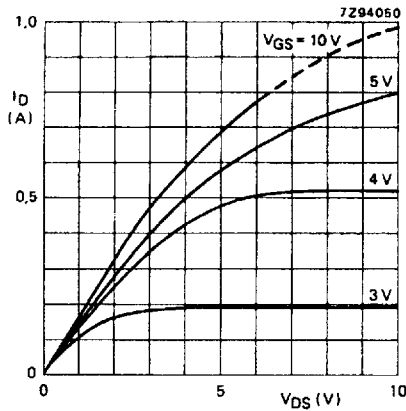


Fig. 6  $T_j = 25^\circ\text{C}$ ; typical values.

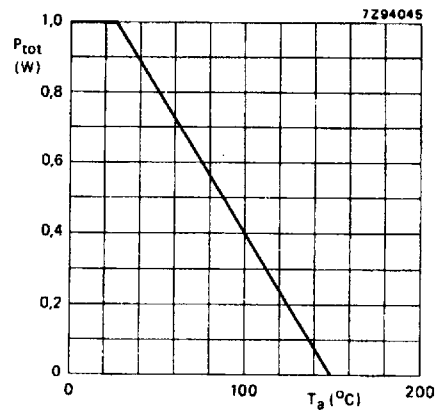


Fig. 7 Power derating curve.

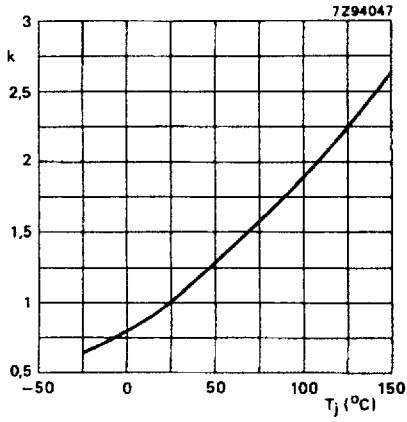


Fig. 8  $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^\circ C}}$ ; at 400 mA/10 V; typical values.

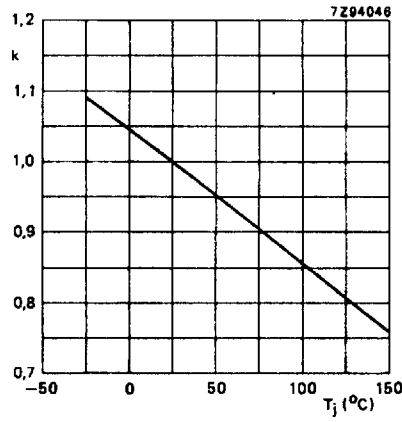


Fig. 9  $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^\circ C}}$ ;  $V_{GS(th)}$  at 1 mA; typical values.

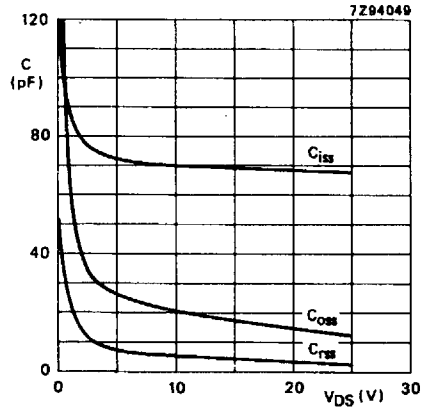


Fig. 10  $T_j = 25\ ^\circ C$ ;  $V_{GS} = 0$ ;  $f = 1\ MHz$ ; typical values.