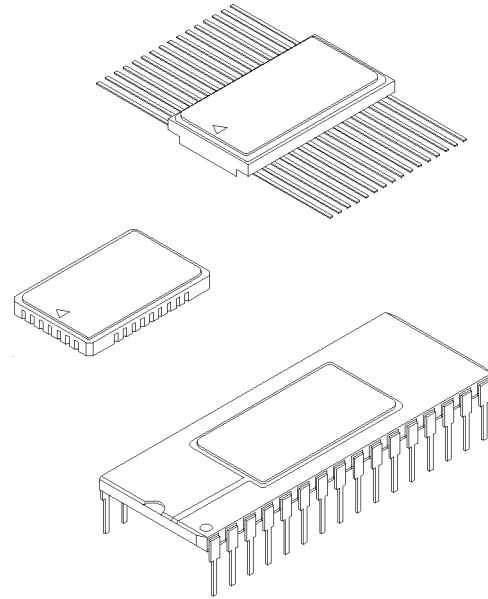


**DESCRIPTION:**

The DPS128M8F/G/N is a monolithic 128K X 8 Static Random Access Memory (SRAM) fabricated using CMOS technology. It is designed for use in high density, high speed, low power applications. All pins are TTL compatible and a single +5 Volt power supply is required.

The DPS128M8F/G/N has extremely low standby power dissipation making it suitable for battery backup.

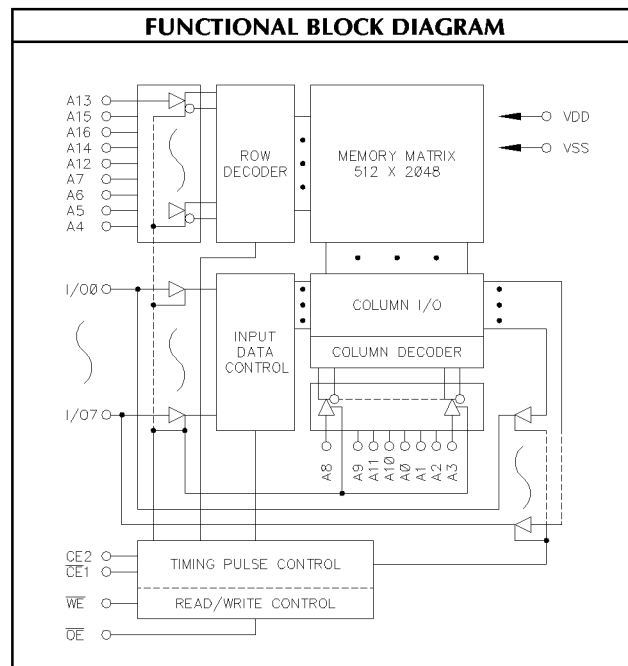
The 600-mil wide, 32-pin ceramic, Dual-In-Line Package (DIP), conforms to the JEDEC standard. Dense-Pac also offers a 32-pin ceramic FLATPACK and a 32-Pin Ceramic Leadless Chip Carrier (LCC).

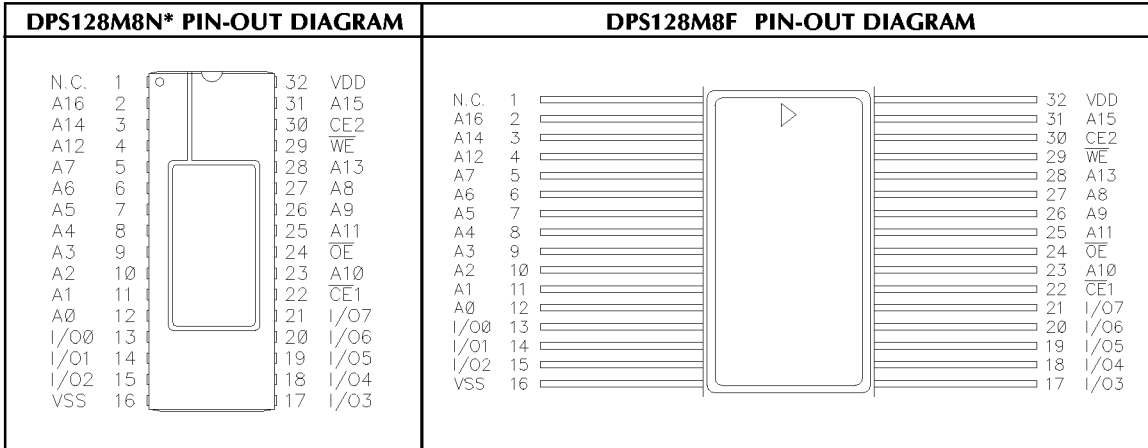


**FEATURES:**

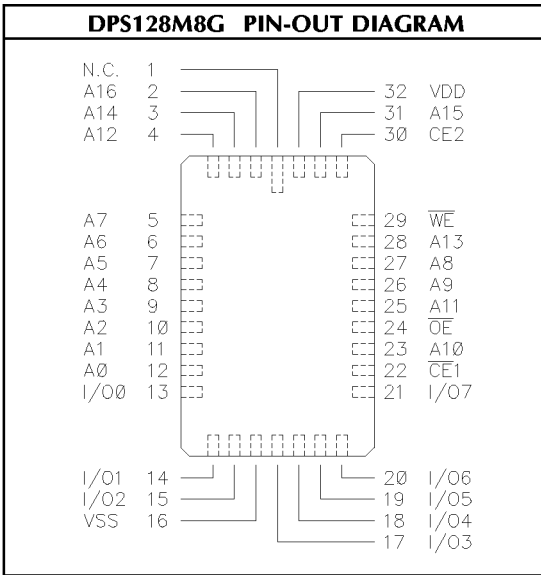
- 131,072 by 8-Bits Organization
- Access Times: 70, 85, 100, 120, 150ns (max.)
- Low Power: 10 $\mu$ W (typ.) Standby  
225mW (typ.) Operating
- Fully Static Operation;  
No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply,  $\pm$ 10% Tolerance
- Two Chip Enables
- Output Enable Functions
- Faster Access Speeds Available Upon Request
- Package Types:  
32-Pin Ceramic Side Brazed DIP  
32-Pin Ceramic FLATPACK  
32-Pin Ceramic LCC

PIN NAMES	
A0-A16	Address Inputs
I/O0-I/O7	Data In/Out
$\overline{CE}1$	Low Chip Enable
CE2	High Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V <sub>DD</sub>	Power (+5V)
V <sub>SS</sub>	Ground
N.C.	No Connect





\* Cerdip also available with one Chip Enable (DPS128M8NS). Pin 30 on this version is a no connect (N.C.) consult factory.



TRUTH TABLE						
Mode	CE1	CE2	OE	WE	I/O Pin	Supply Current
Not Selected	H	X	X	X	HIGH-Z	Standby
Not Selected	X	L	X	X	HIGH-Z	Standby
DOUT Disable	L	H	H	H	HIGH-Z	Active
Read	L	H	L	H	DOUT	Active
Write	L	H	X	K	DIN	Active

H = HIGH      L = LOW      X = Don't Care

CAPACITANCE <sup>4</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C <sub>ADR</sub>	Address Input	8	pF	V <sub>IN</sub> <sup>2</sup> = 0V
C <sub>CE</sub>	Chip Enable	8		
C <sub>CE2</sub>	Active High Chip Select	8		
C <sub>WE</sub>	Write Enable	8		
C <sub>OE</sub>	Output Enable	8		
C <sub>I/O</sub>	Data Input/Output	10		

ABSOLUTE MAXIMUM RATINGS <sup>3</sup>			
Symbol	Parameter	Value	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.5 to +7.0	°C
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to V <sub>DD</sub> +0.5	V

RECOMMENDED OPERATING RANGE <sup>3</sup>						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	Input HIGH Voltage	2.2		V <sub>DD</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage	-0.5 <sup>2</sup>		0.8	V	
T <sub>A</sub>	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-	-4	+4	-4	+4	-4	+4	μA
I <sub>OUT</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>DD</sub> , CE1 or OE = V <sub>IH</sub> , or WE = V <sub>IL</sub>	-	-2	+2	-2	+2	-2	+2	μA
I <sub>CC1</sub>	Active Supply Current	CE1 = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 0mA	15		40		50		55	mA
I <sub>CC2</sub>	Operating Supply Current	Cycle=min., Duty=100% I <sub>OUT</sub> = 0mA	45		75		50		85	mA
I <sub>SB1</sub>	Full Standby Supply Current (CMOS)	CE1 ≥ V <sub>DD</sub> -0.2V, CE2 ≥ V <sub>DD</sub> -0.2V or CE2 ≤ 0.2V	4		200		400		1000	μA
I <sub>SB2</sub>	Standby Current (TTL)	CE1 = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2		6		6		6	mA
I <sub>DR3</sub>	Data Retention Supply Current (3.0V)	V <sub>DR</sub> = 3.0V, CE1 ≥ V <sub>DR</sub> -0.2V, CE2 ≥ V <sub>DR</sub> -0.2V or CE2 ≤ 0.2V	2		100		200		800	μA
I <sub>DR2</sub>	Data Retention Supply Current (2.0V)	V <sub>DR</sub> = 2.0V, CE1 ≥ V <sub>DR</sub> -0.2V, CE2 ≥ V <sub>DR</sub> -0.2V or CE2 ≤ 0.2V	2		90		170		700	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 2.1mA	-		0.4		0.4		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -1.0mA	-	2.4		2.4		2.4		V

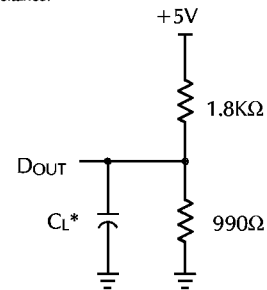
† Typical measurements made at +25°C, Cycle = min., V<sub>DD</sub> = 5.0V.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

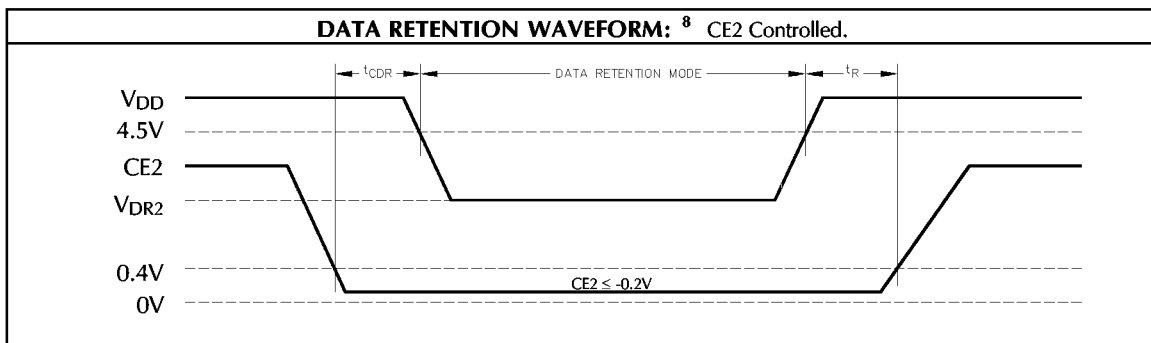
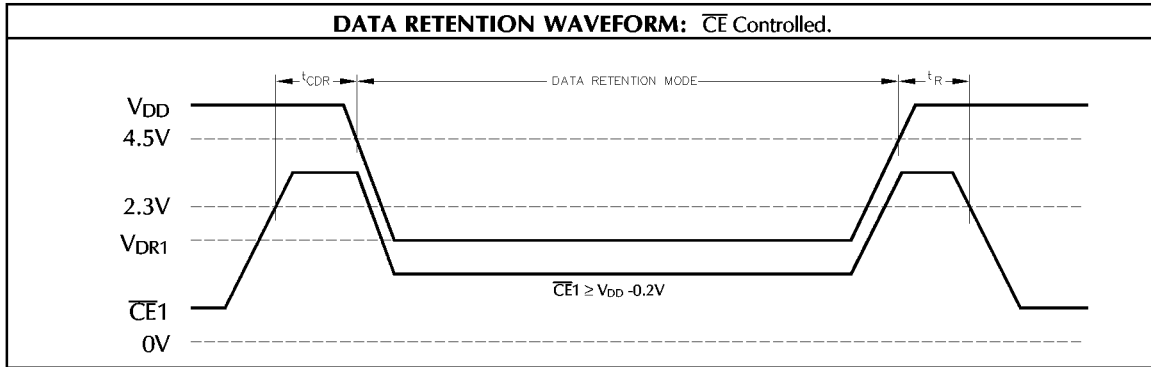
OUTPUT LOAD		
Load	C <sub>L</sub>	Parameters Measured
1	100pF	except t <sub>LZ1</sub> , t <sub>LZ2</sub> , t <sub>HZ1</sub> , t <sub>HZ2</sub> , t <sub>OHZ</sub> , t <sub>OLZ</sub> , and t <sub>WHZ</sub>
2	5pF	t <sub>LZ1</sub> , t <sub>LZ2</sub> , t <sub>HZ1</sub> , t <sub>HZ2</sub> , t <sub>OHZ</sub> , t <sub>OLZ</sub> , and t <sub>WHZ</sub>

Figure 1. Output Load

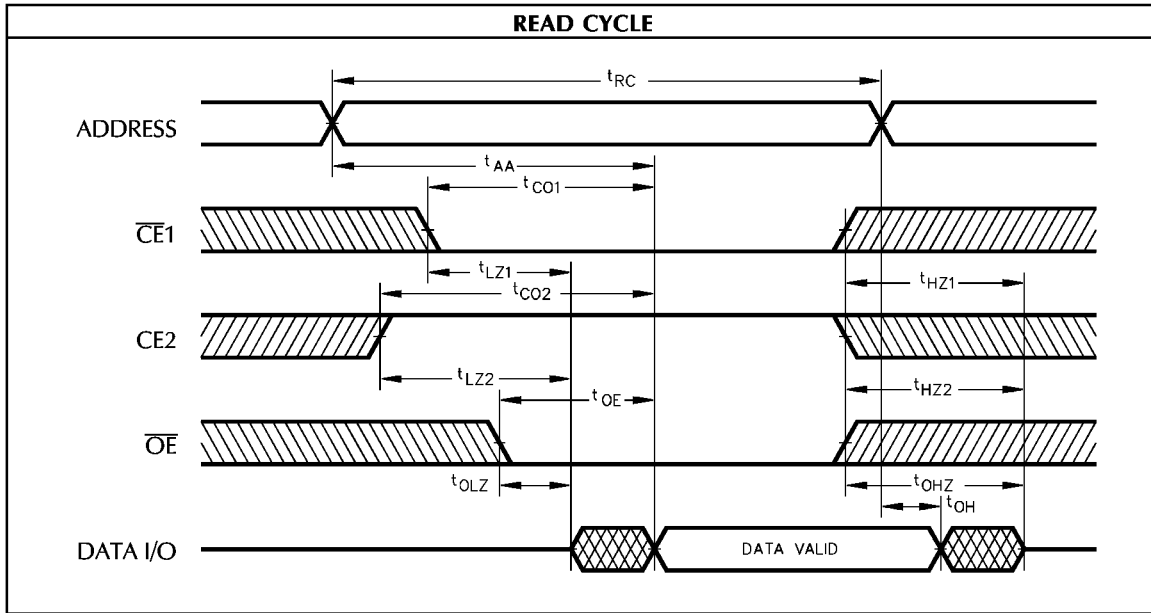
\* Including Probe and Jig Capacitance.



Data Retention AC Characteristics <sup>8</sup>						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	CE1 ≥ V <sub>DR</sub> -0.2V, CE2 ≥ V <sub>DR</sub> -0.2V or CE2 ≤ V <sub>DR</sub> 0.2V	2.0	-	-	V
V <sub>CDR</sub>	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t <sub>R</sub>	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

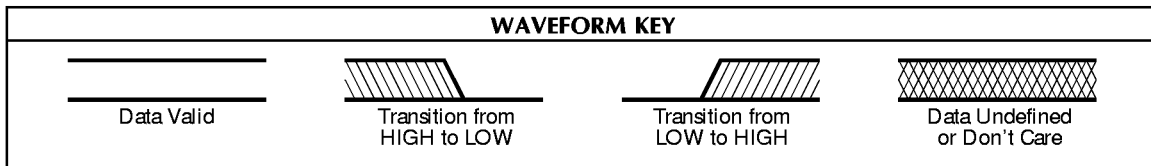


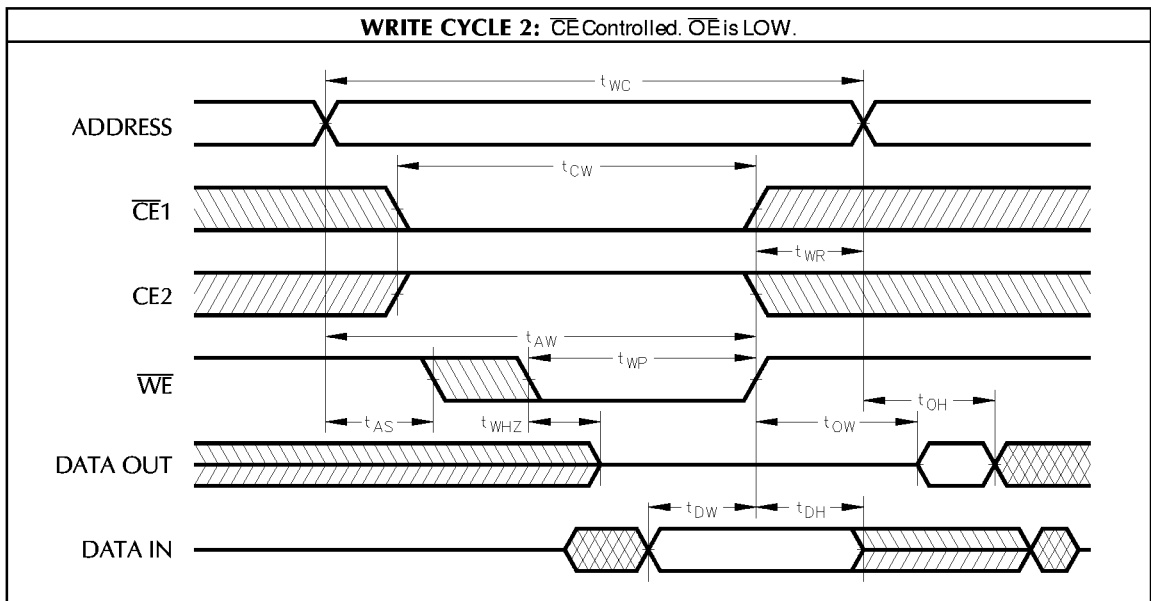
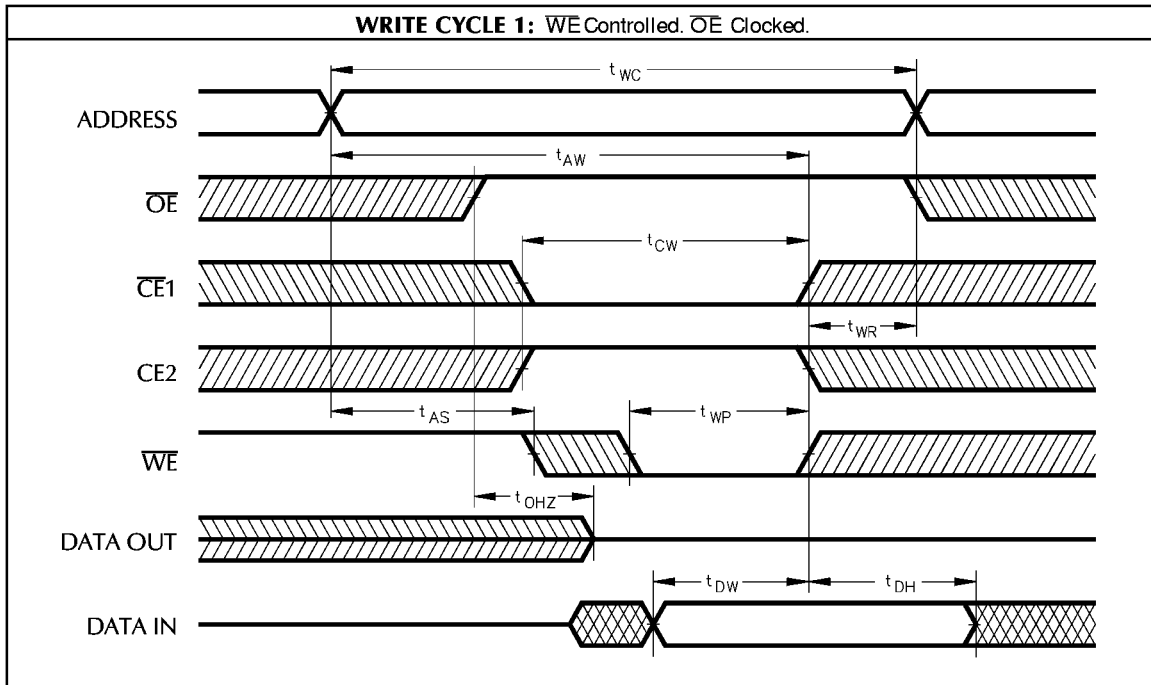
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	70ns		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	$t_{RC}$	Read Cycle Time	70		85		100		120		150		ns
2	$t_{AA}$	Address Access Time		70		85		100		120		150	ns
3	$t_{CO1}$	$\overline{CE1}$ to Output Valid		70		85		100		120		150	ns
4	$t_{CO2}$	CE2 to Output Valid		70		85		100		120		150	ns
5	$t_{OE}$	Output Enable to Output Valid		40		45		50		60		70	ns
6	$t_{LZ1}$	$\overline{CE1}$ to Output in LOW-Z <sup>4,5</sup>	5		5		10		10		10		ns
7	$t_{LZ2}$	CE2 to Output in LOW-Z <sup>4,5</sup>	5		5		10		10		10		ns
8	$t_{OLZ}$	Output Enable to Output in LOW-Z <sup>4,5</sup>	0		0		0		0		0		ns
9	$t_{HZ1}$	$\overline{CE1}$ to Output in HIGH-Z <sup>4,5</sup>		30		30		35		45		50	ns
10	$t_{HZ2}$	CE2 to Output in HIGH-Z <sup>4,5</sup>		30		30		35		45		50	ns
11	$t_{OHZ}$	Output Enable to Output in HIGH-Z <sup>4,5</sup>		30		30		35		45		50	ns
12	$t_{OH}$	Output Hold from Address Change	10		10		10		10		10		ns



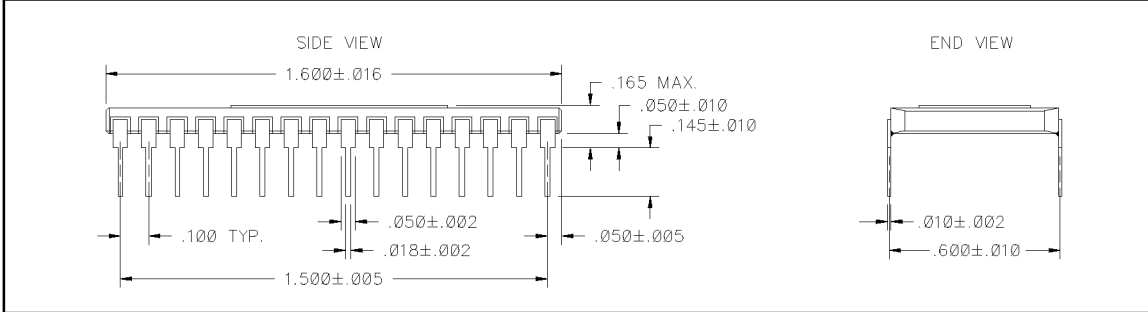
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE <sup>6, 7</sup> : Over operating ranges													
No.	Symbol	Parameter	70ns		85ns		100ns		120ns		150ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	$t_{WC}$	Write Cycle Time	70		85		100		120		150		ns
14	$t_{AW}$	Address Valid to End of Write	65		75		90		100		120		ns
15	$t_{CW}$	Chip Enable to End of Write	65		75		90		100		120		ns
16	$t_{AS}$	Address Set-Up Time *	0		0		0		0		0		ns
17	$t_{WP}$	Write Pulse Width <sup>10</sup>	55		65		75		85		90		ns
18	$t_{WR}$	Write Recovery Time <sup>11</sup>	10		10		10		15		15		ns
19	$t_{WHZ}$	Write Enable to Output in HIGH-Z <sup>4, 5</sup>		30		30		35		40		45	ns
20	$t_{DW}$	Data to Write Time Overlap	35		35		40		50		60		ns
21	$t_{DH}$	Data Hold from Write Time	0		0		0		0		0		ns
22	$t_{OW}$	Output Active from End of Write	5		5		5		5		5		ns

\* Valid for both Read and Write Cycles.

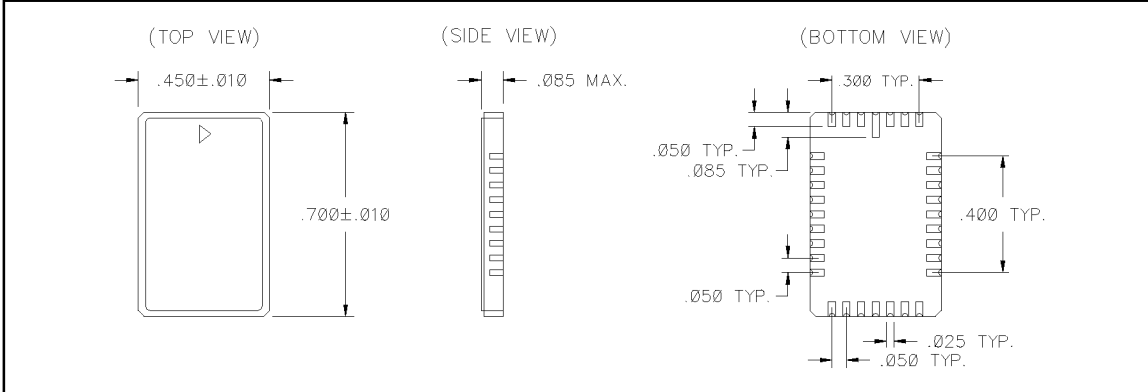




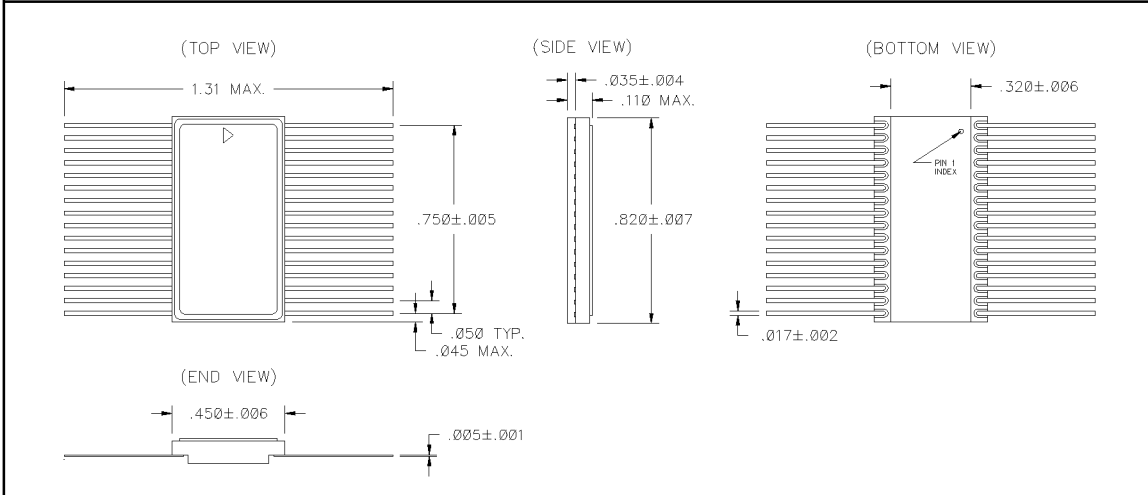
**CERAMIC DIP MECHANICAL DIAGRAM**

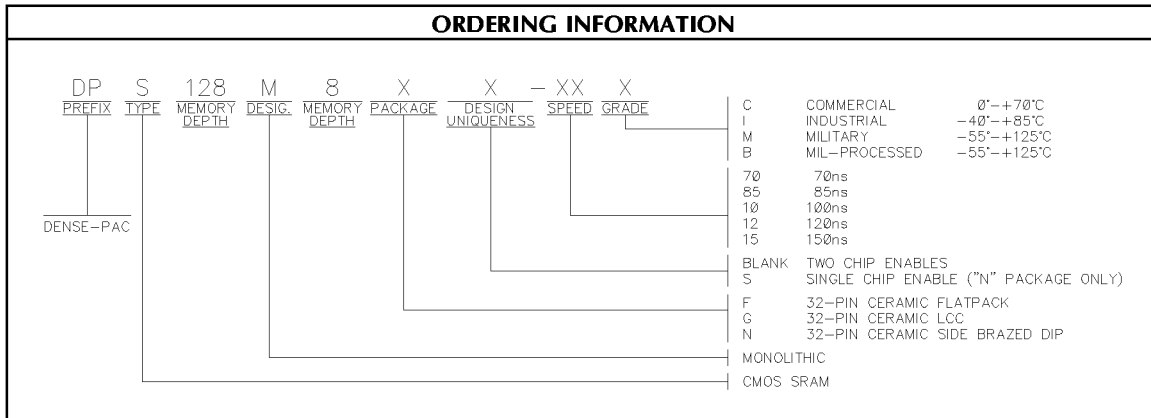


**CERAMIC LCC MECHANICAL DIAGRAM**



**CERAMIC FLATPACK MECHANICAL DIAGRAM**





NOTES:

1. All voltages are with respect to  $V_{SS}$
2. -2.0V min. for pulse width less than 20ns ( $V_{IL}$  min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of  $\pm 500$ mV from steady state voltage.
6. When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when  $\overline{WE}$  is LOW.
8.  $CE2$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{CE1}$  buffer and  $\overline{OE}$  buffer and  $D_{IN}$  buffer. If  $CE2$  controls Data Retention Mode,  $V_{IN}$  levels (Address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $\overline{CE1}$ , I/O) can be in the high impedance state. If  $\overline{CE1}$  controls Data Retention Mode,  $CE2$  must be  $CE2 \geq V_{DD} - 0.2V$  or  $0V \leq CE2 \leq 0.2V$ . The other input levels (Address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the High Impedance State.

**Dense-Pac Microsystems, Inc.**

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 (714) 898-0007 (800) 642-4477 (Outside CA) ♦ FAX: (714) 897-1772 ♦ <http://www.dense-pac.com>