Clock signal generator circuit for digital TV systems (SCGC)

SAA7157

Supercedes data of April 1991

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5A, LL1.5B, LL3A and LL3B (4th and 2nd multiples of input frequency)
- PLL mode or VCO mode selectable
- Reset control and power fail detection
- Suitable for applications with feature box and picture memory

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I_{DDA}	analog supply current	3	-	9	mA
I_{DDD}	digital supply current	10	-	60	mA
V_{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V_{DDA}	V
f_i	input frequency range	6.0	-	7.25	MHz
V_I	input voltage LOW input voltage HIGH	0 2.0	- -	0.8 V_{DDD}	V V
V_O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V_{DDD}	V V
T_{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family and the SAA7199B (DENC). The circuit operates in either the phase-locked loop mode (PLL) or voltage controlled oscillator mode (VCO).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7157	20	DIL	plastic	SOT146
SAA7157T	20	mini-pack (SO20)	plastic	SOT163A

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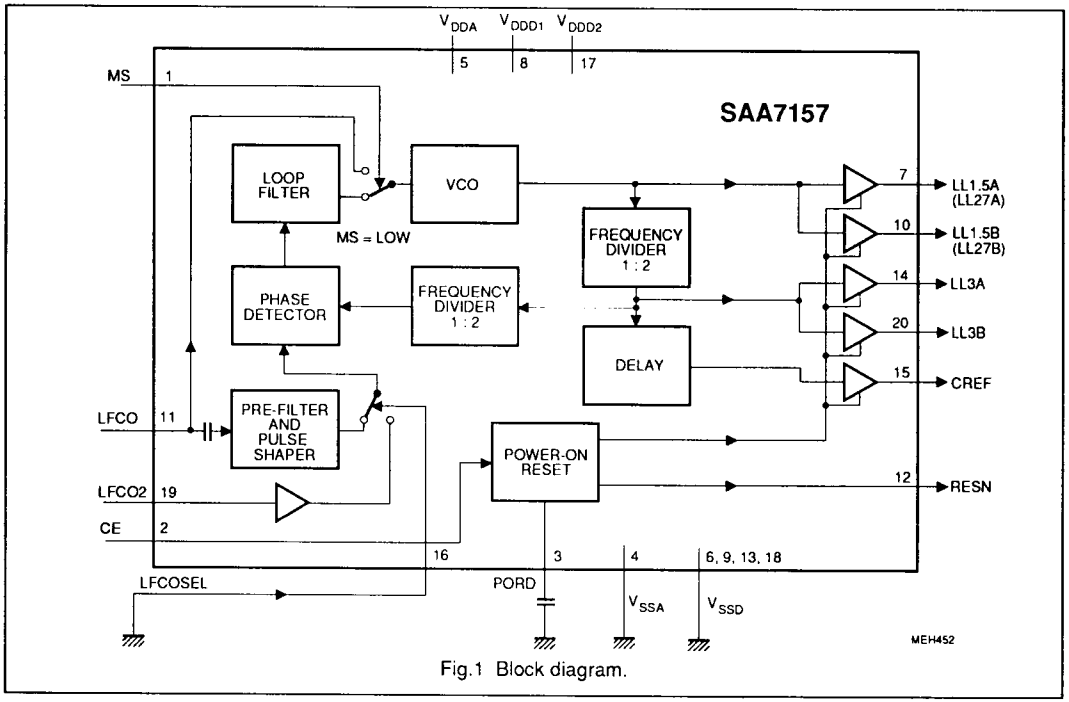

Fig.1 Block diagram.

FUNCTION DESCRIPTION

The SAA7157 generates all clock signals required for a digital TV system suitable for the SAA715x family consisting of an 8-bit analog-to-digital converter (ADC8), digital video multistandard decoder (DMSD2) and video enhancement and D/A processor circuit (VEDA). Optional extras (feature box, video memory etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.
The 6.75 MHz input signal LFCO (triangular waveform) coming from the DMSD or LFCO2 is multiplied to 27 MHz by the PLL (including phase detector, loop filter, VCO and frequency divider) and output on LL1.5A (pin7) and LL1.5B (pin 10). The 13.5 MHz frequencies are generated by dividers using ratio of 1:2 and are output on LL3A (pin 14) and LL3B (pin 20).

The rectangular output signals have 50 % duty factor. Outputs with equal frequency may be connected together externally. The clock outputs go HIGH during power-on reset (and chip enable) to ensure that no output clock signals are available before the PLL has locked-on.

Mode select MS

The LFCO input signal is directly connected to the VCO at MS = HIGH. The circuit operates as an oscillator and frequency divider. This function is not tested.

Source select LFCOSEL

Line frequency control signal (LFCO) is selected by LFCOSEL input.
LFCOSEL = LOW:
signal from LFCO (pin 11) is selected.
LFCOSEL = HIGH:
signal from LFCO2 (pin 19) is selected.
This function is not tested.

Chip enable CE

The buffer outputs are enabled and RESN is set to HIGH by CE = HIGH (Fig.4).
CE = LOW sets the clock outputs HIGH and RESN output LOW.

CREF output

TV2 digital clock reference output signal. Clock qualifier signal to TV system with 2 times of LFCO or LFCO2 frequency.

Power-on reset

Power-on reset is activated at power-on, when the supply voltage decreases below 3.5 V (Fig.4) or when chip enable is done. The indicator output RESN is LOW for a time determined by capacitor on pin 3. The RESN signal can be applied to reset other circuits of this digital TV system.
The LFCO or LFCO2 input signals have to be applied before RESN becomes HIGH.

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PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V_{SSA}	4	analog ground (0 V)
V_{DDA}	5	analog supply voltage (+5 V)
V_{SSD1}	6	digital ground 1 (0 V)
LL1.5A	7	line-locked clock output signal 1.5A (4 times f_{LFCO})
V_{DDD1}	8	digital supply voltage 1 (+5 V)
V_{SSD2}	9	digital ground 2 (0 V)
LL1.5B	10	line-locked clock output signal 1.5B (4 times f_{LFCO})
LFCO	11	line-locked frequency control input signal 1
RESN	12	reset output (active-LOW, Fig.4)
V_{SSD3}	13	digital ground 3 (0 V)
LL3A	14	line-locked clock output signal 3A (2 times f_{LFCO})
CREF	15	clock reference output, qualifier signal (2 times f_{LFCO})
LFCOSEL	16	LFCO source select (LOW = LFCO selected)*
V_{DDD2}	17	digital supply voltage 2 (+5 V)
V_{SSD4}	18	digital ground 4 (0 V)
LFCO2	19	line-locked frequency control input signal 2*
LL3B	20	line-locked clock output signal 3B (2 times f_{LFCO})

PIN CONFIGURATION

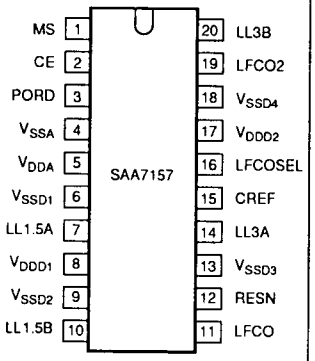

Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); ground pins as well as supply pins together connected.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	−0.5	7.0	V
V_{DDD}	digital supply voltage (pins 8 and 17)	−0.5	7.0	V
$V_{diff\ GND}$	difference voltage $V_{DDA} - V_{DDD}$	-	±100	mV
V_O	output voltage (I_{OM} = 20 mA)	−0.5	V_{DDD}	V
P_{tot}	total power dissipation (DIL20)	0	1.1	W
T_{stg}	storage temperature range	−65	150	°C
T_{amb}	operating ambient temperature range	0	70	°C
V_{ESD}	electrostatic handling** for all pins	-	tbf	V

* MS and LFCO2 functions are not tested. LFCO2 is a multiple of horizontal frequency.

** Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices ".

CHARACTERISTICS

V_{DDA} = 4.5 to 5.5 V; V_{DDD} = 4.5 to 5.5 V; f_{LFCO} = 6.0 to 7.25 MHz and T_{amb} = 0 to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
I_{DDA}	analog supply current (pin 5)		3	-	9	mA
I_{DDD}	digital supply current ($I_8 + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.0	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, LFCOSEL and LFCO2 (pins 1, 2, 16 and 19); note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DDD}	V
f_{LFCO2}	input frequency range for LFCO2		6.0	-	7.25	MHz
I_{LI}	input leakage current	LFCOSEL	50	-	150	µA
		others	-	-	10	µA
C_I	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
t_d	RESN delay time	C_3 = 0.1µF; Fig.4	20	-	200	ms
Output CREF (pin 15)						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.4	-	V_{DDD}	V
f_{CREF}	output frequency CREF	Fig.3	-	2 $f_{LFCO(2)}$		MHz
C_L	output load capacitance		15	-	40	pF
t_{SU}	set-up time	Fig.3; note 1	12	-	-	ns
t_{HD}	hold time	Fig.3; note 1	4	-	-	ns
Output signals LL1.5A, LL1.5B, LL3A and LL3B (pins 7, 10, 14, and 20); note 3						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_{OH} = −0.5 mA	2.6	-	V_{DDD}	V
t_{comp}	composite rise time	Fig.3; notes 1 and 2	-	-	8	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{LL}	output frequency LL1.5A	Fig.3	-	4 $f_{LFCO(2)}$		MHz
	output frequency LL1.5B		-	4 $f_{LFCO(2)}$		MHz
	output frequency LL3A		-	2 $f_{LFCO(2)}$		MHz
	output frequency LL3B		-	2 $f_{LFCO(2)}$		MHz
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	5	ns
t_{LL}	duty factor LL1.5A, LL1.5B, LL3A and LL3B (mean values)	note 1; Fig.3; at 1.5 V level	43	50	57	%

Notes to the characteristics

1. f_{LFCO} = 7.0 MHz and output load 40 pF (Fig.3). V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V. Skew between two LLx clocks will not deviate more than ±2 ns if output loads are matched within 20 %.
3. MS and LFCO2 functions not tested.

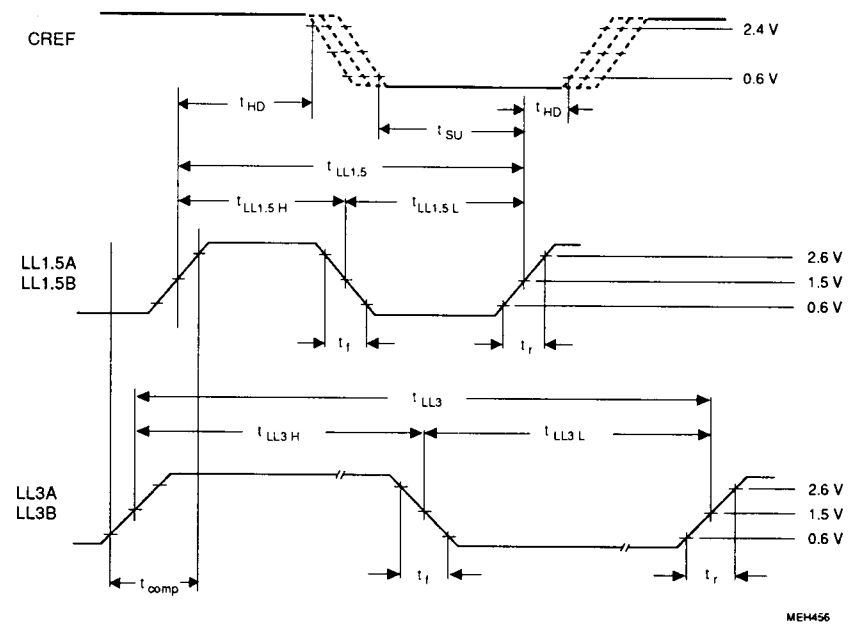

Fig.3 Output timing.

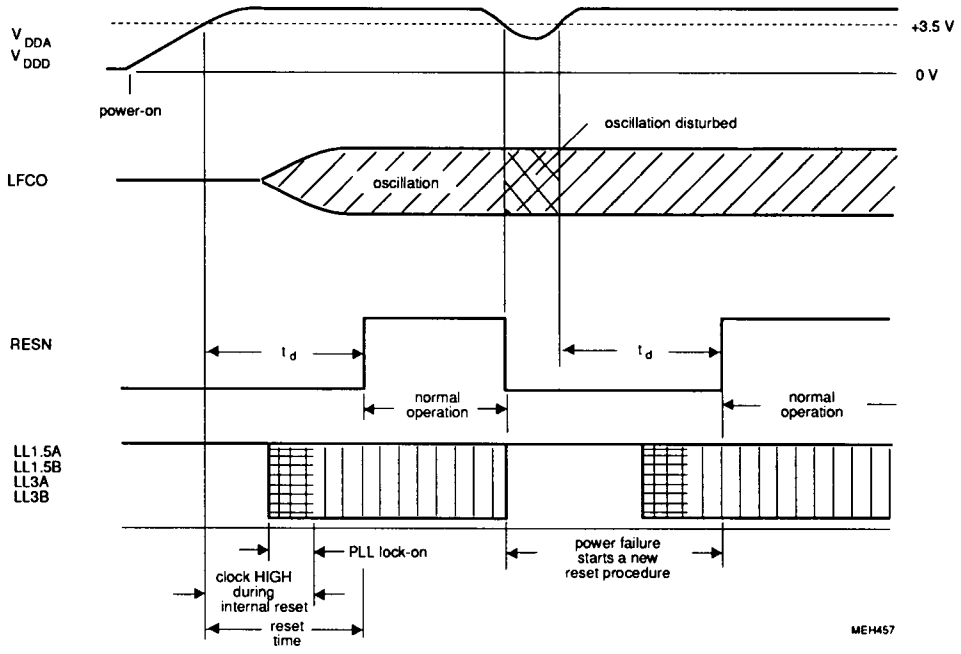

Fig.4 Reset procedure.

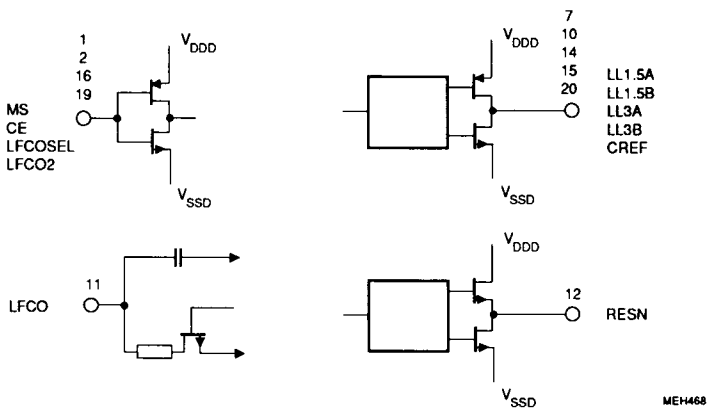

Fig.5 Internal circuit.