Fast Infrared Transceiver Module Family (1.152 Mbit/s) for 3.3 V and 5.0 V Operation

Description

The TFDU5100, TFDS5500, and TFDT5500 are a family of low–power infrared transceiver modules compliant to the IrDA 1.2 standard for fast infrared data communication, supporting IrDA speeds up to 1.152 Mbit/s (Medium IR, MIR), HP-SIR, Sharp ASK and carrier based remote control modes up to 500 kHz. Integrated within the transceiver modules are a photo PIN diode, infrared emitter (IRED), and a low–power CMOS control IC to provide a total front–end solution in a single package. Vishay Semiconductors transceivers are available in three package options, including our Baby Face package (as TFDU5100), the smallest MIR transceiver available on the market. This wide selection provides flexibility for a variety of applications and space constraints. The transceivers are capable of directly interfacing with a wide variety of I/O chips which perform the modulation/ demodulation function, including National Semiconductor's PC87338, PC87108 and PC87109, SMC's FDC37C669, FDC37N769 and CAM35C44, and Hitachi's SH3. At a minimum, a current–limiting resistor in series with the infrared emitter and a V_{CC} bypass capacitor are the only external components required to implement a complete solution.

Features

- Compliant to IrDA 1.2 (Up to 1.152 Mbit/s), HP–SIR®, Sharp ASK® and TV Remote
- Operating in 3.3 V and 5 V Applications
- Low Power Consumption (3 mA Supply Current)
- Power Shutdown Mode (1 μA Shutdown Current)
- Three Surface Mount Package Options
  - Universal (9.7 × 4.7 × 4.0 mm)
  - Side View (13.0 × 5.95 × 5.3 mm)
  - Top View (13.0 × 7.6 × 5.95 mm)
- High Efficiency Emitter
- Baby Face (Universal) Package Capable of Surface Mount Solderability to Side and Top View Orientation
- Directly Interfaces with Various Super I/O and Controller Devices
- Built–In EMI Protection – No External Shielding Necessary
- Few External Components Required
- Backward Compatible to all Vishay Semiconductors SIR and FIR Infrared Transceivers

Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection

Package Options

TFDU5100
Baby Face (Universal)

TFDS5500
Side View

TFDT5500
Top View

This product is currently in development. Inquiries regarding the status of this product should be directed to Vishay Semiconductors Marketing.

Ordering Information

Part Number	Qty / Reel	Description
TFDU5100–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU5100–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting
TFDS5500–TR3	750 pcs	
TFDT5500–TR3	750 pcs	

Functional Block Diagram

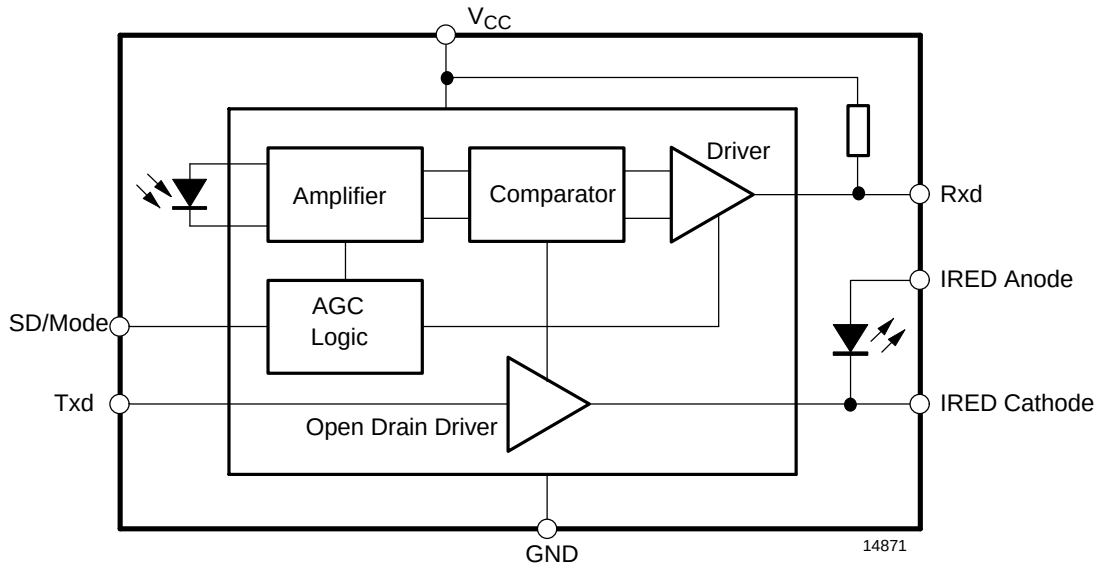


Figure 1. Functional Block Diagram

Pin Description

Pin Number		Function	Description	I/O	Active
"U" and "T" Option	"S" Option				
1	8	IRED Anode	IRED anode, to be externally connected to V_{CC} through a current control resistor		
2	1	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	7	Txd	Transmit Data Input	I	HIGH
4	2	Rxd	Received Data Output, push–pull CMOS driver output capable of driving a standard CMOS or TTL load. No external pull–up or pull–down resistor is required (pin is floating when device is in shutdown mode)	O	LOW
5	6	SD/Mode	Shutdown/Mode	I	HIGH
6	3	V_{CC}	Supply Voltage		
7	5	Mode	High: High speed mode, MIR; LOW: Low speed mode, SIR only (see chapter "Mode Switching")	I	
8	4	GND	Ground		

“U” Option Baby Face (Universal) **“S” Option Side View** **“T” Option Top View**

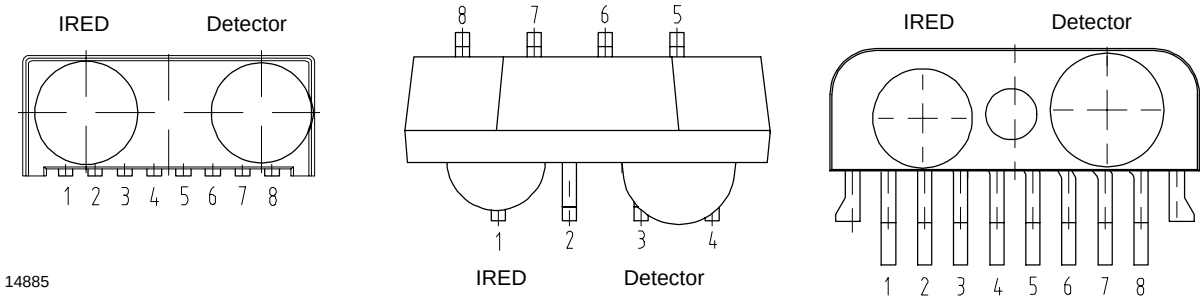


Figure 2. Pinnings

Absolute Maximum Ratings

Reference point Pin GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range		V_{CC}	– 0.5		6	V
Input Currents	For all Pins, Except IRED Anode Pin				10	mA
Output Sinking Current					25	mA
Power Dissipation	See Derating Curve	P_D			350	mW
Junction Temperature		T_J			125	°C
Ambient Temperature Range (Operating)		T_{amb}	–25		+85	°C
Storage Temperature Range		T_{stg}	–25		+85	°C
Soldering Temperature	See Recommended Solder Profile (see figure 9)				240	°C
Average Output Current		I_{IRED} (DC)			135	mA
Repetitive Pulsed Output Current	<90 µs, t_{on} <20%	I_{IRED} (RP)			600	mA
IRED Anode Voltage		V_{IREDA}	– 0.5		V_{CC}+1.5	V
Transmitter Data Input Voltage		V_{Txd}	– 0.5		V_{CC}+0.5	V
Receiver Data Output Voltage		V_{Rxd}	– 0.5		V_{CC}+0.5	V
Virtual Source Size	Method: (1–1/e) encircled energy	d	2.5	2.8		mm
Maximum Intensity for Class 1 Operation of IEC825–1 or EN60825–1 (worst case IrDA FIR pulse pattern)	EN60825, 1997				320	mW/sr

Electrical Characteristics.

T_{amb} = 25°C, V_{CC} = 3.0 V to 5.25 Vunless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Transceiver						
Supply Voltage		V_{CC}	3	3.3	5.25	V
Dynamic Supply Current	SD = Low, E_e = 0 klx SD = Low, E_e = 1 klx *) Receive mode only. In transmit mode, add additional 100 mA (typ) for IRED current.	I_{CC}		3 3	4.5 4.5	mA
Standby Supply Current	SD = High **) Mode = floating, Txd = 0 V T = 25°C, E_e = 0 klx T = 25°C, E_e = 1 klx *)	I_{SD}			 1 1.5	 µA µA
	SD = High **) Mode = floating, Txd = 0 V, T = 85°C Not Ambient Light Sensitive	I_{SD}			5	µA
Operating Temperature Range		T_A	–25		+85	°C
Output Voltage Low	R_{Load} = 2.2 kΩ C_{Load} = 15 pF	V_{OL}		0.5	0.8	V
Output Voltage High	R_{Load} = 2.2 kΩ C_{Load} = 15 pF	V_{OH}	V_{CC}–0.5			V
Input Voltage Low (Txd, SD/Mode, Mode)		V_{IL}	0		0.8	V
Input Voltage High (Txd, SD/Mode, Mode)	CMOS level	V_{IH}	0.9×V_{CC}			V
	TTL level, $V_{CC} \geq 4.5$	V_{IH}	2.4			V
Input Leakage Current (Txd, SD/Mode, Mode)		I_L	–10		+10	µA
Input Capacitance		C_I			5	pF

*) Standard illuminant A

**) CMOS level only, not TTL

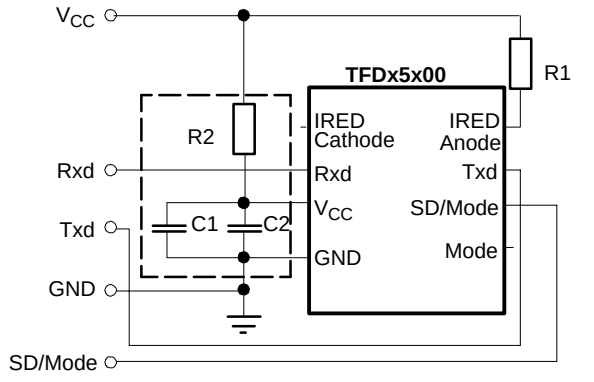
Optoelectronic Characteristics

T_{amb} = 25°C, V_{CC} = 3.0 V to 5.25 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Receiver						
Minimum Detection Threshold Irradiance SIR Mode	TFDS5500/TFDT5500 9.6 kbit/s to 115.2 kbit/s, 3.0 V λ = 850 nm – 900 nm	E_e		20	35	mW/m^2
	TFDU5100 9.6 kbit/s to 115.2 kbit/s, 3.0 V λ = 850 nm – 900 nm	E_e		25	40	mW/m^2
Minimum Detection Threshold Irradiance MIR Mode	TFDS5500/TFDT5500, 3.0 V 1.152 Mbit/s λ = 850 nm – 900 nm	E_e		65	90	mW/m^2
	TFDU5100, 3.0 V 1.152 Mbit/s, λ = 850 nm – 900 nm	E_e		85	100	mW/m^2
Maximum Detection Threshold Irradiance	V_{CC} = 3.0 V λ = 850 nm – 900 nm	E_e	5	10		kW/m^2
Logic LOW Receiver Input Irradiance		E_e	4			mW/m^2
Rise Time of Output Signal	10% to 90%, @2.2 kΩ, 15 pF	$t_{r\ (Rxd)}$	10		40	ns
Fall Time of Output Signal	90% to 10%, @2.2 kΩ, 15 pF	$t_{f\ (Rxd)}$	10		40	ns
Rxd Pulse Width of Output Signal, 50%, SIR mode	Input pulse length 20 µs, 9.6 kbit/s	t_{PW}	1.2	10	20	µs
	Input pulse length 1.41 µs, 115.2 kbit/s	t_{PW}	1.2		1/2 bit lenght	µs
Rxd Pulse Width of Output Signal, 50%, MIR mode	Input pulse length 217 ns, 1.152 Mbit/s	t_{PW}	110		260	ns
Jitter, Leading Edge, MIR mode	Input Irradiance = 100 mW/m^2, 1.152 Mbit/s mode				10	ns
Latency		t_L			120	µs
Transmitter						
IRED Operating Current	R1 = 7.2 Ω, V_{CC} = 5.0 V	I_D		0.4	0.55	A
Output Radiant Intensity, (see fig. 3)	Vcc = 5.0 V, α = 0°, 15° Txd = High, SD = Low, R1 = 7.2 Ω	I_e	100	140	320	mW/sr
Output Radiant Intensity	Vcc = 5.0 V, α = 0°, 15° Txd = Low, or SD = High (Receiver is inactive as long as SD = High) R1 = 7.2 Ω	I_e			0.04	mW/sr
Output Radiant Intensity, Angle of Half Intensity		α		±24		°
Peak – Emission Wavelength		$λ_P$	880		900	nm
Optical Rise Time, Fall Time		t_{ropt}, t_{fopt}	10		40	ns
Optical Overshoot					10	%

Recommended Circuit Diagram

The only required component for designing an IrDA 1.2 compatible design using Vishay Semiconductors FIR transceivers is a current limiting resistor, R1, to the IRED. However, depending on the entire system design and board layout, additional components may be required (see figure 3).



Note: Outlined components are optional depending on the quality of the power supply.

Figure 3. Recommended Application Circuit

Vishay Semiconductors transceivers integrate a sensitive receiver and a built–in power driver. The combination of both needs a careful circuit board layout. The use of thin, long resistive and inductive wiring should be avoided. The inputs (Txd, SD/Mode) and the output Rxd should be directly (DC) coupled to the I/O circuit.

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 see figure 4. For IrDA compliant operation, a current control resistor of 7.2 Ω is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet.

R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{CC} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

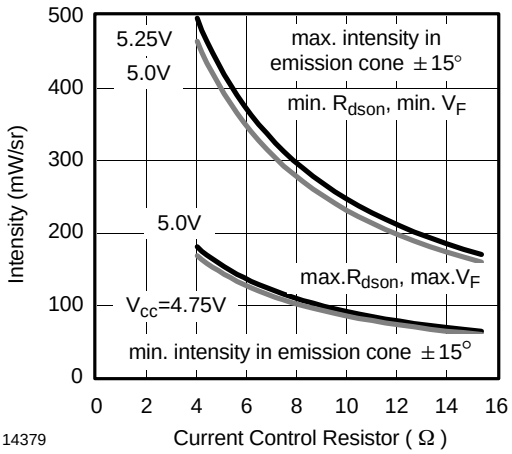


Figure 4. Intensity I_e vs. Current Control Resistor R1

The placement of these parts is critical. It is strongly recommended to position C2 as near as possible to the transceiver power supply pins. An electrolytic capacitor should be used for C1 while a ceramic capacitor is used for C2. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.

Table 1. Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1	4.7 µF, 16 V	293D 475X9 016B 2T
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	5 V supply voltage: 7.2 Ω , 0.25 W (recommend using two 3.6 Ω, 0.125 W resistors in series)	CRCW–1206–3R60–F–RT1
	3.3 V supply voltage: 3.6 Ω , 0.25 W (recommend using two 1.8 Ω, 0.125 W resistors in series)	CRCW–1206–1R80–F–RT1
R2	47 Ω , 0.125 W	CRCW–1206–47R0–F–RT1

Mode Switching

The TFDU5100, TFDS5500 and TFDT5500 do not power on with a default mode, therefore the data transfer rate has to be set by a programming sequence using the Txd and SD/Mode inputs as described below or selected by setting the mode pin. The Mode pin can be used to statically set the mode (Mode pin: LOW: SIR, High: 0.576 Mbit/s to 1.152 Mbit/s). When using the Mode pin, the standby current may increase to about 50 μA to 60 μA when high or low. If not used or in standby mode, the mode input should float to minimize standby current. The low frequency mode covers speeds up to 115.2 kbit/s. Signals with higher data rates should be detected in the high frequency mode. Lower-frequency data can also be received in the high frequency mode but with reduced sensitivity. To switch the transceivers from low frequency mode to the 1.152 Mbit/s mode and vice versa, the programming sequences described below are required.

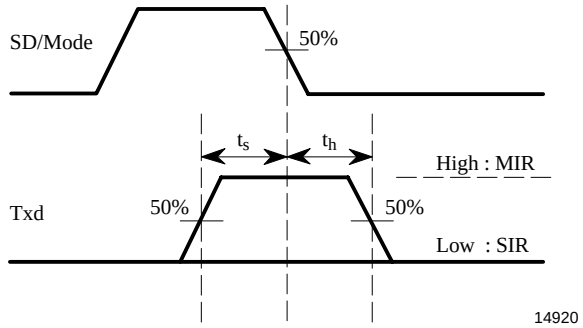


Figure 5. Mode Switching Timing Diagram

Setting to the High Bandwidth Mode (0.576 Mbit/s to 1.152 Mbit/s)

1. Set SD/MODE input to logic “HIGH”.
2. Set Txd input to logic “HIGH”. Wait $t_s \geq 200$ ns.
3. Set SD/MODE to logic “LOW” (this negative edge latches state of Txd, which determines speed setting).
4. After waiting $t_h \geq 200$ ns Txd can be set to logic “LOW”. The hold time of Txd is limited by the maximum allowed pulse length.

Txd is now enabled as normal Txd input for the high bandwidth mode.

Setting to the Lower Bandwidth Mode (2.4 kbit/s to 115.2 kbit/s)

1. Set SD/MODE input to logic “HIGH”.
2. Set Txd input to logic “LOW”. Wait $t_s \geq 200$ ns.
3. Set SD/MODE to logic “LOW” (this negative edge latches state of Txd, which determines speed setting).
4. Txd must be held for $t_h \geq 200$ ns.

Txd is now enabled as normal Txd input for the lower bandwidth mode.

Recommended SMD Pad Layout

The leads of the device should be soldered in the center position of the pads.

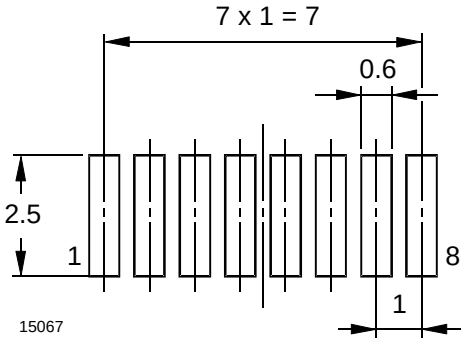


Figure 6. TFDU5100 Baby Face (Universal)

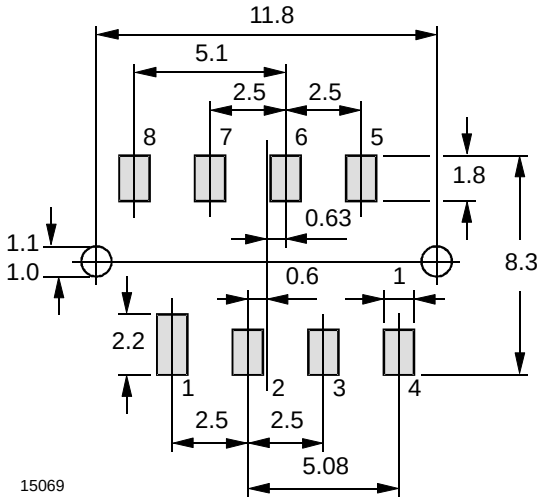


Figure 7. TFDS5500 Side View Package
Note: Leads of the device should be at least 0.3mm within the ends of the pads.
Pad 1 is longer to designate Pin 1 connection to transceiver

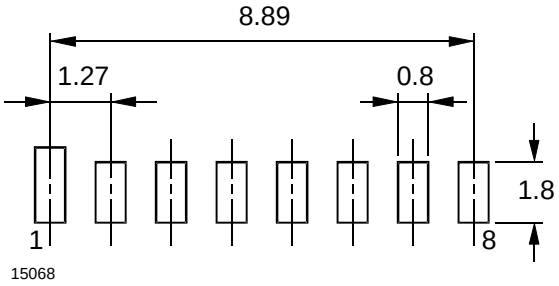


Figure 8. TFDT5500 Top View Package
Note: Leads of the device should be at least 0.3mm within the ends of the pads.
Pad 1 is longer to designate Pin 1 connection to transceiver.

Recommended Solder Profile

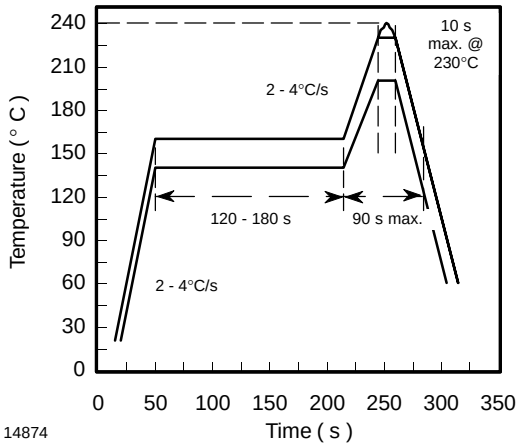


Figure 9. Recommended Solder Profile

Current Derating Diagram

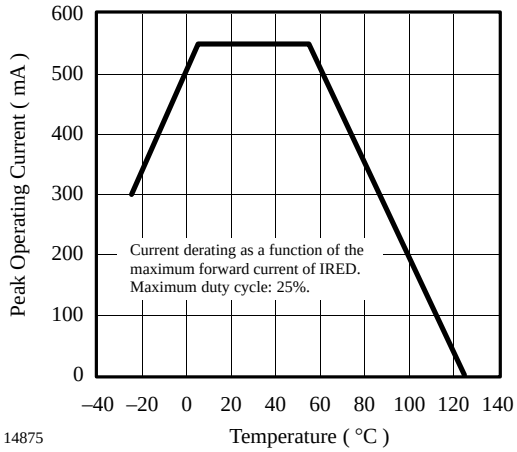
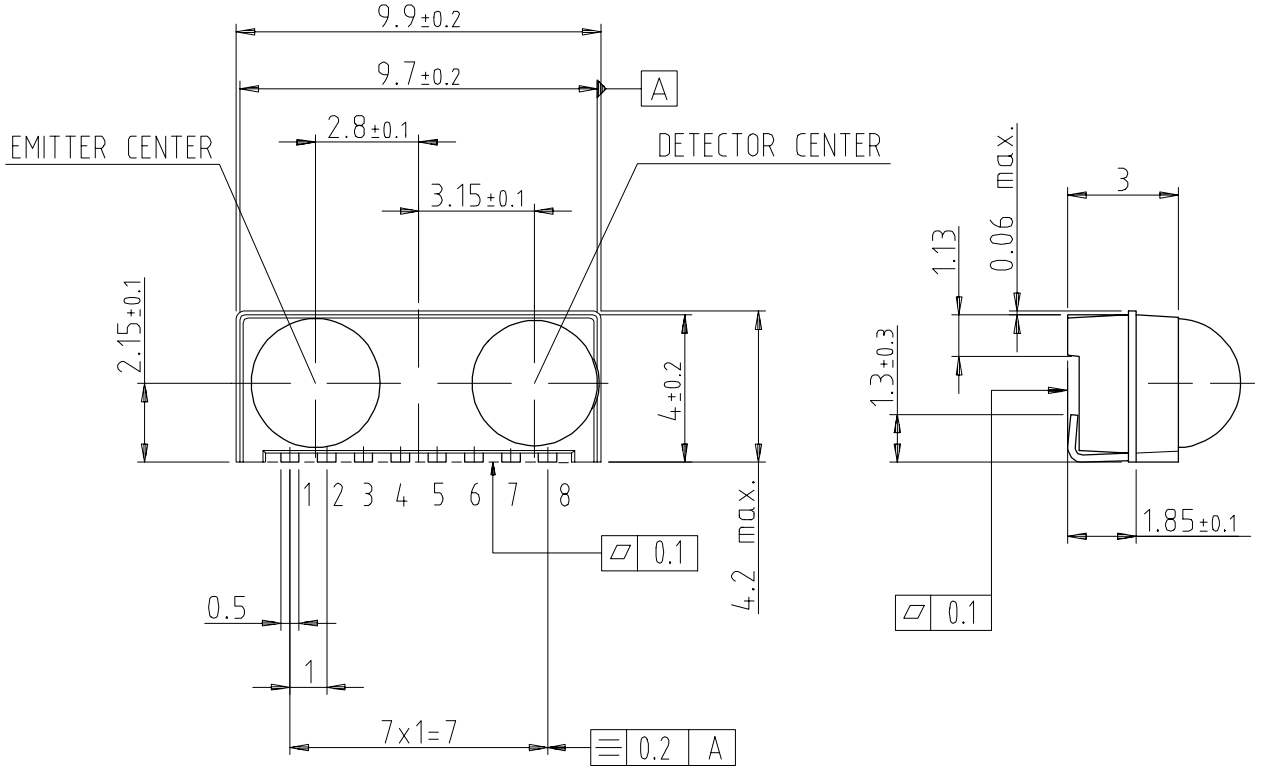
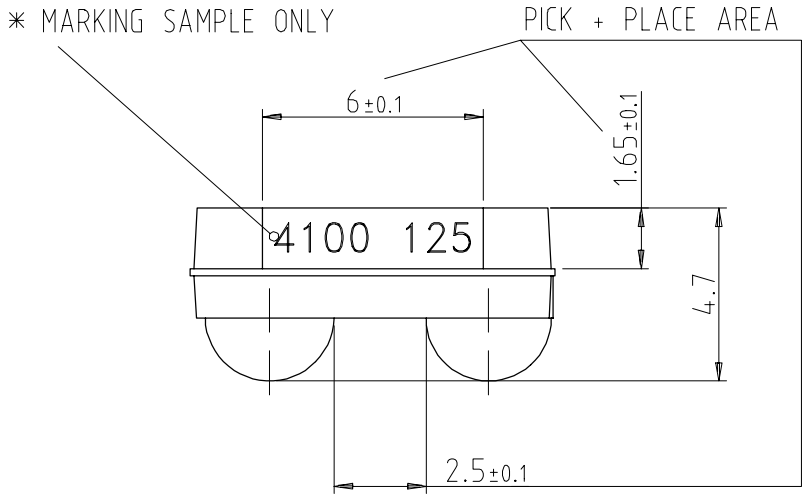


Figure 10. Current Derating Diagram

TFDU5100 – Baby Face (Universal) Package (Mechanical Dimensions)





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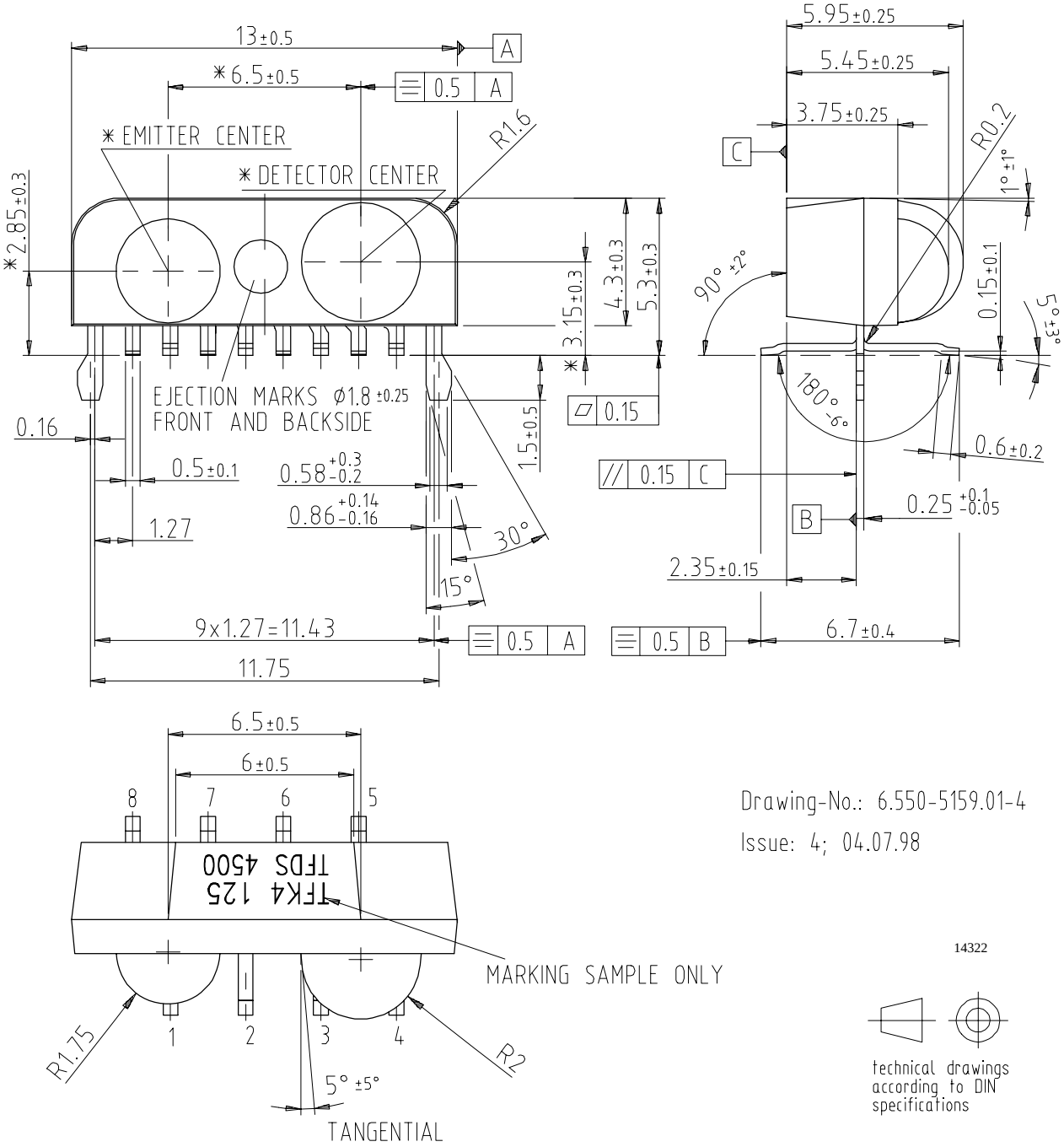
technical drawings according to DIN specifications

* MARKING ORIENTATION 180 DEGREES ALLOWED

Drawing-No.: 6.550-5148.01-4
Issue: 8; 10.7.98

TFDS5500 – Side View Package (Mechanical Dimensions)



Drawing-No.: 6.550-5159.01-4
Issue: 4; 04.07.98

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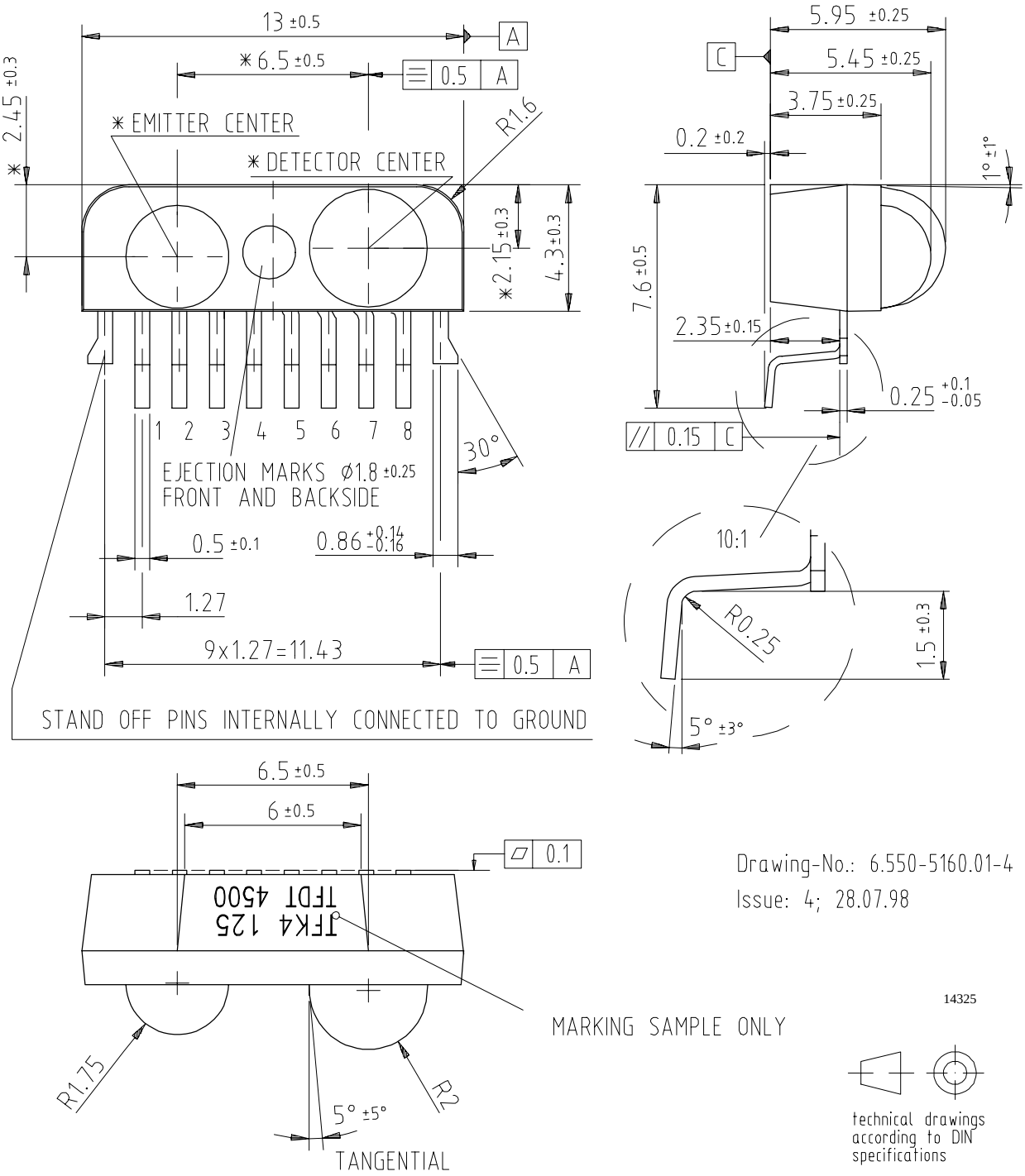
technical drawings
according to DIN
specifications

TFDT5500 – Top View Package (Mechanical Dimensions)



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Issue: 4; 28.07.98

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technical drawings
according to DIN
specifications

Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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