ELPIDA

**PRELIMINARY DATA SHEET**

# 256M bits SDRAM
# WTR (Wide Temperature Range)

## EDS2504APTA-TI (64M words × 4 bits)
## EDS2508APTA-TI (32M words × 8 bits)
## EDS2516APTA-TI (16M words × 16 bits)

### Description

The EDS2504AP is a 256M bits SDRAM organized as 16,777,216 words × 4 bits × 4 banks. The EDS2508 AP is a 256M bits SDRAM organized as 8,388,608 words × 8 bits × 4 banks. The EDS2516 AP is a 256M bits SDRAM organized as 4194304 words × 16 bits × 4 banks. All inputs and outputs are referred to the rising edge of the clock input. It is packaged in standard 54-pin plastic TSOP (II).

### Features

- 3.3V power supply
- Clock frequency: 133MHz (max.)
- LVTTL interface
- Single pulsed /RAS
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8, full page
- 2 variations of burst sequence
  - — Sequential (BL = 1, 2, 4, 8)
  - — Interleave (BL = 1, 2, 4, 8)
- Programmable /CAS latency (CL): 2, 3
- Byte control by DQM
  : DQM (EDS2504/08AP)
  : UDQM, LDQM (EDS2516AP)
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh
- Ambient temperature range: –40 to +85°C

### Pin Configurations

/xxx indicates active low signal.

54-pin plastic TSOP (II)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| VDD | VDD | VDD | 1 | 54 | VSS | VSS | VSS |
| NC | DQ0 | DQ0 | 2 | 53 | DQ15 | DQ7 | NC |
| VDDQ | VDDQ | VDDQ | 3 | 52 | VSSQ | VSSQ | VSSQ |
| NC | NC | DQ1 | 4 | 51 | DQ14 | NC | NC |
| DQ0 | DQ1 | DQ2 | 5 | 50 | DQ13 | DQ6 | DQ3 |
| VSSQ | VSSQ | VSSQ | 6 | 49 | VDDQ | VDDQ | VDDQ |
| NC | NC | DQ3 | 7 | 48 | DQ12 | NC | NC |
| NC | DQ2 | DQ4 | 8 | 47 | DQ11 | DQ5 | NC |
| VDDQ | VDDQ | VDDQ | 9 | 46 | VSSQ | VSSQ | VSSQ |
| NC | NC | DQ5 | 10 | 45 | DQ10 | NC | NC |
| DQ1 | DQ3 | DQ6 | 11 | 44 | DQ9 | DQ4 | DQ2 |
| VSSQ | VSSQ | VSSQ | 12 | 43 | VDDQ | VDDQ | VDDQ |
| NC | NC | DQ7 | 13 | 42 | DQ8 | NC | NC |
| VDD | VDD | VDD | 14 | 41 | VSS | VSS | VSS |
| NC | NC | LDQM | 15 | 40 | NC | NC | NC |
| /WE | /WE | /WE | 16 | 39 | UDQM | DQM | DQM |
| /CAS | /CAS | /CAS | 17 | 38 | CLK | CLK | CLK |
| /RAS | /RAS | /RAS | 18 | 37 | CKE | CKE | CKE |
| /CS | /CS | /CS | 19 | 36 | A12 | A12 | A12 |
| BA0 | BA0 | BA0 | 20 | 35 | A11 | A11 | A11 |
| BA1 | BA1 | BA1 | 21 | 34 | A9 | A9 | A9 |
| A10 | A10 | A10 | 22 | 33 | A8 | A8 | A8 |
| A0 | A0 | A0 | 23 | 32 | A7 | A7 | A7 |
| A1 | A1 | A1 | 24 | 31 | A6 | A6 | A6 |
| A2 | A2 | A2 | 25 | 30 | A5 | A5 | A5 |
| A3 | A3 | A3 | 26 | 29 | A4 | A4 | A4 |
| VDD | VDD | VDD | 27 | 28 | VSS | VSS | VSS |

X 16
X 8
X 4

(Top view)

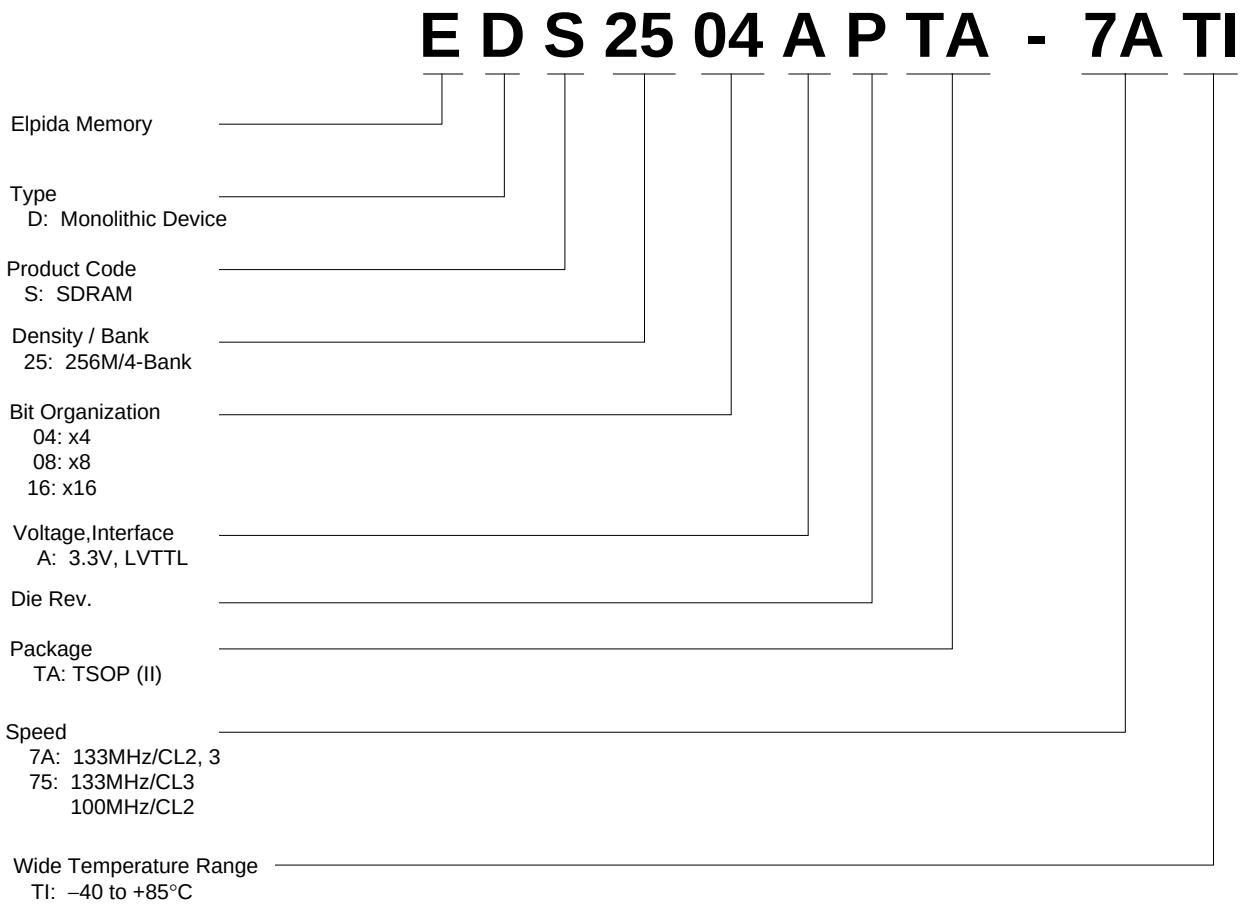
| | | | |
|---|---|---|---|
| A0 to A12, | Address input | DQM | Input/output mask |
| BA0, BA1 | Bank select address | CKE | Clock enable |
| DQ0 to DQ15 | Data-input/output | CLK | Clock input |
| /CS | Chip select | VDD | Power for internal circuit |
| /RAS | Row address strobe | VSS | Ground for internal circuit |
| /CAS | Column address strobe | VDDQ | Power for DQ circuit |
| /WE | Write enable | VSSQ | Ground for DQ circuit |
| | | NC | No connection |

Document No. E0248E20 (Ver. 2.0)
Date Published October 2002 (K) Japan
URL: http://www.elpida.com

## Ordering Information

| Part number | Mask Version | Organization (words × bits) | Internal Banks | Clock frequency MHz (max.) | /CAS latency | Package |
|---|---|---|---|---|---|---|
| EDS2504APTA-7ATI<br>EDS2504APTA-75TI | P | 64M × 4 | 4 | 133 | 2, 3<br>3 | 54-pin Plastic TSOP (II) |
| EDS2508APTA-7ATI<br>EDS2508APTA-75TI | | 32M × 8 | | | 2, 3<br>3 | |
| EDS2516APTA-7ATI<br>EDS2516APTA-75TI | | 16M × 16 | | | 2, 3<br>3 | |

## Part Number



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## Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 100 μs and then, execute Power on sequence and CBR (auto) Refresh before proper device operation is achieved.

### Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Voltage on any pin relative to VSS | VT | –0.5 to VDD + 0.5 (≤ 4.6 (max.)) | V | |
| Supply voltage relative to VSS | VDD | –0.5 to +4.6 | V | |
| Short circuit output current | IOS | 50 | mA | |
| Power dissipation | PD | 1.0 | W | |
| Operating temperature | TA | –40 to +85 | °C | |
| Storage temperature | Tstg | –55 to +125 | °C | |

Notes: 1. Respect to VSS.

**Caution**

**Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended Operating Conditions (TA = –40 to +85°C)

| Parameter | Symbol | min. | max. | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage | VDD, VDDQ | 3.0 | 3.6 | V | 1, 2 |
| | VSS, VSSQ | 0 | 0 | V | 3 |
| Input high voltage | VIH | 2.0 | VDD + 0.3 | V | 1, 4 |
| Input low voltage | VIL | –0.3 | 0.8 | V | 1, 5 |

Notes: 1. All voltage referred to VSS.
2. The supply voltage with all VDD and VDDQ pins must be on the same level.
3. The supply voltage with all VSS and VSSQ pins must be on the same level.
4. VIH (max.) = VDD + 2.0 V for pulse width ≤ 3ns at VDD.
5. VIL (min.) = VSS – 2.0 V for pulse width ≤ 3ns at VSS.

**DC Characteristics 1 (TA = –40 to +85ºC, VDD, VDDQ = 3.3V ± 0.3V, VSS, VSSQ = 0V)**

| Parameter | | | max. | | | | | |
|---|---|---|---|---|---|---|---|---|
| /CAS latency | Symbol | Grade | × 4 | × 8 | × 16 | Unit | Test condition | Notes |
| Operating current | ICC1 | -7A | 130 | 130 | 135 | mA | Burst length = 1<br>tRC = min. | 1, 2, 3 |
| | ICC1 | -75 | 110 | 110 | 115 | mA | Burst length = 1<br>tRC = min. | |
| Standby current in power down | ICC2P | | 3 | 3 | 3 | mA | CKE = VIL, tCK = min. | 6 |
| Standby current in power down (input signal stable) | ICC2PS | | 2 | 2 | 2 | mA | CKE = VIL, tCK = ∞ | 7 |
| Standby current in non power down | ICC2N | | 20 | 20 | 20 | mA | CKE, /CS = VIH,<br>tCK = min. | 4 |
| Standby current in non power down (input signal stable) | ICC2NS | | 9 | 9 | 9 | mA | CKE = VIH, tCK = ∞,<br>/CS = VIH | 8 |
| Active standby current in power down | ICC3P | | 4 | 4 | 4 | mA | CKE = VIL, tCK = min. | 1, 2, 6 |
| Active standby current in power down (input signal stable) | ICC3PS | | 3 | 3 | 3 | mA | CKE = VIL, tCK = ∞ | 2, 7 |
| Active standby current in non power down | ICC3N | | 30 | 30 | 30 | mA | CKE, /CS = VIH,<br>tCK = min. | 1, 2, 4 |
| Active standby current in non power down (input signal stable) | ICC3NS | | 15 | 15 | 15 | mA | CKE = VIH, tCK = ∞,<br>/CS = VIH | 2, 8 |
| Burst operating current | ICC4 | | 130 | 135 | 145 | mA | tCK = min., BL = 4 | 1, 2, 5 |
| Refresh current | ICC5 | -7A | 250 | 250 | 250 | mA | tRC = min. | 3 |
| | ICC5 | -75 | 220 | 220 | 220 | mA | tRC = min. | |
| Self refresh current | ICC6 | | 3 | 3 | 3 | mA | VIH ≥ VDD – 0.2V<br>VIL ≤ 0.2V | |

Notes: 1. ICC depends on output load condition when the device is selected. ICC (max.) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CLK operating current.
7. After power down mode, no CLK operating current.
8. Input signals are VIH or VIL fixed.

**DC Characteristics 2 (TA = –40 to +85°C, VDD, VDDQ = 3.3V ± 0.3V, VSS, VSSQ = 0V)**

| Parameter | Symbol | min. | max. | Unit | Test condition | Notes |
|---|---|---|---|---|---|---|
| Input leakage current | ILI | –1 | 1 | µA | 0 ≤ VIN ≤ VDD | |
| Output leakage current | ILO | –1.5 | 1.5 | µA | 0 ≤ VOUT ≤ VDD, DQ = disable | |
| Output high voltage | VOH | 2.4 | — | V | IOH = –4 mA | |
| Output low voltage | VOL | — | 0.4 | V | IOL = 4 mA | |

**Pin Capacitance (TA = 25°C, VDD, VDDQ = 3.3V ± 0.3V)**

| Parameter | Symbol | Pins | min. | Typ | max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Input capacitance | CI1 | CLK | 2.5 | — | 3.5 | pF | 1, 2, 4 |
| | CI2 | Address, CKE, /CS, /RAS, /CAS, /WE, DQM, | 2.5 | — | 3.8 | pF | 1, 2, 4 |
| Data input/output capacitance | CI/O | DQ | 4 | — | 6.5 | pF | 1, 2, 3, 4 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1MHz, 1.4V bias, 200mV swing.
3. DQM = VIH to disable DOUT.
4. This parameter is sampled and not 100% tested.

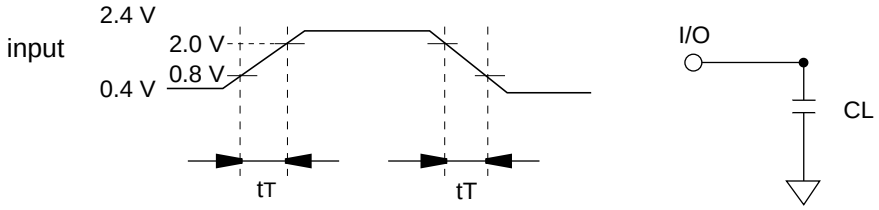
**AC Characteristics (TA = –40 to +85°C, VDD, VDDQ = 3.3V ± 0.3V, VSS, VSSQ = 0V)**

| | | -7A | -75 | | | |
|---|---|---|---|---|---|---|
| Parameter | Symbol | min. | min. | max. | Unit | Notes |
| System clock cycle time | tCK | 7.5 | 7.5 | — | ns | 1 |
| CLK high pulse width | tCH | 2.5 | 2.5 | — | ns | 1 |
| CLK low pulse width | tCL | 2.5 | 2.5 | — | ns | 1 |
| Access time from CLK | tAC | — | — | 5.4 | ns | 1, 2 |
| Data-out hold time | tOH | 2.7 | 2.7 | — | ns | 1, 2 |
| CLK to Data-out low impedance | tLZ | 1 | 1 | — | ns | 1, 2, 3 |
| CLK to Data-out high impedance | tHZ | — | — | 5.4 | ns | 1, 4 |
| Input setup time | tSI | 1.5 | 1.5 | — | ns | 1 |
| Input hold time | tHI | 0.8 | 0.8 | — | ns | 1 |
| Ref/Active to Ref/Active command period | tRC | 60 | 67.5 | — | ns | 1 |
| Active to Precharge command period | tRAS | 45 | 45 | 120000 | ns | 1 |
| Active command to column command (same bank) | tRCD | 15 | 20 | — | ns | 1 |
| Precharge to active command period | tRP | 15 | 20 | — | ns | 1 |
| Write recovery or data-in to precharge lead time | tDPL | 15 | 15 | — | ns | 1 |
| Last data into active latency | tDAL | 2CLK + 15ns | 2CLK + 20ns | — | | |
| Active (a) to Active (b) command period | tRRD | 15 | 15 | — | ns | 1 |
| Transition time (rise and fall) | tT | 0.5 | 0.5 | 5 | ns | |
| Refresh period (8192 refresh cycles) | tREF | — | — | 64 | ms | |

Notes: 1. AC measurement assumes tT = 0.5ns. Reference level for timing of input signals is 1.4V.
2. Access time is measured at 1.4V. Load condition is CL = 50pF.
3. tLZ (min.) defines the time at which the outputs achieves the low impedance state.
4. tHZ (max.) defines the time at which the outputs achieves the high impedance state.

**Test Conditions**

- Input and output timing reference levels: 1.4V
- Input waveform and output load: See following figures




**Output load**

**Relationship Between Frequency and Minimum Latency**

| Parameter | | -7A | -75 | |
|---|---|---|---|---|
| Frequency (MHz) | | 133 | | |
| tCK (ns) | Symbol | 7.5 | 7.5 | Notes |
| Active command to column command (same bank) | lRCD | 2 | 3 | 1 |
| Active command to active command (same bank) | lRC | 8 | 9 | 1 |
| Active command to precharge command (same bank) | lRAS | 6 | 6 | 1 |
| Precharge command to active command (same bank) | lRP | 2 | 3 | 1 |
| Write recovery or data-in to precharge command (same bank) | lDPL | 2 | 2 | 1 |
| Active command to active command (different bank) | lRRD | 2 | 2 | 1 |
| Self refresh exit time | lSREX | 1 | 1 | 2 |
| Last data in to active command (Auto precharge, same bank) | lDAL | 4 | 5 | = [lDPL + lRP] |
| Self refresh exit to command input | lSEC | 8 | 9 | = [lRC]<br>3 |
| Precharge command to high impedance (CL = 2) | lHZP | 2 | 2 | |
| (CL = 3) | lHZP | 3 | 3 | |
| Last data out to active command (auto precharge) (same bank) | lAPR | 1 | 1 | |
| Last data out to precharge (early precharge) (CL = 2) | lEP | –1 | –1 | |
| (CL = 3) | lEP | –2 | –2 | |
| Column command to column command | lCCD | 1 | 1 | |
| Write command to data in latency | lWCD | 0 | 0 | |
| DQM to data in | lDID | 0 | 0 | |
| DQM to data out | lDOD | 2 | 2 | |
| CKE to CLK disable | lCLE | 1 | 1 | |
| Register set to active command | lMRD | 2 | 2 | |
| /CS to command disable | lCDD | 0 | 0 | |
| Power down exit to command input | lPEC | 1 | 1 | |

Notes: 1.lRCD to lRRD are recommended value.

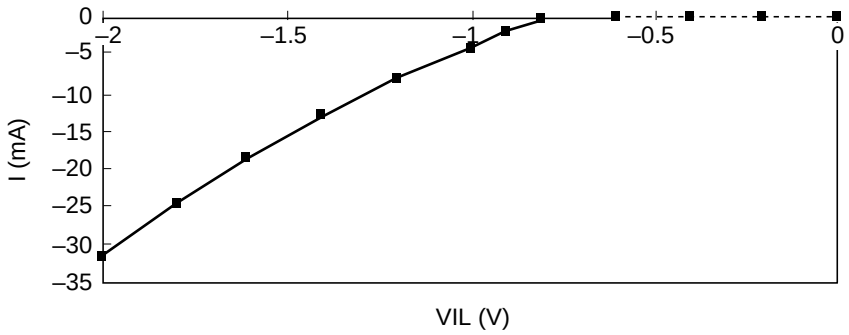
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

**VIL/VIH Clamp**

This SDRAM component has VIL and VIH clamp for CLK, CKE, /CS, DQM and DQ pins.

**[Minimum VIL Clamp Current]**

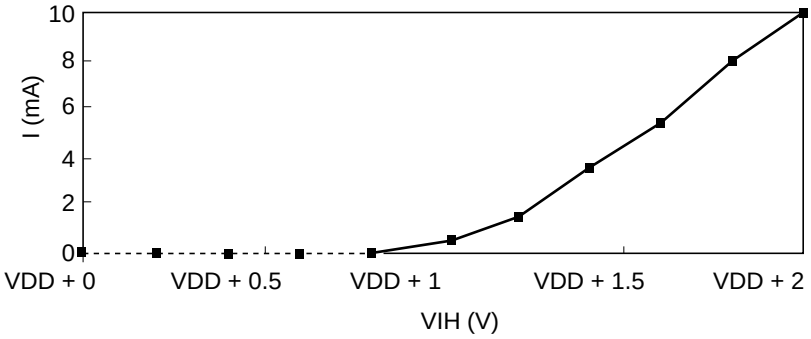
| VIL (V) | I (mA) |
|---|---|
| –2 | –32 |
| –1.8 | –25 |
| –1.6 | –19 |
| –1.4 | –13 |
| –1.2 | –8 |
| –1 | –4 |
| –0.9 | –2 |
| –0.8 | –0.6 |
| –0.6 | 0 |
| –0.4 | 0 |
| –0.2 | 0 |
| 0 | 0 |




**Minimum VIL Clamp Current**

**[Minimum VIH Clamp Current]**

| VIH (V) | I (mA) |
|---|---|
| VDD + 2 | 10 |
| VDD + 1.8 | 8 |
| VDD + 1.6 | 5.5 |
| VDD + 1.4 | 3.5 |
| VDD + 1.2 | 1.5 |
| VDD + 1 | 0.3 |
| VDD + 0.8 | 0 |
| VDD + 0.6 | 0 |
| VDD + 0.4 | 0 |
| VDD + 0.2 | 0 |
| VDD + 0 | 0 |

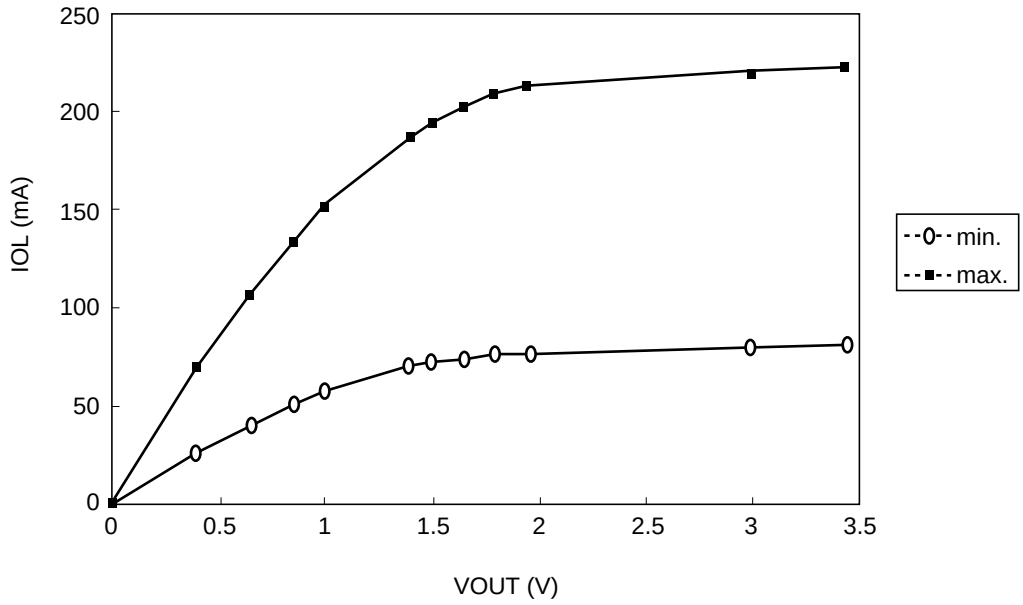



**Minimum VIH Clamp Current**

**IOL/IOH Characteristics**

**[Output Low Current (IOL)]**

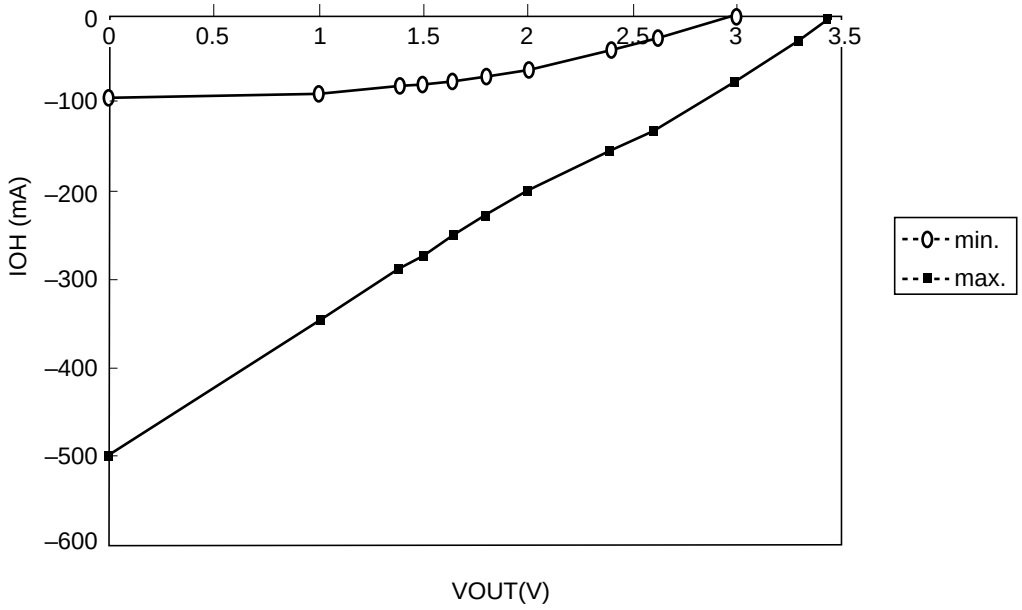
| VOUT (V) | IOL min. (mA) | IOL max. (mA) |
|---|---|---|
| 0 | 0 | 0 |
| 0.4 | 27 | 71 |
| 0.65 | 41 | 108 |
| 0.85 | 51 | 134 |
| 1 | 58 | 151 |
| 1.4 | 70 | 188 |
| 1.5 | 72 | 194 |
| 1.65 | 75 | 203 |
| 1.8 | 77 | 209 |
| 1.95 | 77 | 212 |
| 3 | 80 | 220 |
| 3.45 | 81 | 223 |




**Output Low Current (IOL)**

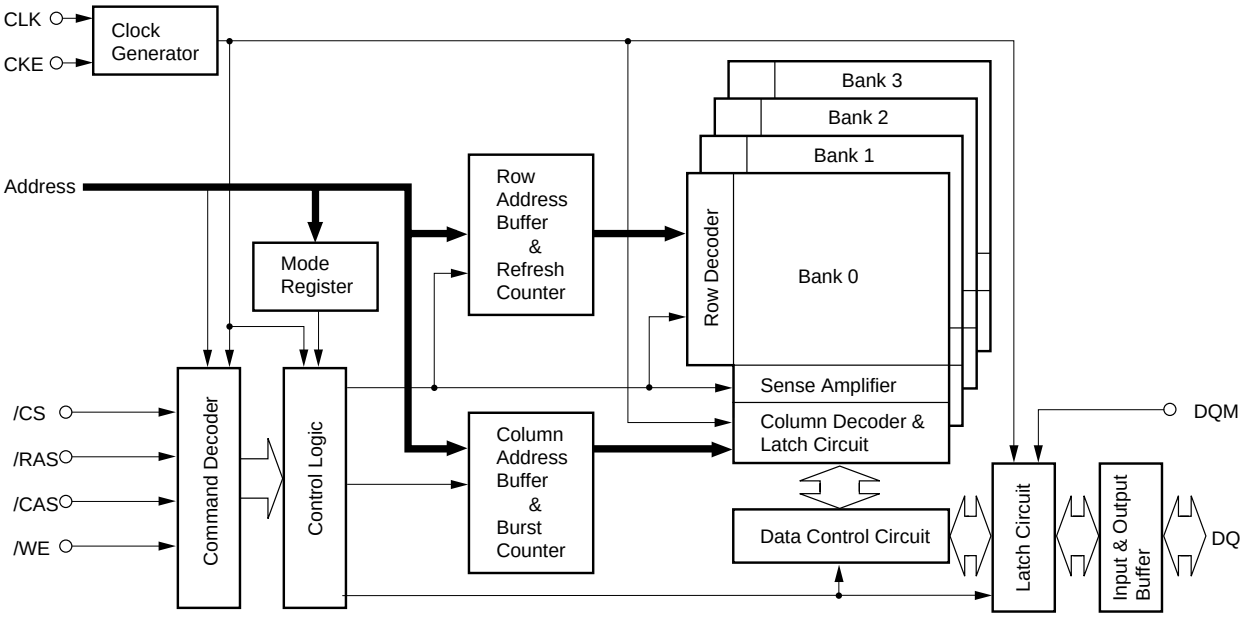
**[Output High Current (IOH)]**

| | IOH | IOH |
|---|---|---|
| VOUT (V) | min. (mA) | max. (mA) |
| 3.45 | — | –3 |
| 3.3 | — | –28 |
| 3 | 0 | –75 |
| 2.6 | –21 | –130 |
| 2.4 | –34 | –154 |
| 2 | –59 | –197 |
| 1.8 | –67 | –227 |
| 1.65 | –73 | –248 |
| 1.5 | –78 | –270 |
| 1.4 | –81 | –285 |
| 1 | –89 | –345 |
| 0 | –93 | –503 |




**Output High Current (IOH)**

## Block Diagram



## Pin Function

### CLK (input pin)

CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

### /CS (input pin)

When /CS is Low, the command input cycle becomes valid. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

### /RAS, /CAS, and /WE (input pins)

Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

### A0 toA12 (input pins)

Row address (AX0 to AX12) is determined by A0 to A12 at the bank active command cycle CLK rising edge. Column address is determined by A0 to A8, A9 or A11 (see Address Pins Table) at the read or write command cycle CLK rising edge. And this column address becomes burst access start address.

**[Address Pins Table]**

| | Address (A0 to A12) | |
|---|---|---|
| Part number | Row address | Column address |
| EDS2504AP | AX0 to AX12 | AY0 to AY9, AY11 |
| EDS2508AP | AX0 to AX12 | AY0 to AY9 |
| EDS2516AP | AX0 to AX12 | AY0 to AY8 |

A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 and BA1 (BS) is precharged. For details refer to the command operation section.

### BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal (BS). (See Bank Select Signal Table)

**[Bank Select Signal Table]**

| | BA0 | BA1 |
|---|---|---|
| Bank 0 | L | L |
| Bank 1 | H | L |
| Bank 2 | L | H |
| Bank 3 | H | H |

Remark: H: VIH. L: VIL. ×: VIH or VIL

### CKE (input pin)

This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down mode, clock suspend mode and self refresh mode.

**DQM, UDQM and LDQM (input pins)**

DQM controls input/output buffers. In 16M × 16 products, UDQM and LDQM control upper byte (DQ8 to DQ15) and lower byte (DQ0 to DQ7).

Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. (The latency of DQM during reading is 2 clocks.)

Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written. (The latency of DQM during writing is 0 clock.)

**DQ0 toDQ15 (input/output pins)**

Data is input to and output from these pins (DQ0 to DQ3; EDS2504AP , DQ0 to DQ7; EDS2508AP, DQ0 to DQ15; EDS2516AP).

**VDD, VSS, VDDQ, VSSQ (Power supply)**

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

## Command Operation

### Command Truth Table

The SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

| | | CKE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Function | Symbol | n – 1 | n | /CS | /RAS | /CAS | /WE | BA1,BA0 | A10 | A0 to A12 |
| Device deselect | DESL | H | × | H | × | × | × | × | × | × |
| No operation | NOP | H | × | L | H | H | H | × | × | × |
| Burst stop | BST | H | × | L | H | H | L | × | × | × |
| Read | READ | H | × | L | H | L | H | V | L | V |
| Read with auto precharge | READA | H | × | L | H | L | H | V | H | V |
| Write | WRIT | H | × | L | H | L | L | V | L | V |
| Write with auto precharge | WRITA | H | × | L | H | L | L | V | H | V |
| Bank activate | ACT | H | × | L | L | H | H | V | V | V |
| Precharge select bank | PRE | H | × | L | L | H | L | V | L | × |
| Precharge all banks | PALL | H | × | L | L | H | L | × | H | × |
| Mode register set | MRS | H | × | L | L | L | L | L | L | V |

Remark: H: VIH. L: VIL. ×: VIH or VIL

#### Device deselect command [DESL]

When this command is set (/CS is High), the SDRAM ignore command input at the clock. However, the internal status is held.

#### No operation [NOP]

This command is not an execution command. However, the internal operations continue.

#### Burst stop command [BST]

This command can stop the current burst operation.

#### Column address strobe and read command [READ]

This command starts a read operation. In addition, the start address of burst read is determined by the column address (see Address Pins Table in Pin Function) and the bank select address. After the read operation, the output buffer becomes High-Z.

#### Read with auto-precharge [READA]

This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8.

#### Column address strobe and write command [WRIT]

This command starts a write operation. When the burst write mode is selected, the column address (see Address Pins Table in Pin Function) and the bank select address (BA0, BA1) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (see Address Pins Table in Pin Function) and the bank select address (BA0, BA1).

#### Write with auto-precharge [WRITA]

This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation.

**Row address strobe and bank activate [ACT]**

This command activates the bank that is selected by BA0, BA1 and determines the row address (AX0 to AX12). (See Bank Select Signal Table)

**Precharge selected bank [PRE]**

This command starts precharge operation for the bank selected by BA0, BA1. (See Bank Select Signal Table)

**[Bank Select Signal Table]**

| | BA0 | BA1 |
|---|---|---|
| Bank 0 | L | L |
| Bank 1 | H | L |
| Bank 2 | L | H |
| Bank 3 | H | H |

Remark: H: VIH. L: VIL. ×: VIH or VIL

**Precharge all banks [PALL]**

This command starts a precharge operation for all banks.

**Refresh [REF/SELF]**

This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

**Mode register set [MRS]**

The SDRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to BA0 and BA1) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

**DQM Truth Table**

| | | CKE | | DQM | |
|---|---|---|---|---|---|
| Commands | Symbol | n – 1 | n | UDQM | LDQM |
| Write enable/output enable | ENB | H | × | L | |
| Write inhibit/output disable | MASK | H | × | H | |
| Upper byte write enable/output enable | ENBU | H | × | L | × |
| Lower byte write enable/output enable | ENBL | H | × | × | L |
| Upper byte write inhibit/output disable | MASKU | H | × | H | × |
| Lower byte write inhibit/output disable | MASKL | H | × | × | H |

Remark: H: VIH. L: VIL. ×: VIH or VIL
Write: IDID is needed.
Read: IDOD is needed.

**CKE Truth Table**

| | | | CKE | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Current state | Function | Symbol | n – 1 | n | /CS | /RAS | /CAS | /WE | Address |
| Activating | Clock suspend mode entry | | H | L | × | × | × | × | × |
| Any | Clock suspend mode | | L | L | × | × | × | × | × |
| Clock suspend | Clock suspend mode exit | | L | H | × | × | × | × | × |
| Idle | CBR (auto) refresh command | REF | H | H | L | L | L | H | × |
| Idle | Self refresh entry | SELF | H | L | L | L | L | H | × |
| Self refresh | Self refresh exit | | L | H | L | H | H | H | × |
| | | | L | H | H | × | × | × | × |
| Idle | Power down entry | | H | L | L | H | H | H | × |
| | | | H | L | H | × | × | × | × |
| Power down | Power down exit | | L | H | H | × | × | × | × |
| | | | L | H | L | H | H | H | × |

Remark: H: VIH. L: VIL. ×: VIH or VIL

**Function Truth Table**

The following table shows the operations that are performed when each command is issued in each mode of the SDRAM.

The following table assumes that CKE is high.

| Current state | /CS | /RAS | /CAS | /WE | Address | Command | Operation |
|---|---|---|---|---|---|---|---|
| Precharge | H | × | × | × | × | DESL | Enter IDLE after tRP |
| | L | H | H | H | × | NOP | Enter IDLE after tRP |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL*3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL*3 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*3 |
| | L | L | H | L | BA, A10 | PRE, PALL | NOP*5 |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Idle | H | × | × | × | × | DESL | NOP |
| | L | H | H | H | × | NOP | NOP |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL*4 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL*4 |
| | L | L | H | H | BA, RA | ACT | Bank and row active |
| | L | L | H | L | BA, A10 | PRE, PALL | NOP |
| | L | L | L | H | × | REF, SELF | Refresh |
| | L | L | L | L | MODE | MRS | Mode register set*8 |
| Row active | H | × | × | × | × | DESL | NOP |
| | L | H | H | H | × | NOP | NOP |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | Begin read*6 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | Begin write*6 |
| | L | L | H | H | BA, RA | ACT | Other bank active<br>ILLEGAL on same bank*2 |
| | L | L | H | L | BA, A10 | PRE, PALL | Precharge*7 |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Read | H | × | × | × | × | DESL | Continue burst to end |
| | L | H | H | H | × | NOP | Continue burst to end |
| | L | H | H | L | × | BST | Burst stop |
| | L | H | L | H | BA, CA, A10 | READ/READA | Continue burst read to /CAS latency and New read |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | Term burst read/start write |
| | L | L | H | H | BA, RA | ACT | Other bank active<br>ILLEGAL on same bank*2 |
| | L | L | H | L | BA, A10 | PRE, PALL | Term burst read and Precharge |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |

| Current state | /CS | /RAS | /CAS | /WE | Address | Command | Operation |
|---|---|---|---|---|---|---|---|
| Read with auto-precharge | H | × | × | × | × | DESL | Continue burst to end and precharge |
| | L | H | H | H | × | NOP | Continue burst to end and precharge |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL*3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL*3 |
| | L | L | H | H | BA, RA | ACT | Other bank active<br>ILLEGAL on same bank*2 |
| | L | L | H | L | BA, A10 | PRE, PALL | ILLEGAL*3 |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Write | H | × | × | × | × | DESL | Continue burst to end |
| | L | H | H | H | × | NOP | Continue burst to end |
| | L | H | H | L | × | BST | Burst stop |
| | L | H | L | H | BA, CA, A10 | READ/READA | Term burst and New read |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | Term burst and New write |
| | L | L | H | H | BA, RA | ACT | Other bank active<br>ILLEGAL on same bank*3 |
| | L | L | H | L | BA, A10 | PRE, PALL | Term burst write and Precharge*1 |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Write with auto-precharge | H | × | × | × | × | DESL | Continue burst to end and precharge |
| | L | H | H | H | × | NOP | Continue burst to end and precharge |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL*3 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL*3 |
| | L | L | H | H | BA, RA | ACT | Other bank active<br>ILLEGAL on same bank*3 |
| | L | L | H | L | BA, A10 | PRE, PALL | ILLEGAL*3 |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |
| Refresh (auto-refresh) | H | × | × | × | × | DESL | Enter IDLE after tRC |
| | L | H | H | H | × | NOP | Enter IDLE after tRC |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL*4 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL*4 |
| | L | L | H | H | BA, RA | ACT | ILLEGAL*4 |
| | L | L | H | L | BA, A10 | PRE, PALL | ILLEGAL*4 |
| | L | L | L | H | × | REF, SELF | ILLEGAL |
| | L | L | L | L | MODE | MRS | ILLEGAL |

| Current state | /CS | /RAS | /CAS | /WE | Address | Command | Operation |
|---|---|---|---|---|---|---|---|
| Mode register set | H | × | × | × | × | DESL | NOP |
| | L | H | H | H | × | NOP | NOP |
| | L | H | H | L | × | BST | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | ILLEGAL*4 |
| | L | H | L | L | BA, CA, A10 | WRIT/WRITA | ILLEGAL*4 |
| | L | L | H | H | BA, RA | ACT | Bank and row active*9 |
| | L | L | H | L | BA, A10 | PRE, PALL | NOP |
| | L | L | L | H | × | REF, SELF | Refresh*9 |
| | L | L | L | L | MODE | MRS | Mode register set*8 |

Remark: H: VIH. L: VIL. ×: VIH or VIL

Notes: 1.An interval of tDPL is required between the final valid data input and the precharge command.

2. If tRRD is not satisfied, this operation is illegal.
3. Illegal for same bank, except for another bank.
4. Illegal for all banks.
5. NOP for same bank, except for another bank.
6. Illegal if tRCD is not satisfied.
7. Illegal if tRAS is not satisfied.
8. MRS command must be issued after DOUT finished, in case of DOUT remaining.
9. Illegal if lMRD is not satisfied.

**Command Truth Table for CKE**

| | CKE | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Current State | n – 1 | n | /CS | /RAS | /CAS | /WE | Address | Operation | Notes |
| Self refresh | H | × | × | × | × | × | × | INVALID, CLK (n – 1) would exit self refresh | |
| | L | H | H | × | × | × | × | Self refresh recovery | |
| | L | H | L | H | H | × | × | Self refresh recovery | |
| | L | H | L | H | L | × | × | ILLEGAL | |
| | L | H | L | L | × | × | × | ILLEGAL | |
| | L | L | × | × | × | × | × | Continue self refresh | |
| Self refresh recovery | H | H | H | × | × | × | × | Idle after $t_{RC}$ | |
| | H | H | L | H | H | × | × | Idle after $t_{RC}$ | |
| | H | H | L | H | L | × | × | ILLEGAL | |
| | H | H | L | L | × | × | × | ILLEGAL | |
| | H | L | H | × | × | × | × | ILLEGAL | |
| | H | L | L | H | H | × | × | ILLEGAL | |
| | H | L | L | H | L | × | × | ILLEGAL | |
| | H | L | L | L | × | × | × | ILLEGAL | |
| Power down | H | × | × | × | × | × | | INVALID, CLK (n – 1) would exit power down | |
| | L | H | H | × | × | × | × | EXIT power down | |
| | L | H | L | H | H | H | × | EXIT power down | |
| | L | L | × | × | × | × | × | Continue power down mode | |
| All banks idle | H | H | H | × | × | × | | Refer to operations in Function Truth Table | |
| | H | H | L | H | × | × | | Refer to operations in Function Truth Table | |
| | H | H | L | L | H | × | | Refer to operations in Function Truth Table | |
| | H | H | L | L | L | H | × | CBR (auto) Refresh | |
| | H | H | L | L | L | L | OPCODE | Refer to operations in Function Truth Table | |
| | H | L | H | × | × | × | | Begin power down next cycle | |
| | H | L | L | H | × | × | | Refer to operations in Function Truth Table | |
| | H | L | L | L | H | × | | Refer to operations in Function Truth Table | |
| | H | L | L | L | L | H | × | Self refresh | 1 |
| | H | L | L | L | L | L | OPCODE | Refer to operations in Function Truth Table | |
| | L | H | × | × | × | × | × | Exit power down next cycle | |
| | L | L | × | × | × | × | × | Power down | 1 |
| Row active | H | × | × | × | × | × | × | Refer to operations in Function Truth Table | |
| | L | × | × | × | × | × | × | Clock suspend | 1 |
| Any state other than | H | H | × | × | × | × | | Refer to operations in Function Truth Table | |
| listed above | H | L | × | × | × | × | × | Begin clock suspend next cycle | 2 |
| | L | H | × | × | × | × | × | Exit clock suspend next cycle | |
| | L | L | × | × | × | × | × | Maintain clock suspend | |

Remark: H: VIH. L: VIL. ×: VIH or VIL

Notes: 1. Self refresh can be entered only from the all banks idle state. Power down can be entered only from all banks idle. Clock suspend can be entered only from following states, row active, read, read with auto-precharge, write and write with auto precharge.

2. Must be legal command as defined in Function Truth Table.

**Clock suspend mode entry**

The SDRAM enters clock suspend mode from active mode by setting CKE to Low. If command is input in the clock suspend mode entry cycle, the command is valid. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

**ACTIVE clock suspend**

This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

**READ suspend and READ with Auto-precharge suspend**

The data being output is held (and continues to be output).

**WRITE suspend and WRIT with Auto-precharge suspend**

In this mode, external signals are not accepted. However, the internal state is held.

**Clock suspend**

During clock suspend mode, keep the CKE to Low.

**Clock suspend mode exit**

The SDRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

**IDLE**

In this state, all banks are not selected, and completed precharge operation.

**Auto-refresh command [REF]**

When this command is input from the IDLE state, the SDRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the SDRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 8192 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

**Self-refresh entry [SELF]**

When this command is input during the IDLE state, the SDRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

**Power down mode entry**

When this command is executed during the IDLE state, the SDRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

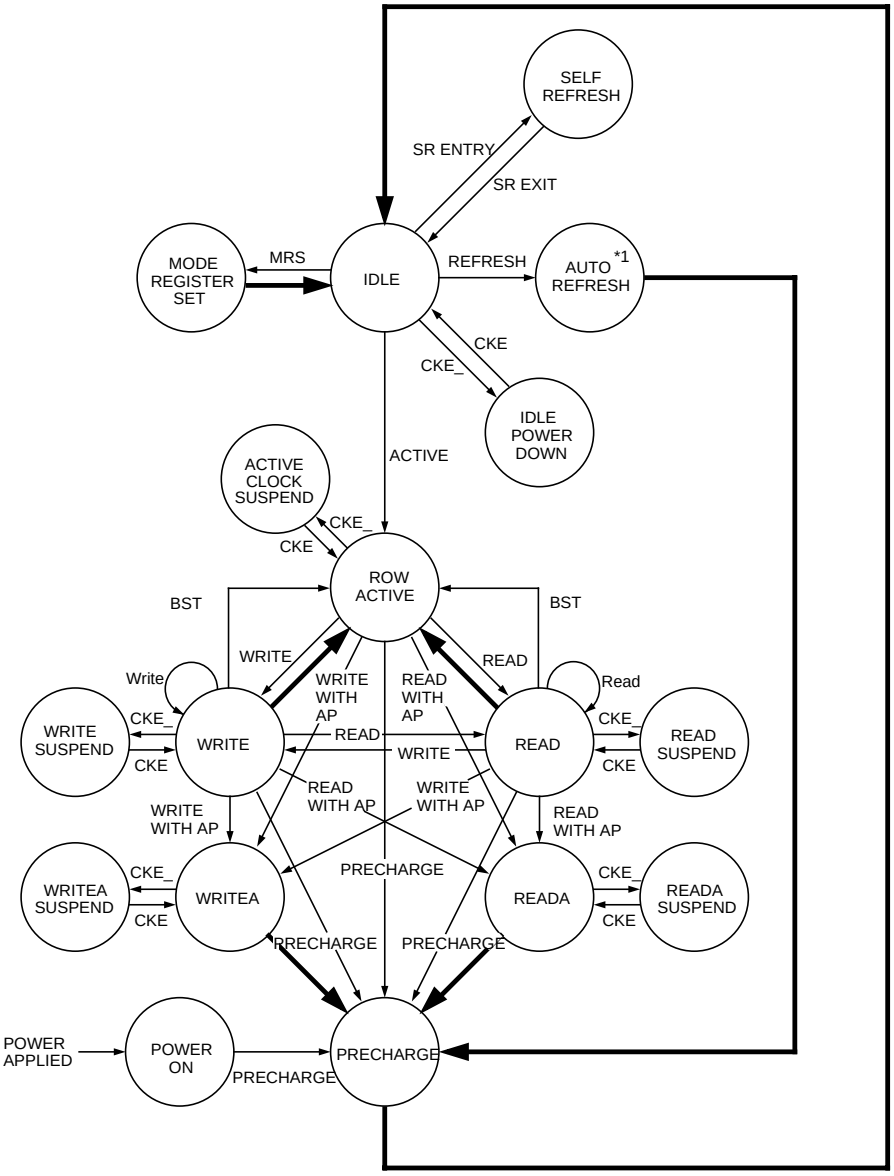
**Self-refresh exit**

When this command is executed during self-refresh mode, the SDRAM can exit from self-refresh mode. After exiting from self-refresh mode, the SDRAM enters the IDLE state.

**Power down exit**

When this command is executed at the power down mode, the SDRAM can exit from power down mode. After exiting from power down mode, the SDRAM enters the IDLE state.

**Simplified State Diagram**




Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

### Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A12, BA0 and BA1) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

BA1, BA0, A8, A9, A10, A11, A12: (OPCODE): The SDRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and burst write: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

Burst read and single write: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle. If this pin is high, the vender test mode is set.

A6, A5, A4: (LMODE): These pins specify the /CAS latency.

A3: (BT): A burst type is specified.

A2, A1, A0: (BL): These pins specify the burst length.

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPCODE | | | | | | | 0 | LMODE | | | BT | BL | | |

| A6 | A5 | A4 | CAS latency |
|---|---|---|---|
| 0 | 0 | 0 | R |
| 0 | 0 | 1 | R |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | X | X | R |

| A3 | Burst type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A2 | A1 | A0 | Burst length | |
|---|---|---|---|---|
| | | | BT=0 | BT=1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | R | R |
| 1 | 0 | 1 | R | R |
| 1 | 1 | 0 | R | R |
| 1 | 1 | 1 | R | R |

| BA1 | BA0 | A12 | A11 | A10 | A9 | A8 | Write mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Burst read and burst write |
| X | X | X | X | X | 0 | 1 | R |
| X | X | X | X | X | 1 | 0 | Burst read and single write |
| X | X | X | X | X | 1 | 1 | R |

R is Reserved (inhibit)
X: 0 or 1

**Mode Register Set Timing**

Burst length = 2

| Starting Ad. | Addressing(decimal) | |
|---|---|---|
| A0 | Sequential | Interleave |
| 0 | 0, 1, | 0, 1, |
| 1 | 1, 0, | 1, 0, |

Burst length = 4

| Starting Ad. | | Addressing(decimal) | |
|---|---|---|---|
| A1 | A0 | Sequential | Interleave |
| 0 | 0 | 0, 1, 2, 3, | 0, 1, 2, 3, |
| 0 | 1 | 1, 2, 3, 0, | 1, 0, 3, 2, |
| 1 | 0 | 2, 3, 0, 1, | 2, 3, 0, 1, |
| 1 | 1 | 3, 0, 1, 2, | 3, 2, 1, 0, |

Burst length = 8

| Starting Ad. | | | Addressing(decimal) | |
|---|---|---|---|---|
| A2 | A1 | A0 | Sequential | Interleave |
| 0 | 0 | 0 | 0, 1, 2, 3, 4, 5, 6, 7, | 0, 1, 2, 3, 4, 5, 6, 7, |
| 0 | 0 | 1 | 1, 2, 3, 4, 5, 6, 7, 0, | 1, 0, 3, 2, 5, 4, 7, 6, |
| 0 | 1 | 0 | 2, 3, 4, 5, 6, 7, 0, 1, | 2, 3, 0, 1, 6, 7, 4, 5, |
| 0 | 1 | 1 | 3, 4, 5, 6, 7, 0, 1, 2, | 3, 2, 1, 0, 7, 6, 5, 4, |
| 1 | 0 | 0 | 4, 5, 6, 7, 0, 1, 2, 3, | 4, 5, 6, 7, 0, 1, 2, 3, |
| 1 | 0 | 1 | 5, 6, 7, 0, 1, 2, 3, 4, | 5, 4, 7, 6, 1, 0, 3, 2, |
| 1 | 1 | 0 | 6, 7, 0, 1, 2, 3, 4, 5, | 6, 7, 4, 5, 2, 3, 0, 1, |
| 1 | 1 | 1 | 7, 0, 1, 2, 3, 4, 5, 6, | 7, 6, 5, 4, 3, 2, 1, 0, |

**Burst Sequence**

## Power-up sequence

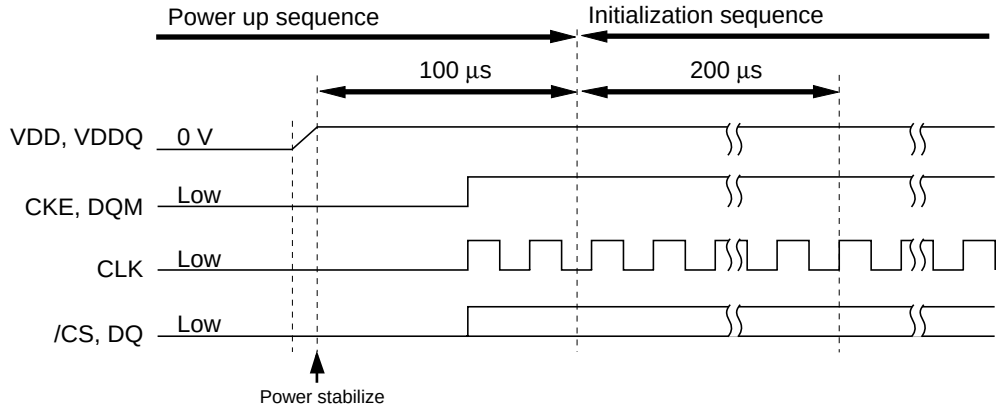
### Power-up sequence

The SDRAM should be goes on the following sequence with power up.

The CLK, CKE, /CS, DQM and DQ pins keep low till power stabilizes.
The CLK pin is stabilized within 100 µs after power stabilizes before the following initialization sequence.
The CKE and DQM is driven to high between power stabilizes and the initialization sequence.
This SDRAM has VDD clamp diodes for CLK, CKE, /CS DQM and DQ pins. If these pins go high before power up, the large current flows from these pins to VDD through the diodes.

### Initialization sequence

When 200 µs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After tRP delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQM and CKE to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.




**Power-up sequence and Initialization sequence**

## Operation of the SDRAM

### Read/Write Operations

#### Bank active

Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

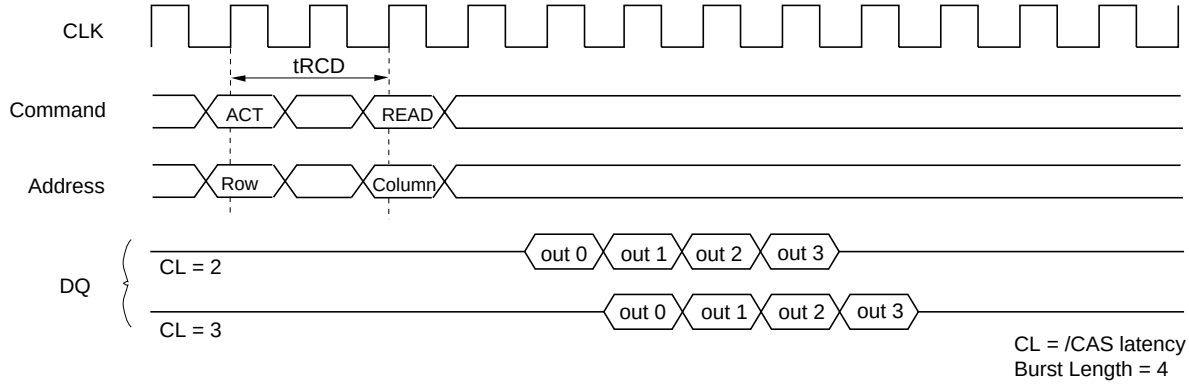
#### Read operation

A read operation starts when a read command is input. Output buffer becomes Low-Z in the (/CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.

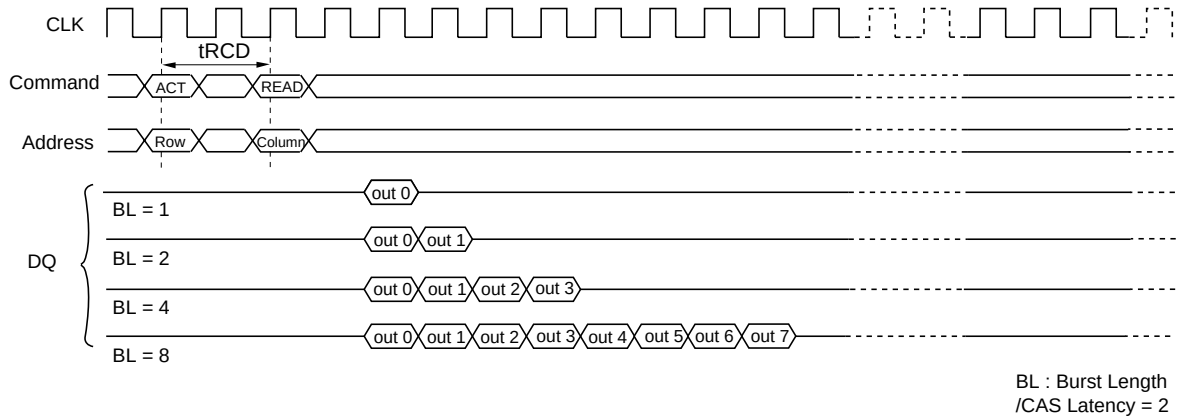
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the /CAS Latency. The /CAS Latency can be set to 2 or 3.

When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.

The /CAS latency and burst length must be specified at the mode register.




**/CAS Latency**

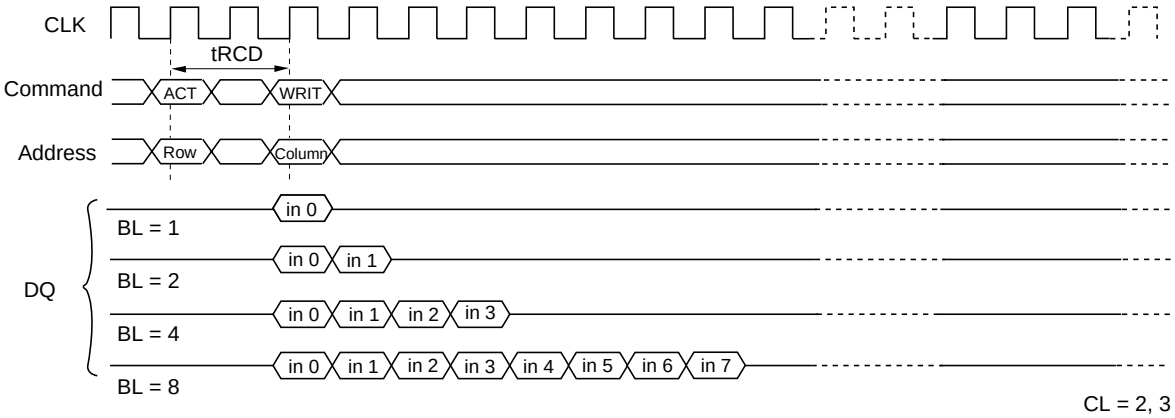



**Burst Length**

**Write operation**

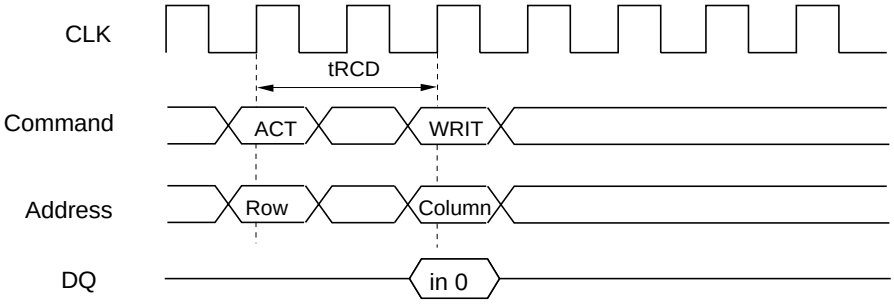
Burst write or single write mode is selected by the OPCODE of the mode register.

1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4 and 8, like burst read operations. The write start address is specified by the column address and the bank select address at the write command set cycle.




**Burst write**

2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock).




**Single write**

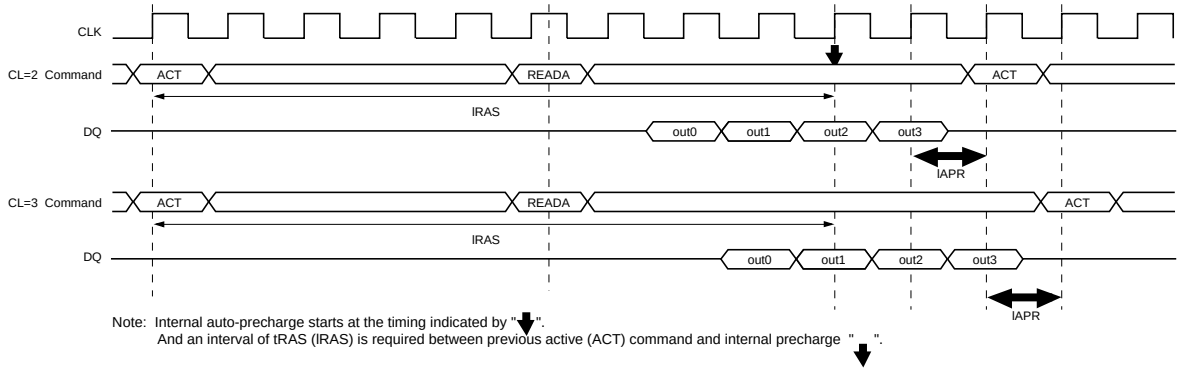
**Auto Precharge**

**Read with auto-precharge**

In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval defined by lAPR is required before execution of the next command.

**[Clock cycle time]**

| /CAS latency | Precharge start cycle |
|---|---|
| 3 | 2 cycle before the final data is output |
| 2 | 1 cycle before the final data is output |

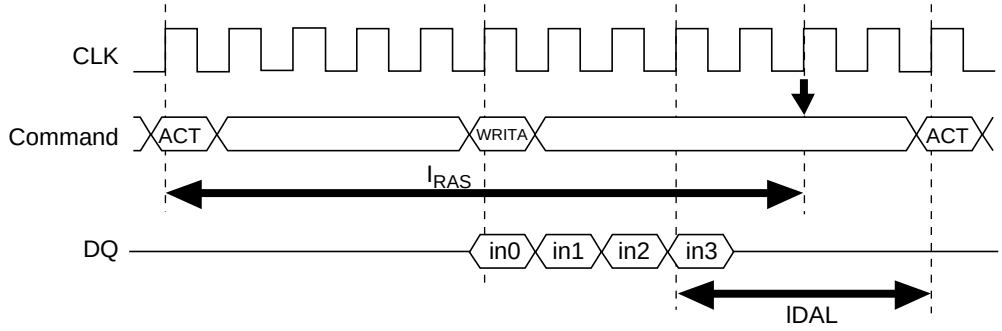



Note: Internal auto-precharge starts at the timing indicated by "↓".
And an interval of tRAS (lRAS) is required between previous active (ACT) command and internal precharge "↓".

**Burst Read (BL = 4)**

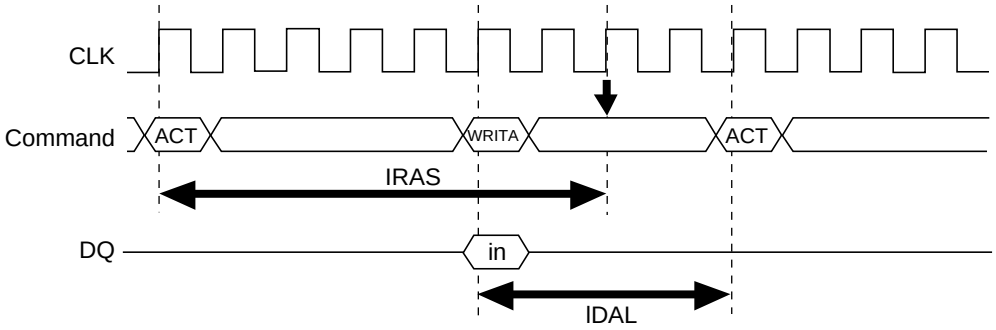
**Write with auto-precharge**

In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval of lDAL is required between the final valid data input and input of next command.




Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (lRAS) is required between previous active (ACT) command and internal precharge "↓".

**Burst Write (BL = 4)**

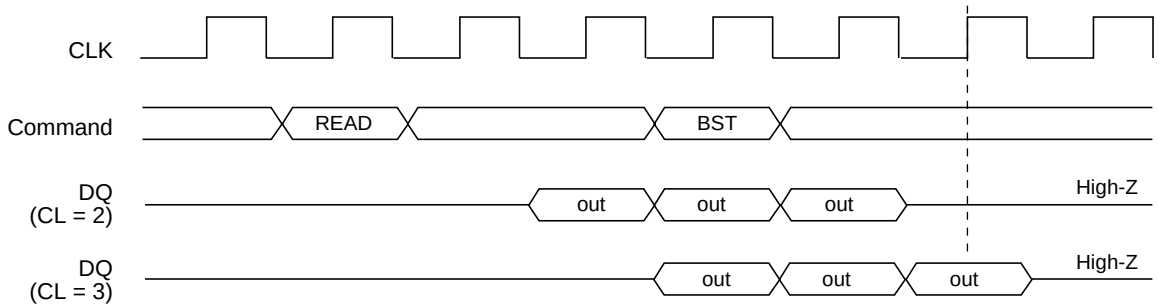



Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (lRAS) is required between previous active (ACT) command and internal precharge "↓".

**Single Write**

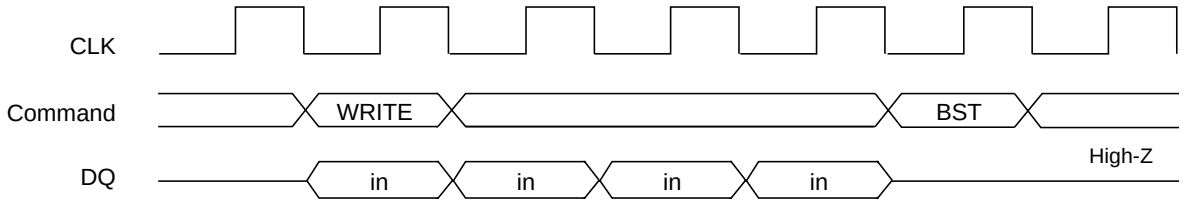
**Burst Stop Command**

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.




**Burst Stop at Read**

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.

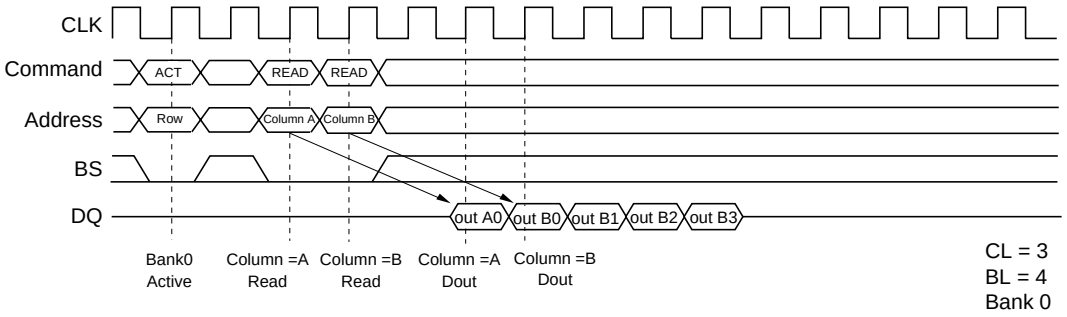



**Burst Stop at Write**

**Command Intervals**

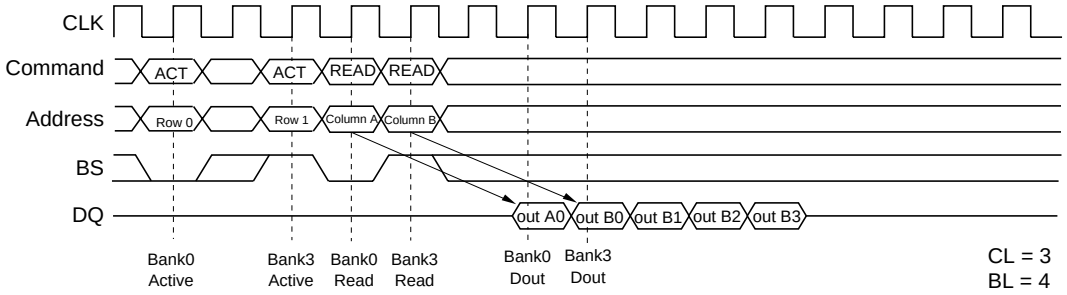
**Read command to Read command interval**

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.




**READ to READ Command Interval (same ROW address in same bank)**

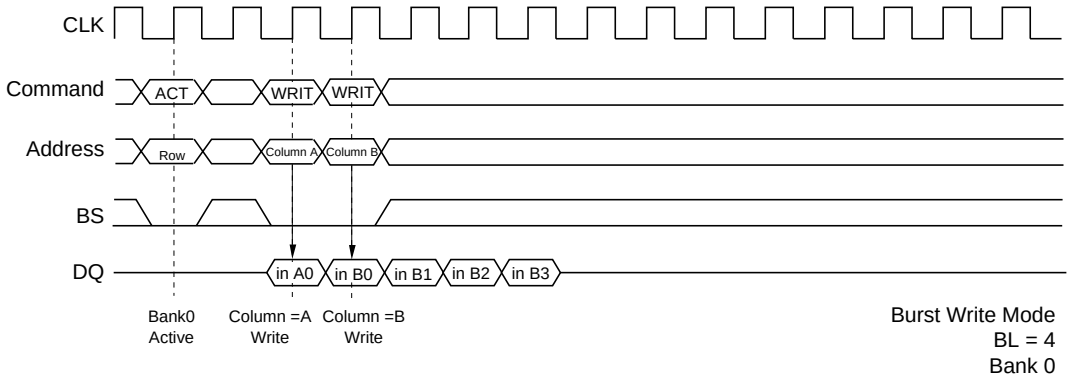
2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.




**READ to READ Command Interval (different bank)**

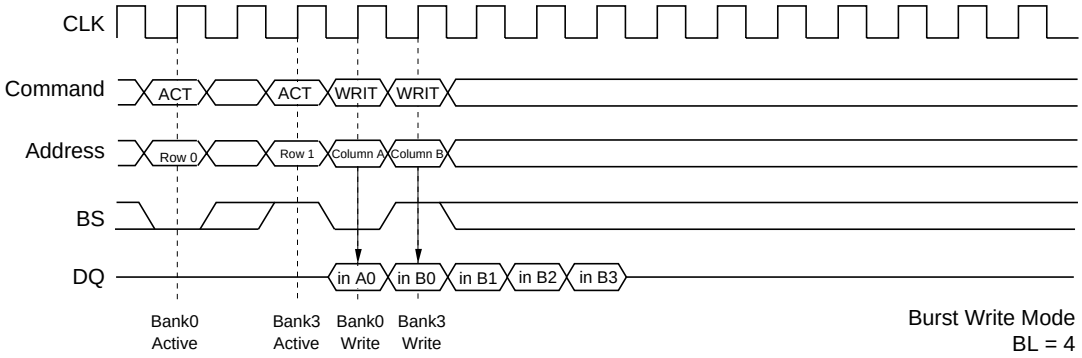
**Write command to Write command interval**

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.




**WRITE to WRITE Command Interval (same ROW address in same bank)**

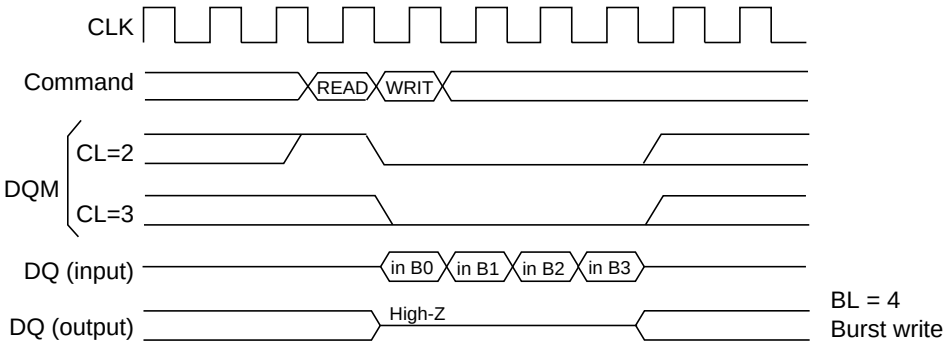
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.



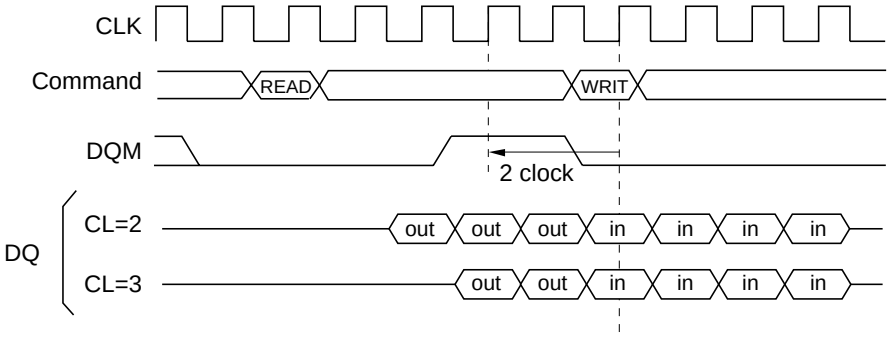

**WRITE to WRITE Command Interval (different bank)**

**Read command to Write command interval**

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQM must be set High so that the output buffer becomes High-Z before data input.




**READ to WRITE Command Interval (1)**

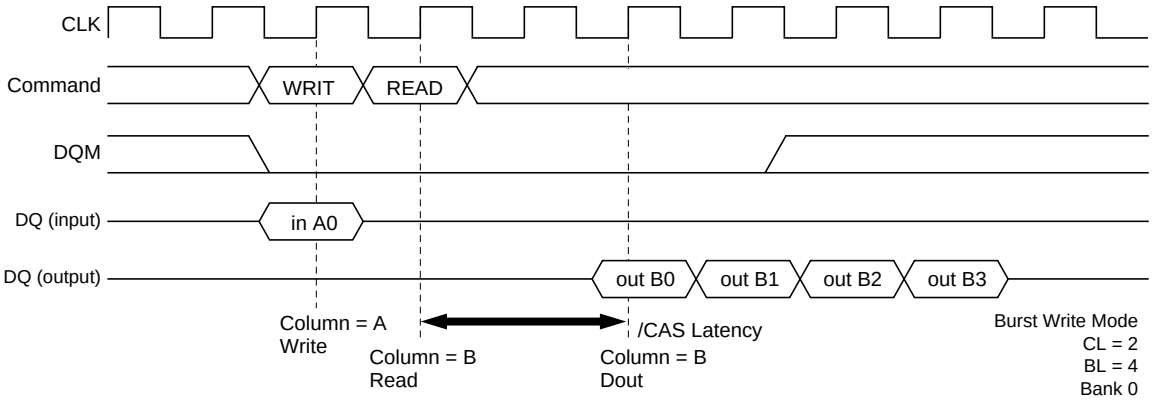



**READ to WRITE Command Interval (2)**

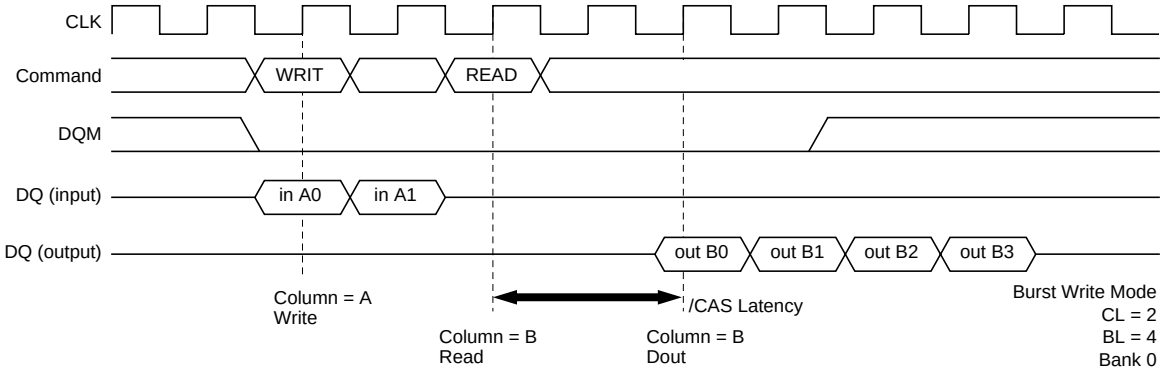
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

**Write command to Read command interval:**

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.




**WRITE to READ Command Interval (1)**

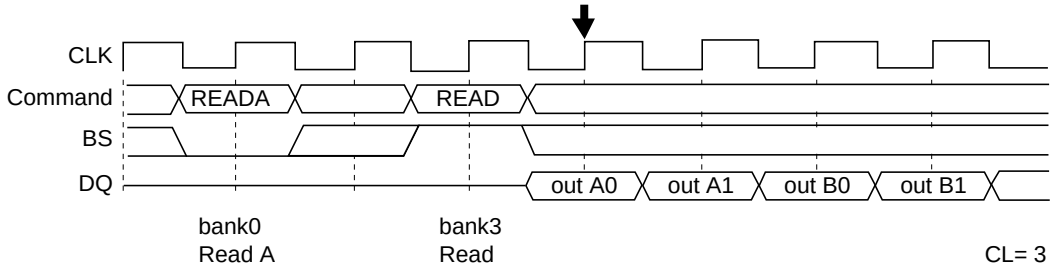



**WRITE to READ Command Interval (2)**

2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

**Read with auto precharge to Read command interval**

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the next clock of the second command.



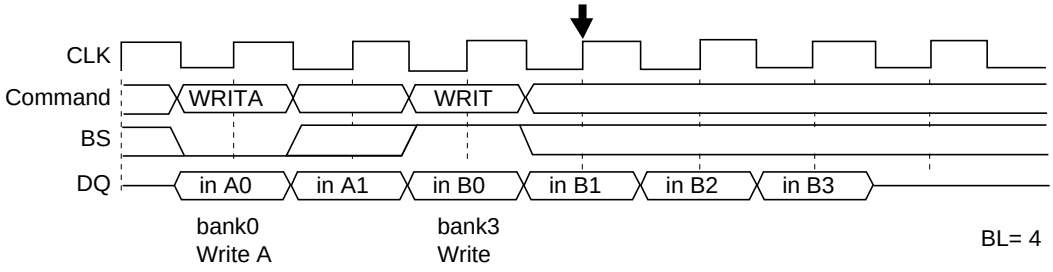

Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

**Read with Auto Precharge to Read Command Interval (Different bank)**

2. Same bank: The consecutive read command (the same bank) is illegal.

**Write with auto precharge to Write command interval**

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts 2 clocks later from the second command.



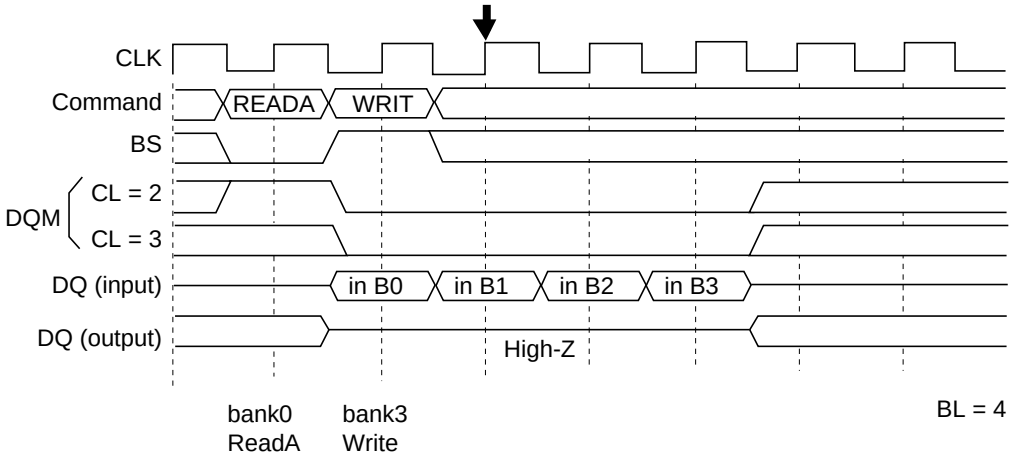

Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

**Write with Auto Precharge to Write Command Interval (Different bank)**

2. Same bank: The consecutive write command (the same bank) is illegal.

**Read with auto precharge to Write command interval**

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, DQM must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.



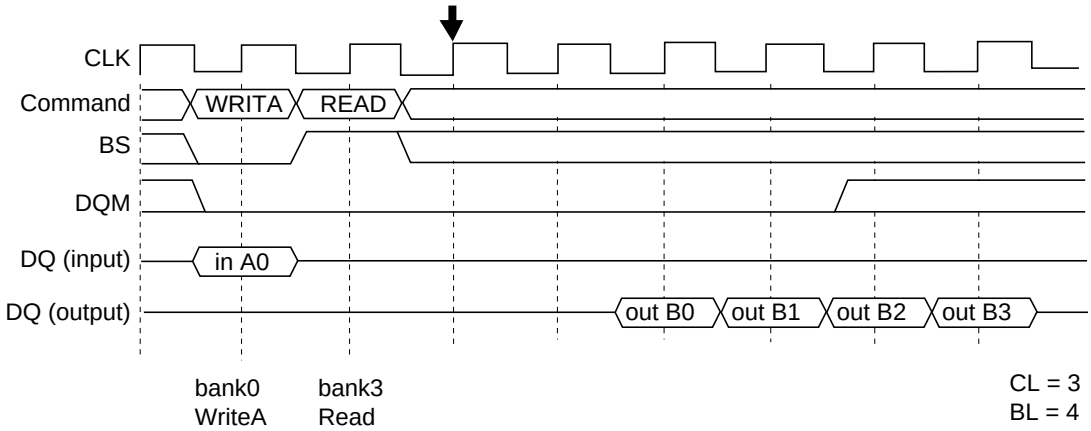

Note: Internal auto-precharge starts at the timing indicated by " ⬇ ".

**Read with Auto Precharge to Write Command Interval (Different bank)**

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

**Write with auto precharge to Read command interval**

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at 2 clocks later from the second command.



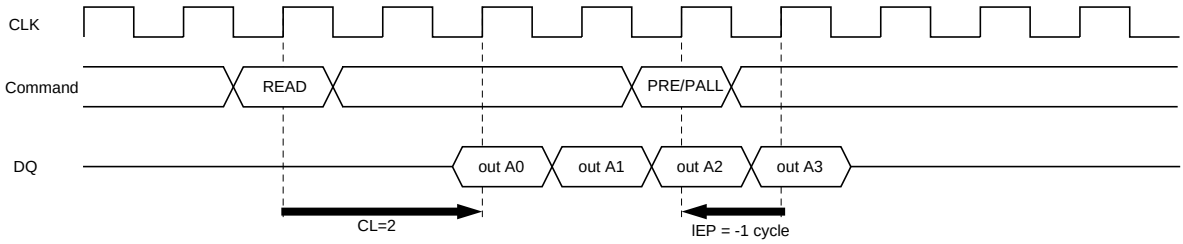

Note: Internal auto-precharge starts at the timing indicated by " ⬇ ".

**Write with Auto Precharge to Read Command Interval (Different bank)**

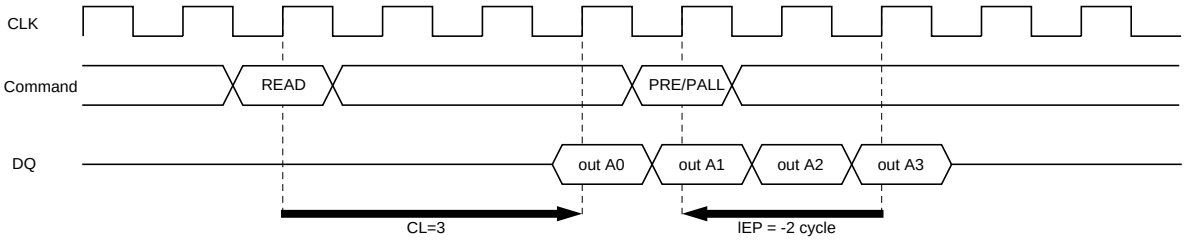
2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

**Read command to Precharge command interval (same bank)**

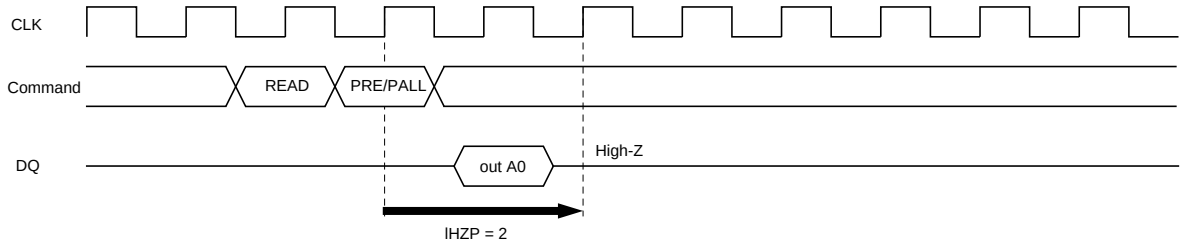
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by lHZP, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by lEP must be assured as an interval from the final data output to precharge command execution.



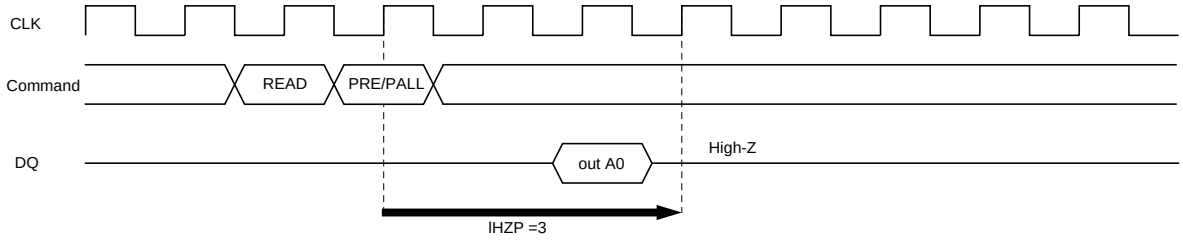

**READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2, BL = 4)**




**READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)**



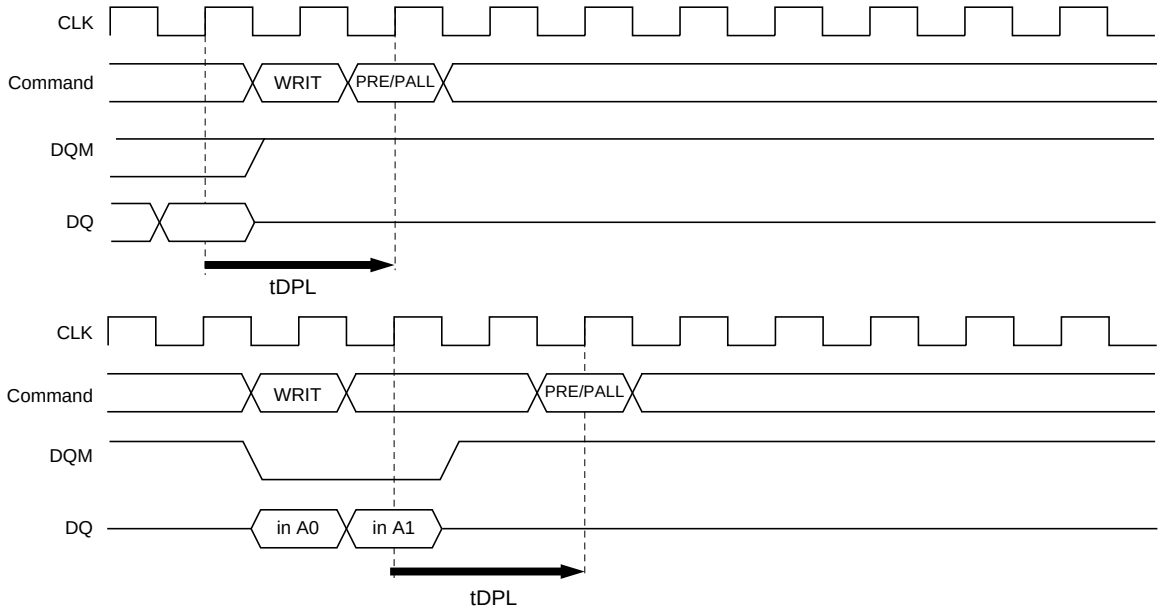

**READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2, BL = 1, 2, 4, 8)**



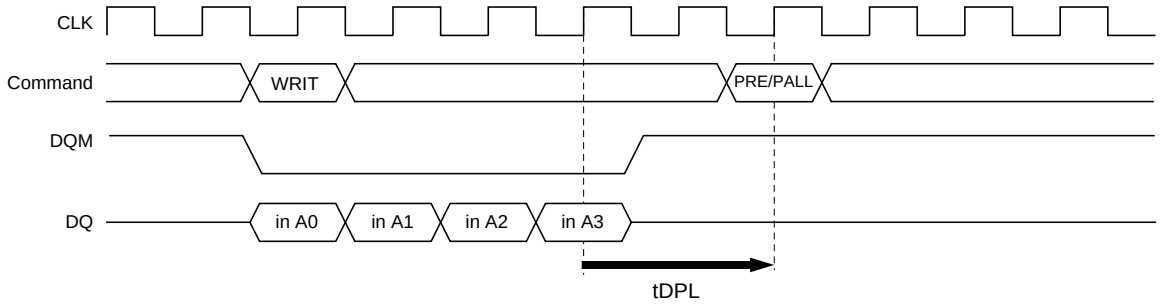

**READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 1, 2, 4, 8)**

**Write command to Precharge command interval (same bank)**

When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the clock defined by tDPL.



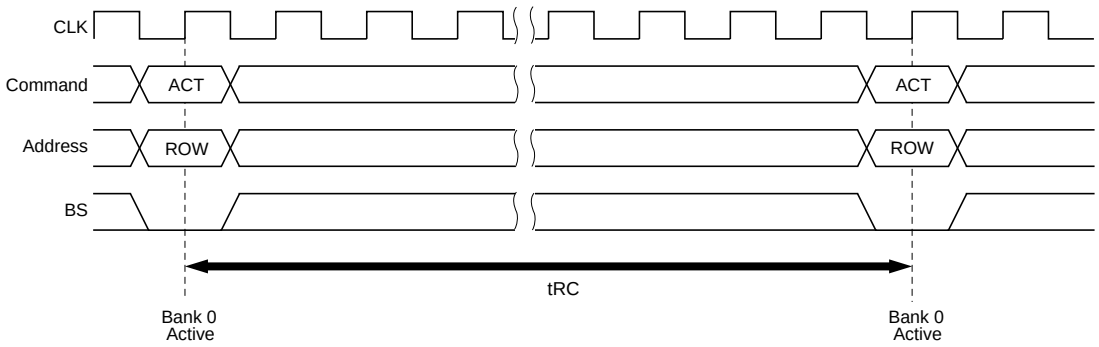

**WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To stop write operation))**



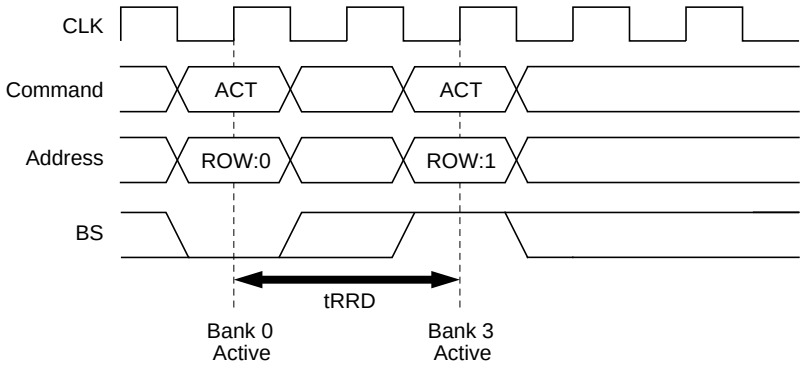

**WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To write all data))**

**Bank active command interval**

1. Same bank: The interval between the two bank active commands must be no less than tRC.
2. In the case of different bank active commands: The interval between the two bank active commands must be no less than tRRD.



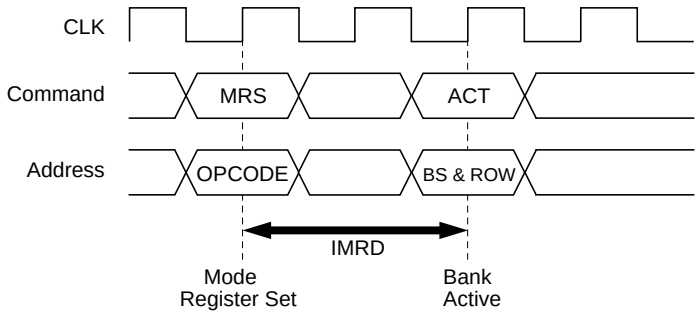

**Bank Active to Bank Active for Same Bank**




**Bank Active to Bank Active for Different Bank**

**Mode register set to Bank active command interval**

The interval between setting the mode register and executing a bank active command must be no less than IMRD.




**Mode register set to Bank active command interval**

**DQM Control**

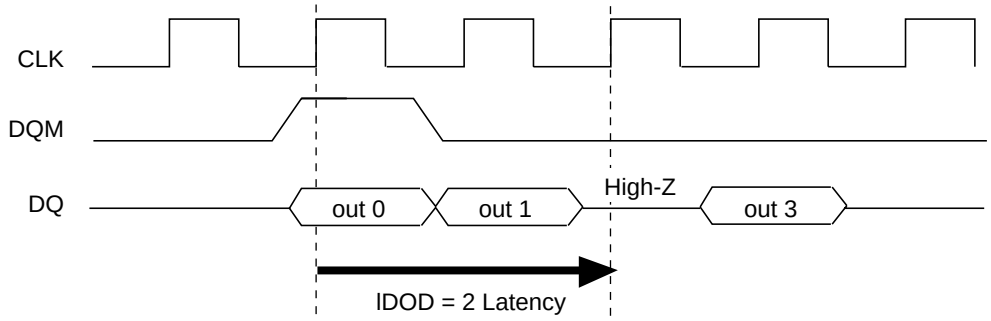
The DQM mask the DQ data. The UDQM and LDQM mask the upper and lower bytes of the DQ data, respectively. The timing of UDQM/LDQM is different during reading and writing.

**Reading**

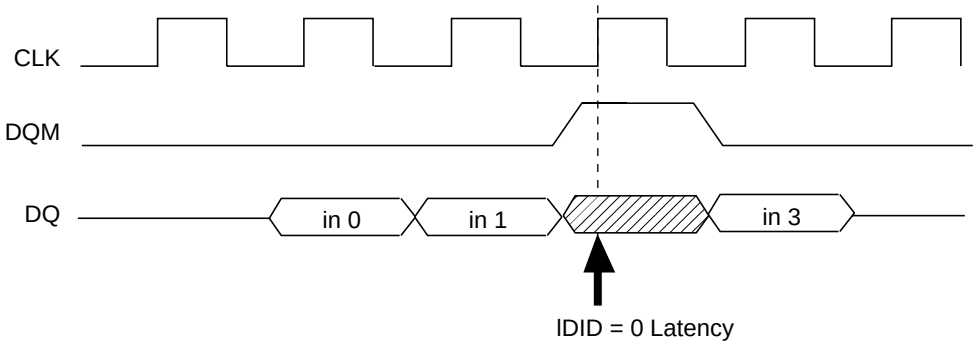
When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2 clocks.

**Writing**

Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0 clock.




**Reading**




**Writing**

**Refresh**

**Auto-refresh**

All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycles are required to refresh all the ROW addresses within tREF (max.). The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

**Self-refresh**

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF (max.) period on the condition 1 and 2 below.

1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below*after exiting from self-refresh mode.

Note: tREF (max.) / refresh cycles.

**Others**

**Power-down mode**

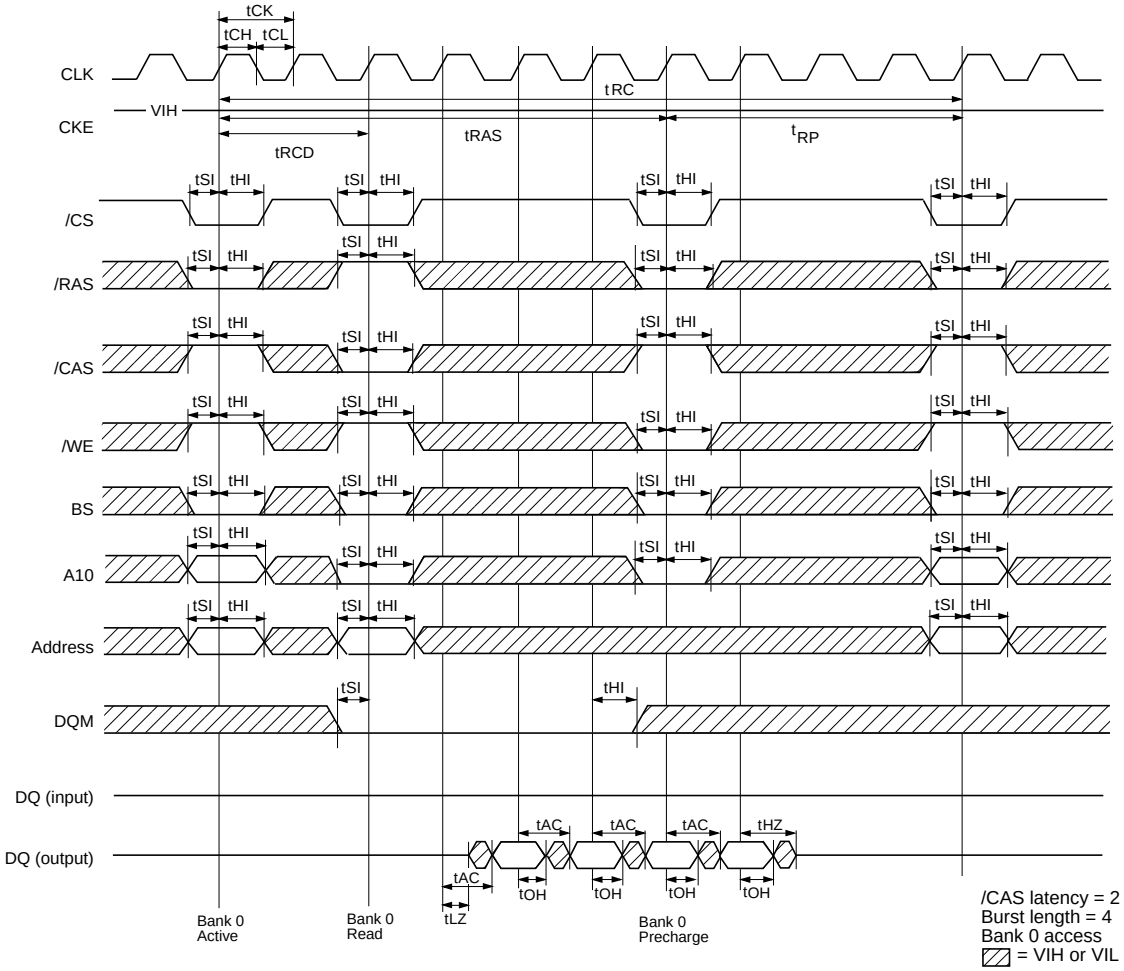
The SDRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

**Clock suspend mode**

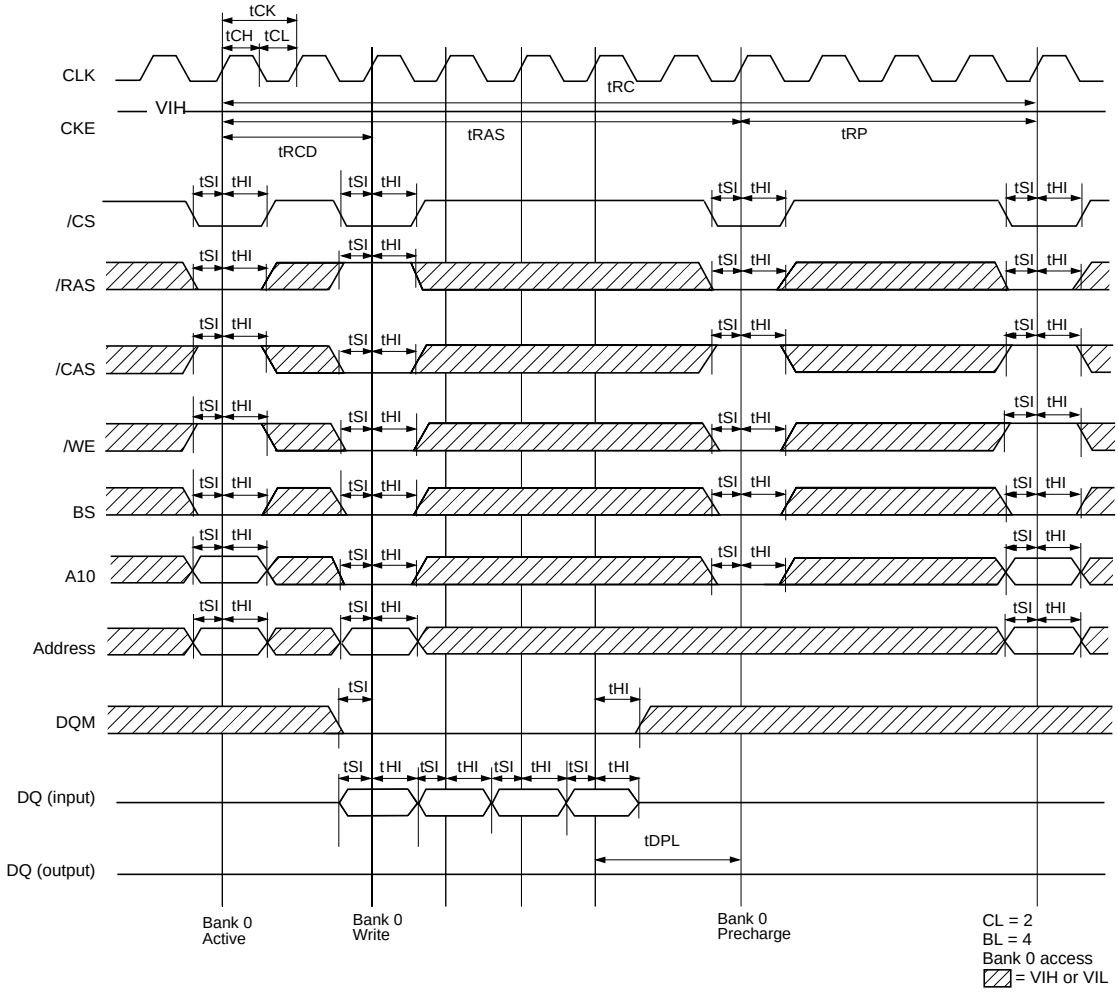
By driving CKE to Low during a bank active or read/write operation, the SDRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

## Timing Waveforms

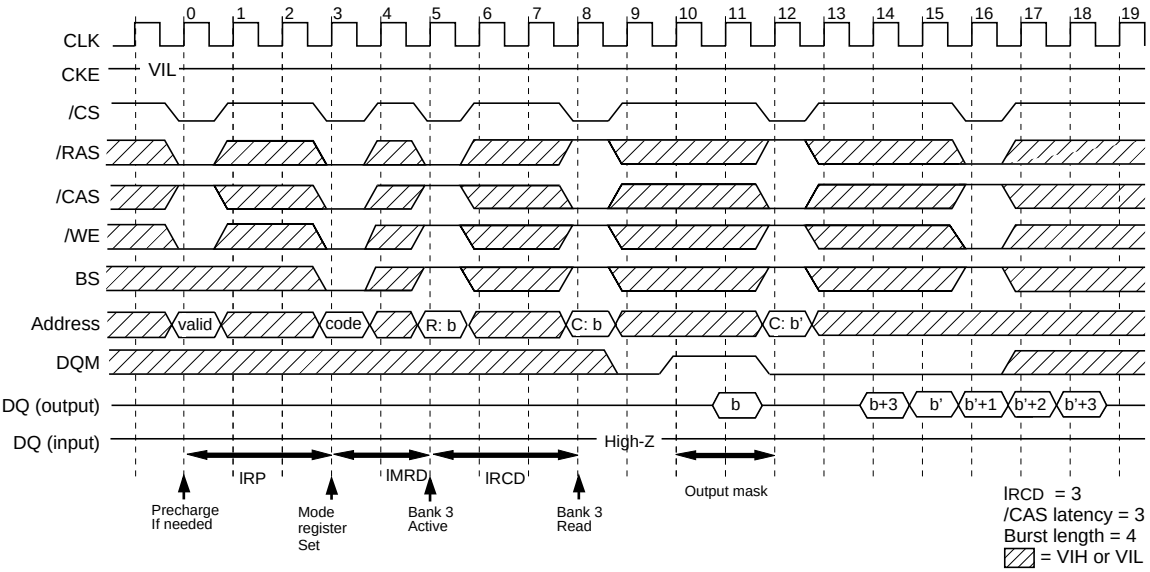
### Read Cycle



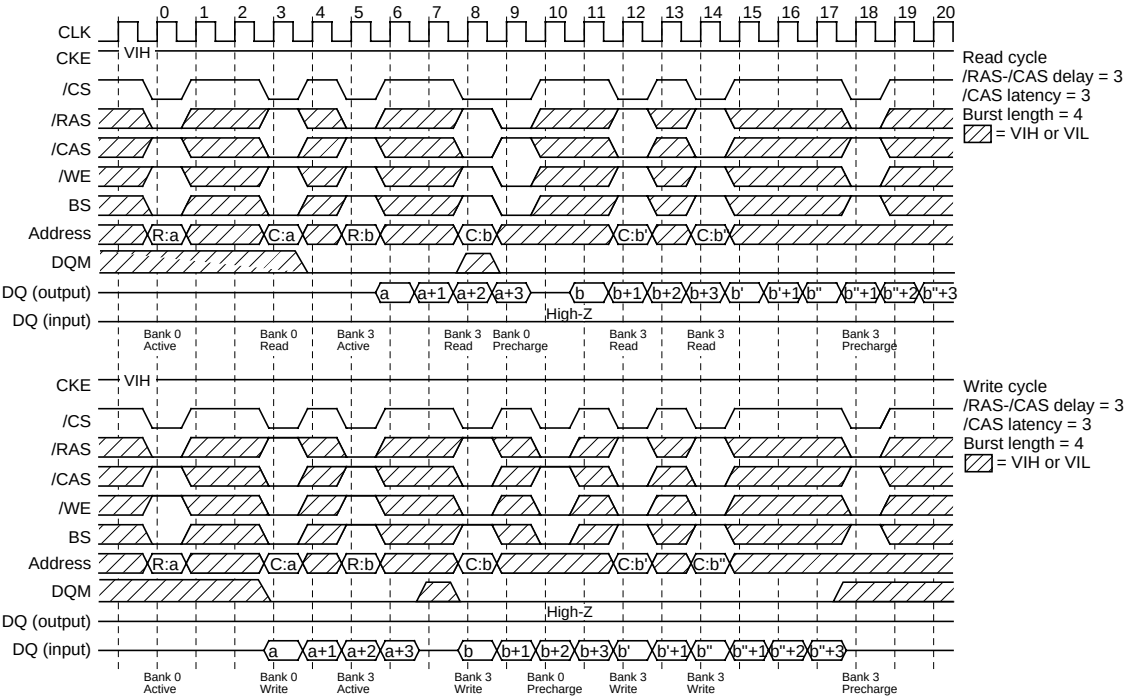
**Write Cycle**



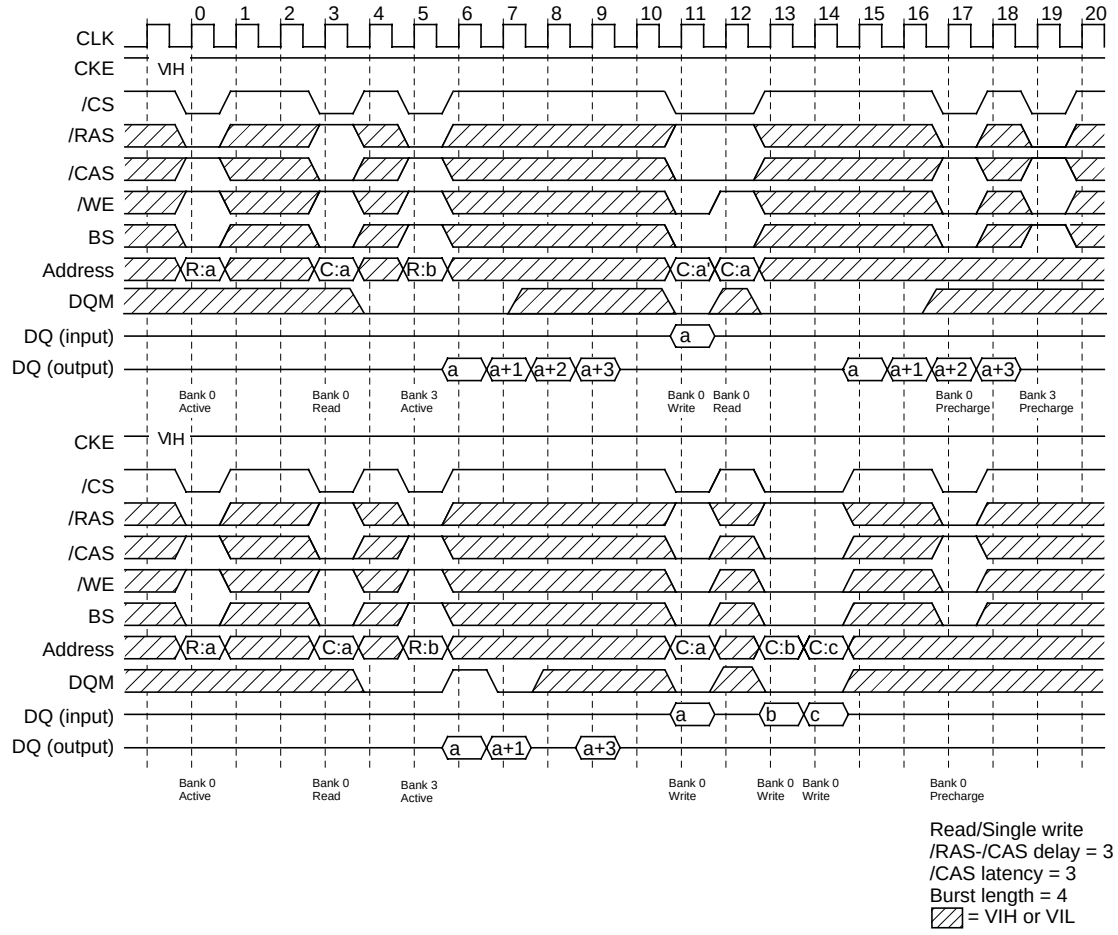

**Mode Register Set Cycle**



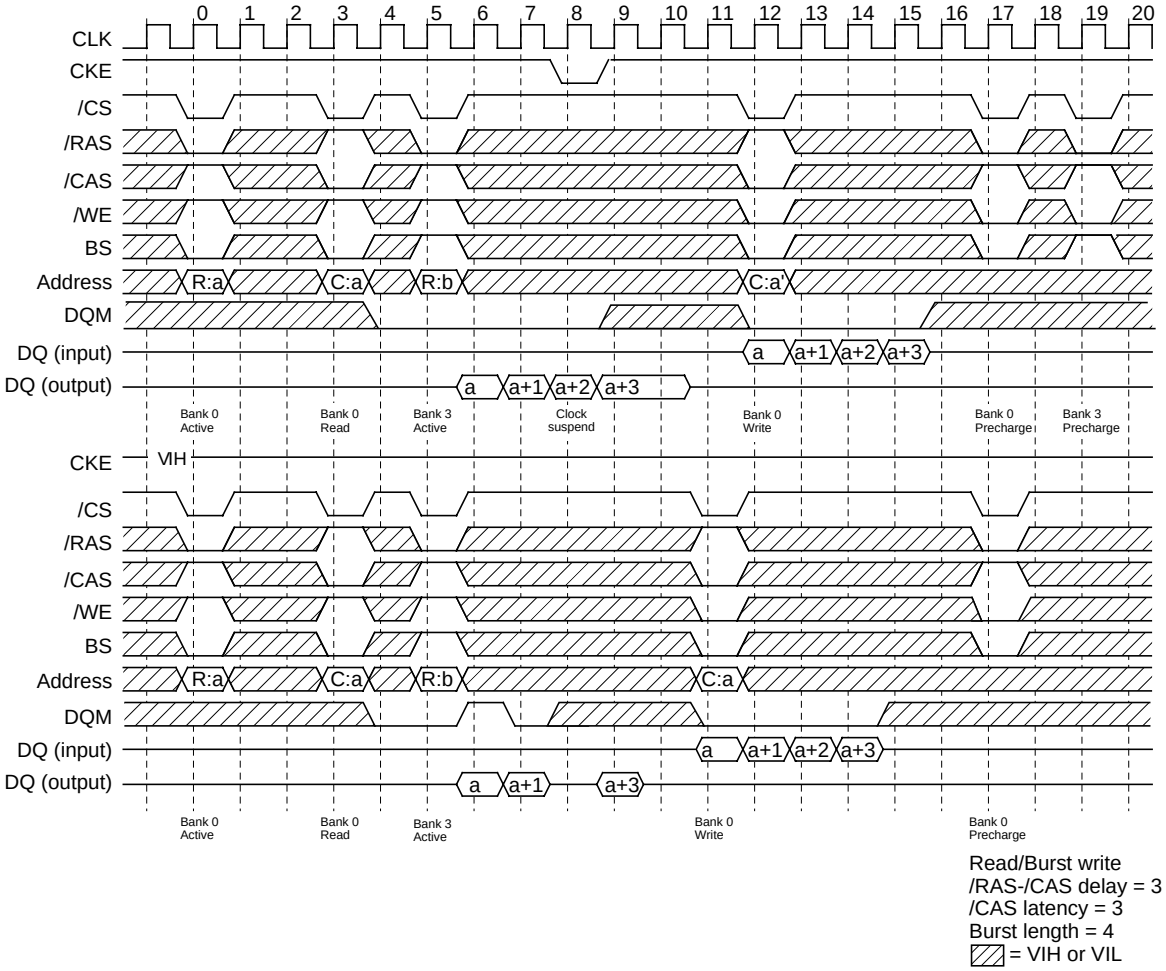
### Read Cycle/Write Cycle



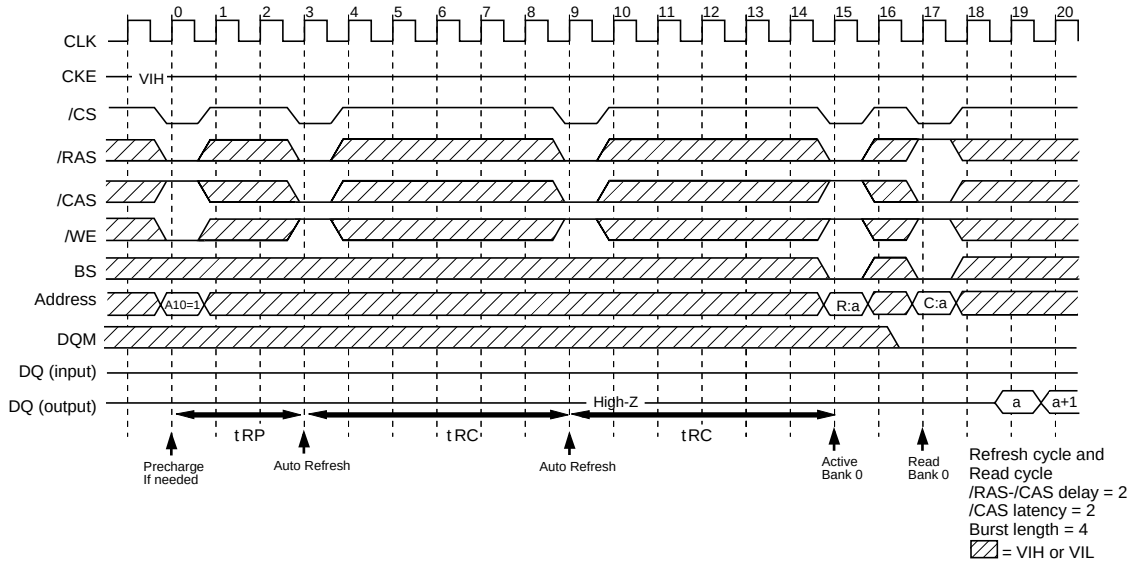

### Read/Single Write Cycle



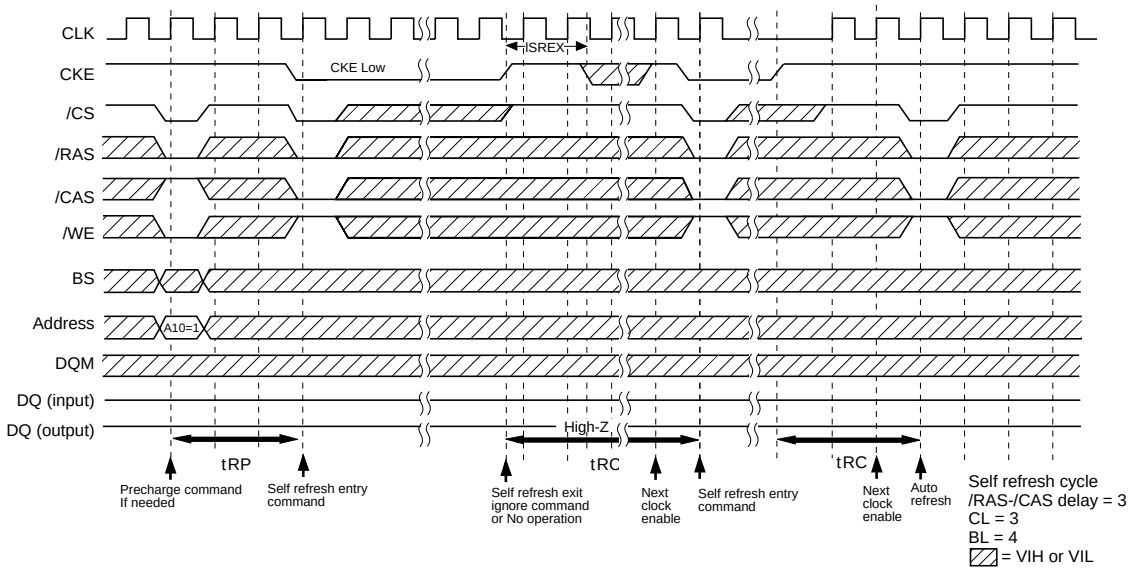
**Read/Burst Write Cycle**



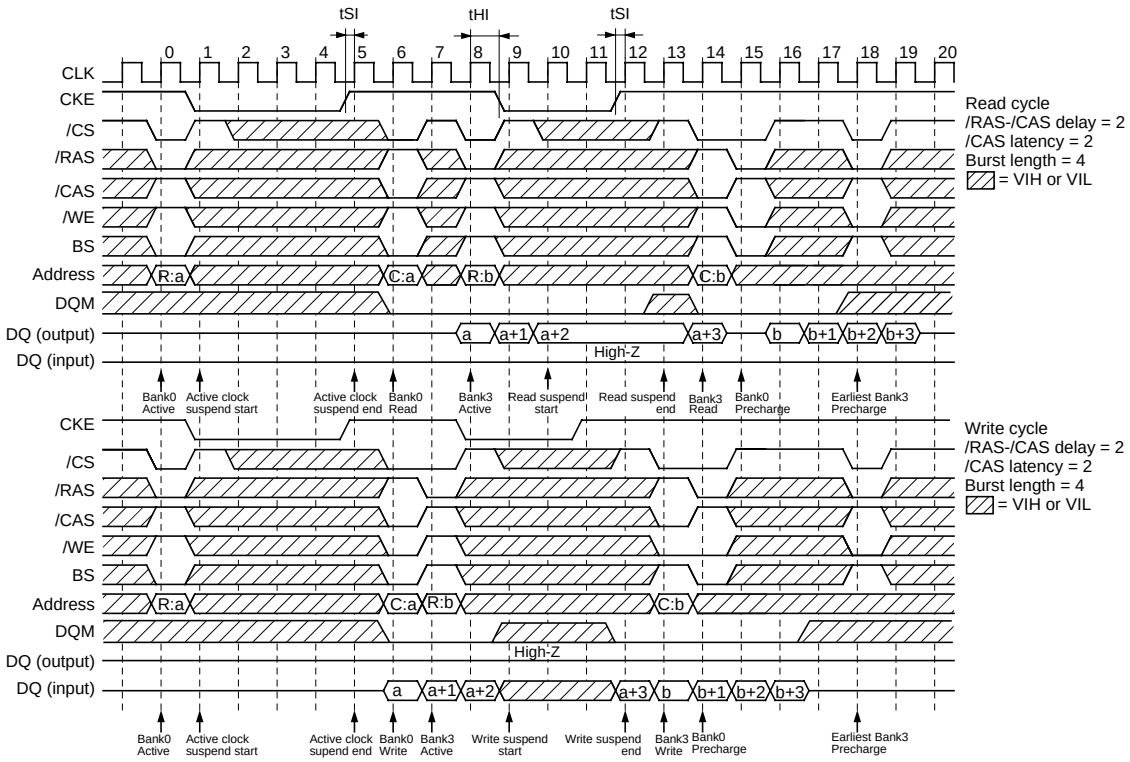

**Auto Refresh Cycle**



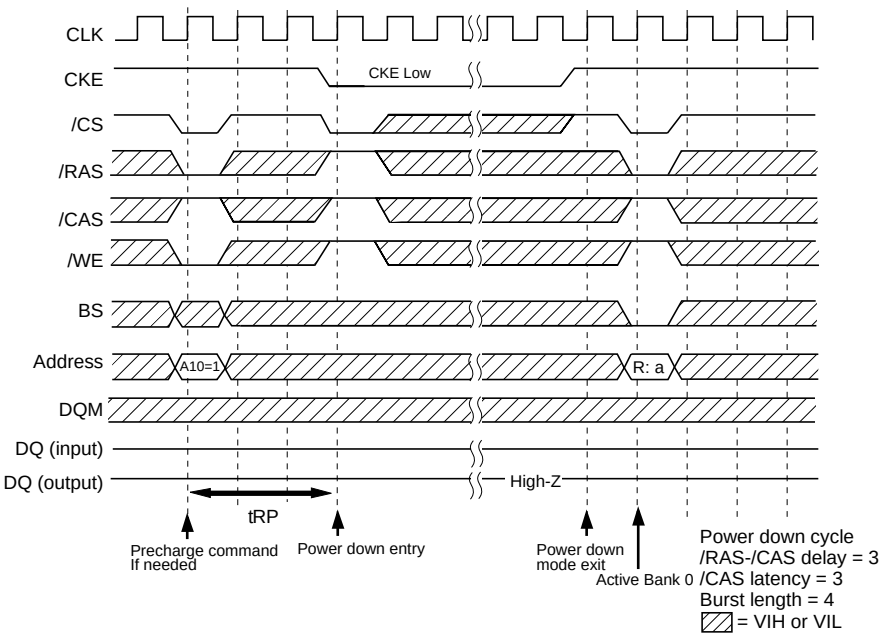
### Self Refresh Cycle



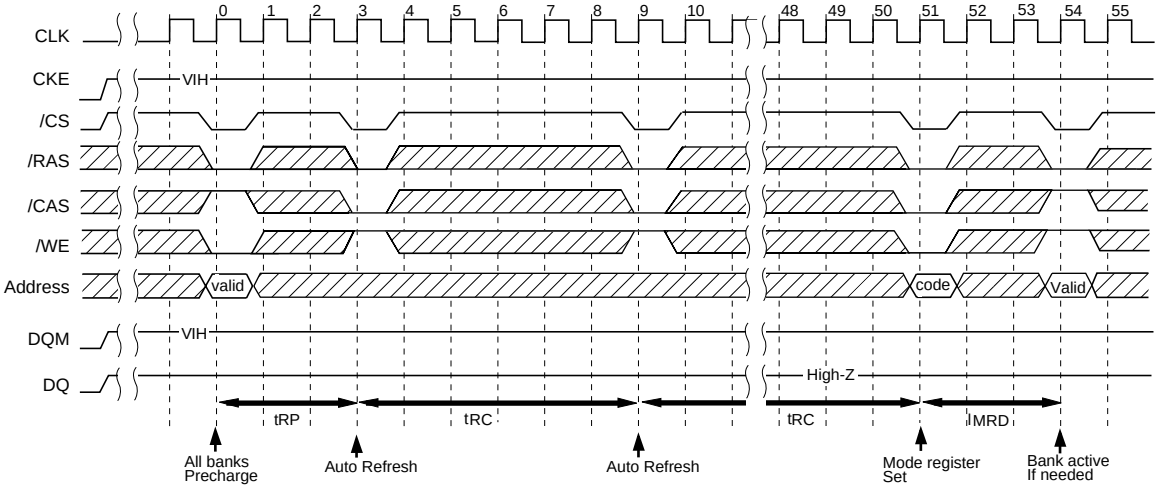

### Clock Suspend Mode



**Power Down Mode**



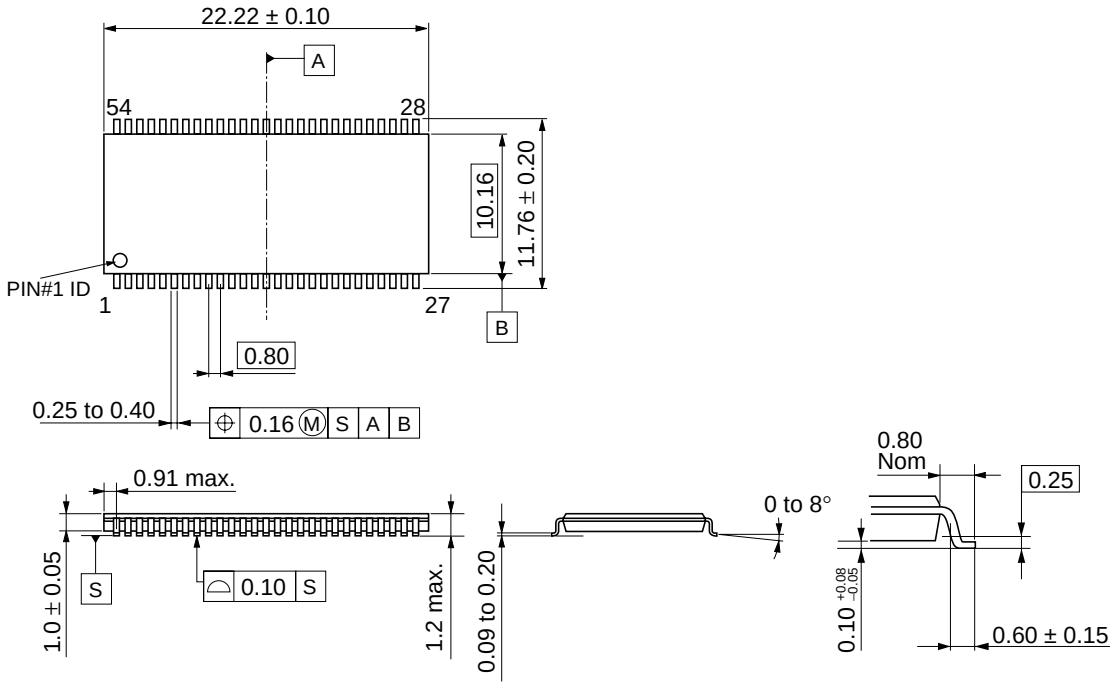

**Initialization Sequence**



## Package Drawing

### 54-pin Plastic TSOP (II)

Unit: mm




Note: Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.20mm per side.

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### Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDS25XXAPTA.

**Type of Surface Mount Device**

EDS25XXAPTA: 54-pin Plastic TSOP (II)

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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