TMS34092 BUSINESS GRAPHICS ARRAY FOR THE TMS34010

* Multiplexed Pixel Pipeline from VRAM to palette at 75 MHz
* Supports up to four oscillator sources
* Programmable for 1, 2, 4 or 8-Bit Pixel Size
* Direct connection to the TMS34010, VRAM, DRAM and palette
* Decodes the TMS34010 address space
  - Up to 1 Megabyte of VRAM
  - Up to 2 Megabytes of DRAM
  - Palette register access
* Three state outputs for VGA pass-through capability

DESCRIPTION

The TMS34092 Business Graphics Array (BGA)tm is a peripheral device for the TMS34010 Graphics System Processor. The Business Graphics Array generates the local memory address and control signals for the TMS34010 and manages the pixel pipeline for the graphics system. The Business Graphics Array memory bus supports 256Kx4 VRAM and 64Kx4 or 256Kx4 DRAM devices, generating the multiplexed addresses, and row and column address strobes for the RAMs. Several memory organizations are supported to provide flexible and efficient utilization of the available menory. A minimum of 512K of VRAM may be used or up to 1M of VRAM and 2M of DRAM. The memory bus may be forced to a high-impedance state to allow other devices to control the local memory.

The pixel pipeline within the TMS34092 provides multiplexing of the serial data from VRAMs to a Bt47x style palette at 1, 2, 4 and 8 bits per pixel and at data rates up to 75 MHz. The pipeline also generates the video dot clock (DOTCLOCK) to the palette, the appropriate serial clock (SC) for the VRAM and the video clock (VCLK) used by the TMS34010. The TMS34092 decodes the TMS34010 accesses to the palette and provides data buffering for palette data transactions.

The pixel pipeline outputs of the TMS34092 may be placed in a high impedance state to allow the system to implement VGA pass-through including sharing the palette.

The OSC0-OSC3 inputs allow for up to four separate video dot clock sources to allow multiple display resolutions. The TMS34092 provides for dividing the oscillator input frequency by two, giving the capability for each oscillator to provide multiple display resolutions. In addition, the OCS1 input may also be divided by four, which allows a single oscillator to be used for both the TMS34010 INCLK and one video dot clock.

SIGNAL DESCRIPTIONS

GSP Interface Group

Name	I/O	Description
LAD0-LAD15	I/O	Local Address/Data Bus.
RAS*	I	Local Row Address Strobe.
CAS*	I	Local Column Address Strobe.
LAL*	I	Local Address Latched.
DEN*	I	Local Data Enable.
DDOUT	I	Local Data Direction Out.
W*	I	Local Write Strobe.
TR*/QE*	I	Local Shift Register Transfer or Output Enable.
LRDY	O	Local Ready.

Local Memory Group

Name	I/O	Description
MA0-MA8	O	Multiplexed address.
RS0*-RS2*	O	Row Address Strobes.
CS0*-CS1*	O	Column address strobes.
SC	O	Serial Clock for VRAMs.
V0-V31	I	Serial Data inputs from VRAMs.

Palette Group

Name	I/O	Description
PD0-PD7	I/O	Data from/to Palette.
DSIZ	O	Controls the size of the Palette DAC. (8 or 6 bits).
PRD*	O	Palette read strobe.
PWR*	O	Palette write strobe.
PR0-1	O	Palette register select controls.
DOTCLOCK	O	Video dot clock to the palette.
P0-P7	O	Video data to the palette.
BLNK*	O	Video blanking.
CSYNC	O	Composite sync.

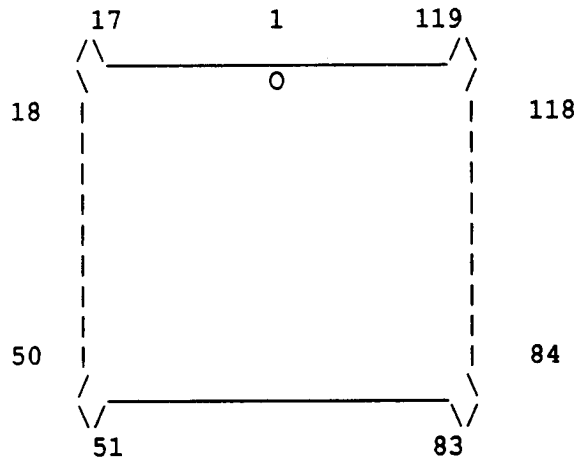
Video Group

Name	I/O	Description
PASS*	O	Display pass-through control.
S0-S3	I	Monitor Sense inputs.
ESYNC	I	External Sync Enable input.
EVID	I	External Video Enable input.
BLANK*	I	Blanking from the TMS34010.
HSYNC*	I	Horizontal sync from the TMS34010.
VSYNC*	I	Vertical sync from the TMS34010.
HS	I/O	Horizontal sync to the monitor.
VS	I/O	Vertical sync to the monitor.
VCLK	O	Video clock to the TMS34010.

System Group

Name	I/O	Description
RESET	I	Active high system reset input.
RST*	O	Active low reset output.
OSC0-OSC3	I	Oscillator inputs
HCS*	O	Host Chip Select to TMS34010.
FLT/256	O	Bus float/Color 256.
VCC	I	Nominal 5-volt power supply
VSS	I	Ground

TMS34092 Pin Assignments



132-pin Quad Flat Pack

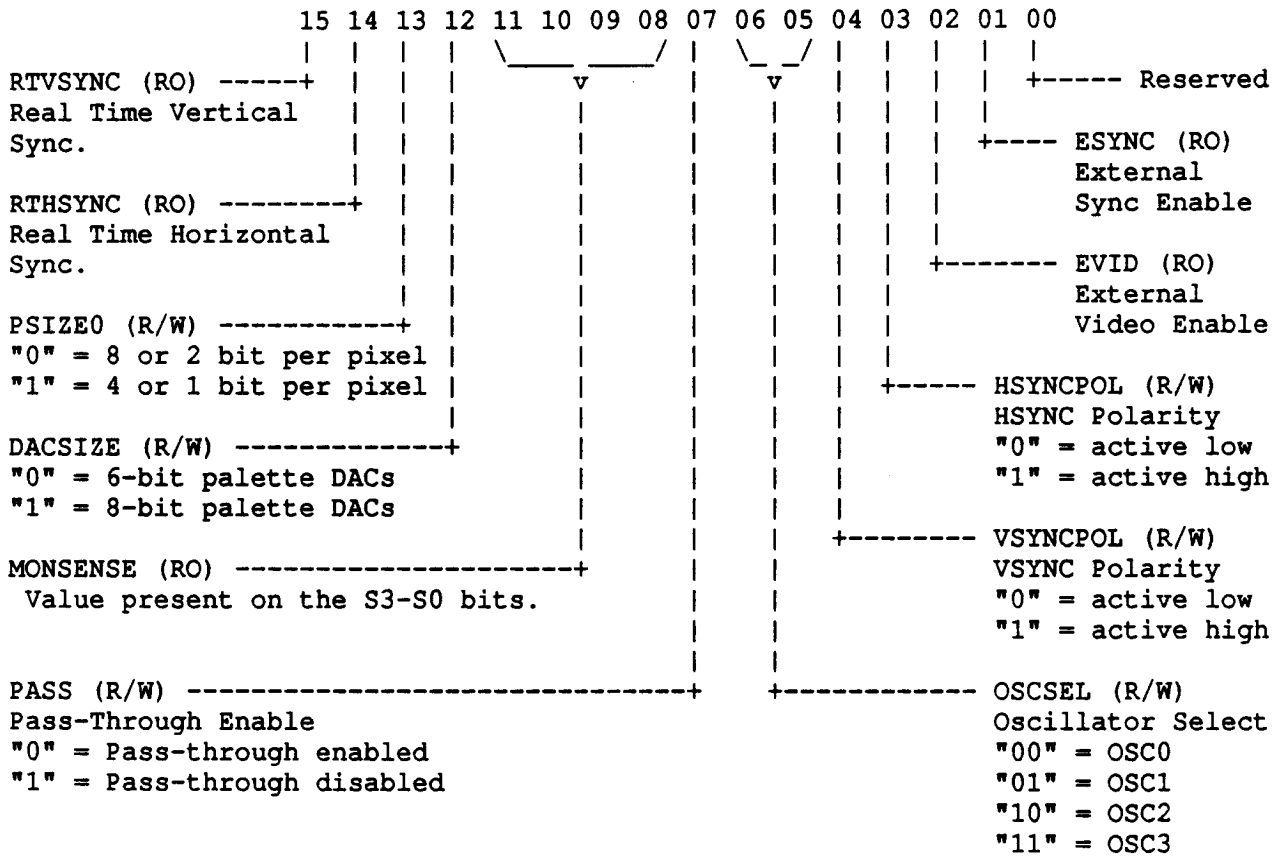
1	MA3	34	V23	67	LAD3	100	P1
2	MA2	35	V24	68	LAD2	101	VSS
3	MA1	36	V25	69	LAD1	102	P0
4	MA0	37	V26	70	LAD0	103	DOTCLK
5	VCC	38	V27	71	VCC	104	VCC
6	RS0*	39	V28	72	SC	105	CSYNC
7	RS1*	40	V29	73	VCLK	106	BLNK*
8	VSS	41	V30	74	VSS	107	VSS
9	LRDY	42	V31	75	OSC0	108	PR1
10	RS2*	43	TR*/QE*	76	OSC1	109	PR0
11	V0	44	W*	77	OSC2	110	PWR*
12	V1	45	CAS*	78	OSC3	111	PRD*
13	V2	46	RAS*	79	RST*	112	DSIZ
14	V3	47	DEN*	80	HCS*	113	S0
15	V4	48	DDOUT	81	PD7	114	S1
16	V5	49	LAL*	82	PD6	115	S2
17	V6	50	BLANK*	83	PD5	116	S3
18	V7	51	VSYNC*	84	PD4	117	EVID
19	V8	52	HSYNC*	85	PD3	118	RESET
20	V9	53	VCC	86	VCC	119	ESYNC
21	V10	54	LAD15	87	PD2	120	FLT/256
22	V11	55	LAD14	88	PD1	121	PASS*
23	V12	56	VSS	89	VSS	122	VS
24	V13	57	LAD13	90	PD0	123	HS
25	V14	58	LAD12	91	P7	124	CS0*
26	V15	59	LAD11	92	VCC	125	VCC
27	V16	60	LAD10	93	P6	126	CS1*
28	V17	61	LAD9	94	P5	127	MA8
29	V18	62	LAD8	95	VSS	128	VSS
30	V19	63	LAD7	96	P4	129	MA7
31	V20	64	LAD6	97	P3	130	MA6
32	V21	65	LAD5	98	VCC	131	MA5
33	V22	66	LAD4	99	P2	132	MA4

registers

There are 3 user accessable registers within the TMS34092 Business Graphics Array:

CR0	Control Register 0
CR1	Control Register 1
CR2	Control Register 2

CR0

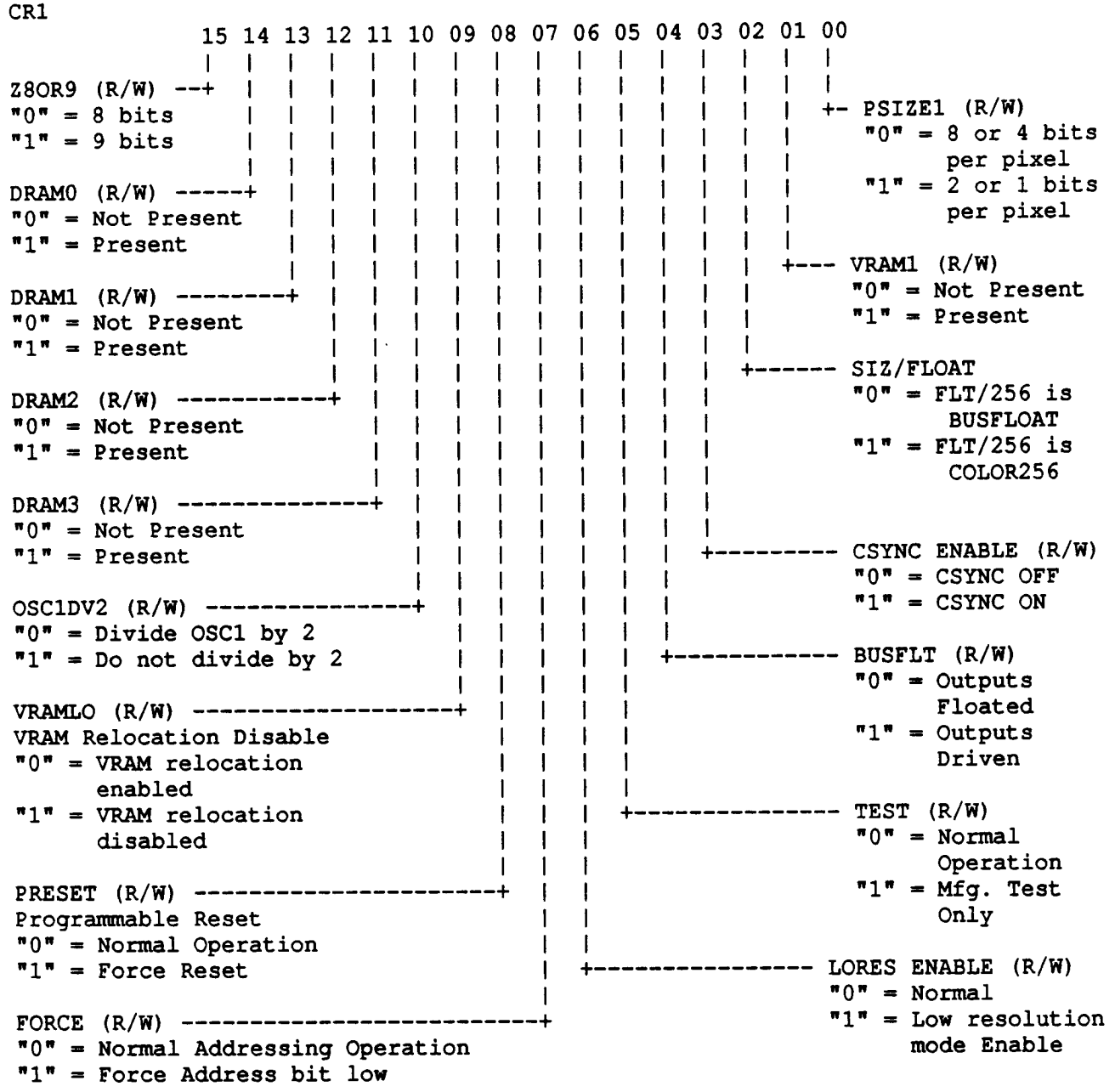


The CR0 register is accessed on memory cycles to address C000 2000 by the TMS34010.

Upon Reset, the CR0 register is set to "0000".

All reserved bits will always read "0" and should be written with "0" to allow compatibility with future revisions of the Business Graphics Array.

CR1



The CR1 register is accessed on memory cycles to address C000 2010 by the TMS34010.

Upon Reset, the CR1 register is set to "0000".

All reserved bits will always read "0" and should be written with "0" to allow compatibility with future revisions of the Business Graphics Array.

Reading External Real-Time Synchronization Signals. The RTVSYNC and RTHSYNC signals to the monitor may be read by the TMS34010 through these bits in CR0. In order to read these bits, a write to the CR0 register is first performed which will latch the data present on these signals. Then a read to the CR0 register will provide the data that was present at the time of the CR0 write.

Pixel Size Control. PSIZE0 (CR0 bit 13) and PSIZE1 (CR1 bit 00) concatenated together (PSIZE1:PSIZE0) control the pixel size (depth). The truth table for the pixel sizes is:

00 - 8 bits/pixel
01 - 4 bits/pixel
10 - 2 bits/pixel
11 - 1 bit/pixel

DAC Size. The TMS34092 provides the DSIZ output to control the current size of the DACs within the palette. When the DACSIZE bit is low the DSIZ pin is driven low to select the 6-bit (64 color) mode of the palette. When the DACSIZE bit is high the DSIZ pin is high to select the 8-bit (256 color) mode of the palette.

Monitor Sensing. The value present on the S3-S0 pins of the TMS34092 is available on the MONSENSE bits of CR0. These may be used by software to determine configuration information about the system. Typically, these will be used to determine the monitor type. The S3 signal is sensed at CR0 bit 11, S2 at bit 10, S1 at bit 9 and S0 at bit 8.

Pass-Through Enable. The TMS34092 supports passing video information and control from other devices to the palette by setting PASS to "0". This places the output of the pixel pipeline and control in a high-impedance state.

Oscillator Selection. The OSCSEL bits are use to select the oscillator input for the dotclock (DOTCLOCK) generation. These inputs also are used in conjunction with the PSIZE bits to set the Serial Clock (SC) and Video Clock (VCLK) timing.

Sync Polarity. The VSYNCPOL and HSYNCPOL bits control the logical sense of the vertical and horizontal synchronization signals (VS and HS) output by the TMS34092.

Reading External Synchronization and Video Enable. The EVID and ESYNC bits of CR0 allow the TMS34010 to determine if an external video subsystem has taken control of an external video bus, as in a VGA pass-through environment. In order to read these bits, a write to the CR0 register is first performed which will latch the data present on these signals. Then a read to the CR0 register will provide the data that was present at the time of the register write.

VRAM Installed. By definition, one physical bank of VRAM must always be installed (VRAM0), thus there is no bit to indicate its presence. An optional physical bank of VRAM is supported (VRAM1); however, its access is not enabled unless VRAM1 (CR1 bit 01) is set to "1." Additionally, when VRAM1 is present, the TMS34092 accesses VRAM0 and VRAM1 in an interleaved fashion (ie. Every other 16-bit word in the memory will be mapped to either VRAM0 or VRAM1).

FLT/256 Selection. The SIZ/FLOAT bit (CR1 bit 02) controls the function of the FLT/256 pin of the TMS34092. When SIZ/FLOAT is low, the FLT/256 pin is used to indicate the sense of the BUSFLT bit (CR1 bit 04). In this mode, the bit may be used to enable or disable other devices that share the memory and pixel pipeline buses with the TMS34092. When SIZ/FLOAT is high, the FLT/256 pin is used to indicate the current pixel size such that if the TMS34092 is operating in 8-bit per pixel (256 color) mode, the FLT/256 pin will be low and in all other modes (4, 2, and 1 bit per pixel), the FLT/256 pin will be high.

CSYNC Enable. If an RS-343 monitor is in use, a composite sync source must be provided to the monitor output. Setting the CSYNC bit to "1" enables the CSYNC output from the TMS34092.

Supporting Other Video Devices. Other video devices may be connected up to the memory, palette, and video buses by setting BUSFLT to "0", which causes the TMS34092 to allow all signals connected to those buses to go to a high-impedance state. If the SIZ/FLOAT bit (CR1 bit 02) is low then the FLT/256 output will also be driven low, which may be used as an enable to the other video device.

Testing the TMS34092 Buses. For testing purposes, all TMS34092 outputs may be forced to a high-impedance state when the TEST bit is set to "1." This bit has no useful function for the application programmer or end-user.
NOTE: Since LRDY, HCS* and RST* are forced to high-impedance by this bit, designers should include pull-up resistors on LRDY and RST* (10K ohms) and a pull-down on HCS* (1K ohms) so that if this bit is set, the TMS34010 can still be accessed through the host port.

Low Resolution Mode. The TMS34092 supports low resolution display modes for animation using the same oscillator inputs required for the higher resolution modes. Setting the LORES bit high causes the dotclock to be divided by two before entering the pixel pipeline logic which effectively reduces the horizontal resolution by half.

Force Address. When the LORES mode is enabled (CR1 bit 06), setting the FORCE bit high causes the TMS34092 to force the least significant bit of the display row address generated on shift register transfer cycles to a "0". This causes every row to be displayed twice, effectively reducing the vertical resolution by half.

Program Controlled Reset. A host or TMS34010 program may force a reset of the the TMS34092 by setting PRESET to "1", which also sets the RST* output low. The duration of this reset is fixed at approximately 260 clock periods of OSC1 (10.4 us at 50.35MHz with OSC1DV2 = 0).

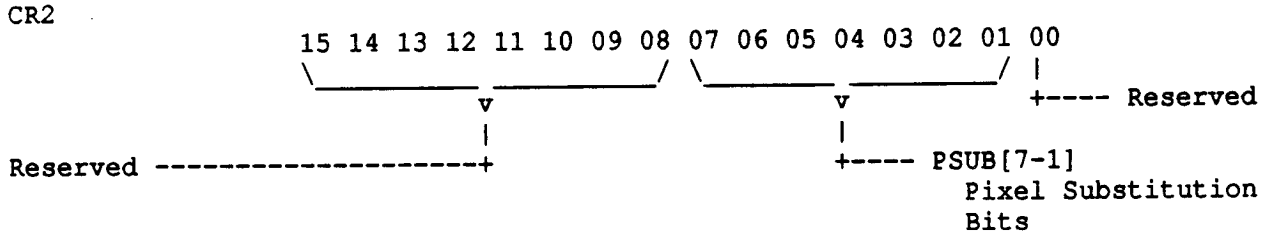
Disabling VRAM Relocation to High Memory Addresses. For the special case where only one bank of VRAM is installed and only DRAM0 is installed, the user may desire to utilize all of the VRAM for display memory (e.g. for 640x480x8 displays). Setting the VRAMLO bit high prevents the 128K of VRAM from being remapped to the top of the memory space.

Oscillator 1 Divided By Two. OSC1DV2 (bit 10) provides support for TMS34092 implementations which use a TMS34010 INCLK frequency which is twice a display dotclock frequency. In such an implementation, the INCLK frequency is connected to the TMS34092 OSC1 input and is internally divided by two prior to use in the pixel pipeline logic. Those implementations which cannot use an INCLK at twice dotclock frequency will provide a diferent oscillator from the TMS34010 INCLK oscillator and disable the divide by two by setting OSC1DV2 to "1".

DRAM Installed. DRAM Bank 0 which is controlled by the DRAM0 (bit 14), is the only DRAM bank which is allowed to have less than 512 KBytes available. DRAM Bank 0 may have either 128K, 256K, or 512K installed, depending upon the memory devices used. DRAM Banks 1-3 inclusive support only 512 KByte installations. The DRAM Banks should be filled in the order 0, 1, 2, 3; higher numbered banks are enabled only if all lower numbered banks are enabled (i.e. DRAM0 must be set to "1" to enable DRAM1; both DRAM0 and DRAM1 must be enabled to enable DRAM2; DRAM0, DRAM1 and DRAM2 must be enabled to enable DRAM3.)

DRAM0 Address Multiplexing. Since DRAM Bank 0 may be require either 8 or 9 bits of multiplexed address, the Z8OR9 bit (bit 15) selects the width of the address multiplexing for DRAM0 accesses. The power-up configuration is Z8OR9 set to "0" selecting 8 bits of multiplexed address for the DRAM0 memory. This bit has no effect on other DRAM or VRAM memory banks.

CR2



The CR2 register is accessed on memory cycles to address C000 2020 by the TMS34010.

Upon Reset, the CR2 register is set to "0000".

All reserved bits will always read "0" and should be written with "0" to allow compatibility with future revisions of the Business Graphics Array.

Pixel Substitution Bits. For the cases where the TMS34092 is operating at less than 8 bits/pixel, the pixel substitution bits provide programmable control over the unused bits output on P7-P0, starting from the most significant bit downward. For example in the case of 4 bit/pixel systems, the least significant 4 bits (P3-P0) are provided to the palette from the frame buffer, and the most significant 4 bits (P7-P4) from PSUB[7-4]. With suitable palette programming, the preceding example allows the application to have 16 different palettes instantaneously available.

RESET

Reset puts the TMS34092 into a known initial state. A reset is initiated by asserting the input signal at the RESET input to its active-high level OR by setting the PRESET bit in CR1 high. During a reset, the RST* output is driven to its active-low level and HCS* is driven high. Upon setting the PRESET bit in CR1, RST* is held low by the TMS34092 to satisfy the 40 LCLK cycle reset requirement of the TMS34010 (This is done by counting 512 cycles of OSC1). HCS* is held high until after the low-to-high transition of RST* to keep the TMS34010 in a halted state following the reset.

During a Reset the TMS34092 Signals are:

Outputs set to high impedance	Outputs set low	Outputs set high	Bidirectionals set to high impedance
RS0*-RS2*	FLT/256	LRDY	LAD0-LAD15
CS0*-CS1*	PASS*	HCS*	PD0-PD7
MA0-MA8	RST*		HS
SC			VS
DSIZ			
P0-P7			
PRD*			
PWR*			
PR0-PR1			
DOTCLK			
BLNK*			
CSYNC			

After a Reset the TMS34092 Signals are:

Outputs set to high impedance	Outputs set low	Outputs set high	Bidirectionals set to high impedance
RS0*-RS2*	FLT/256	LRDY	LAD0-LAD15
CS0*-CS1*	PASS*	RST*	PD0-PD7
MA0-MA8	HCS*		HS
SC			VS
DSIZ			
P0-P7			
PRD*			
PWR*			
PR0-PR1			
DOTCLK			
BLNK*			
CSYNC			

NOTE: The only difference between these two tables are the levels of HCS* and RST*.

All of the control register bits are set to "0" during a reset, so that following reset, the BUSFLT bit in CR1 must be set high to enable the outputs of the TMS34092. The default power-up configuration of the TMS34092 registers is for operation with the minimum of 512K of VRAM and no DRAM present.

TMS34092 Signals controlled by BUSFLT

When the BUSFLT bit in CR1 is set low, the following signals will be placed in a high-impedance state:

RS0*-RS2*	PRD*	CSYNC
CS0*-CS1*	PWR*	LAD0-LAD15
MA0-MA8	PR0-PR1	PD0-PD7
SC	DOTCLK	HS
DSIZ	BLNK*	VS
P0-P7		

The state of the FLT/256 signal depends upon the SIZ/FLOAT bit in CR1. If SIZ/FLOAT is set low, setting BUSFLT low will cause the TMS34092 to place the controlled signals in a high-impedance state. Logic within the TMS34092 will delay a minimum of 4 cycles of OSC1 and then set FLT/256 low. Setting BUSFLT high causes FLT/256 to go high, and after the minimum of 4 cycles of OSC1 the TMS34092 will assert its outputs. If SIZ/FLOAT is set high, the state of the FLT/256 output is determined by the PSIZE bits (FLT/256 is low when configured for 8 bit per pixel mode).

TMS34092 Signals not affected by BUSFLT

RST*	LRDY
HCS*	PASS*

TMS34092 Signals controlled by TEST

When the TEST bit in CR1 is set high, all of the TMS34092 outputs are placed in a high-impedance state:

RS0*-RS2*	PRD*	FLT/256	LAD0-LAD15
CS0*-CS1*	PWR*	PASS*	PD0-PD7
MA0-MA8	PR0-PR1	HCS*	HS
SC	DOTCLK	RST*	VS
DSIZ	BLNK*	LRDY	
P0-P7	CSYNC		

TMS34092 Signals controlled by PASS

When the PASS bit in CR1 is set low, the following signals will be placed in a high-impedance state:

DSIZ	PR0-PR1
P0-P7	DOTCLK
PRD*	BLNK*
PWR*	CSYNC

Setting the PASS bit low will cause the TMS34092 to place the controlled signals in a high-impedance state. Logic within the TMS34092 will delay at a minimum 4 cycles of OSC1 and then set the PASS* output signal low. Setting the PASS bit high causes the PASS* signal to go high, and after a minimum of 4 cycles of OSC1 the TMS34092 will assert its outputs.

TMS34092 Signals not affected by PASS

RS0*-RS2*	FLT/256	LAD0-LAD15
CS0*-CS1*	HCS*	PD0-PD7
MA0-MA8	RST*	HS
SC	LRDY	VS
DSIZ		

Oscillator Selection and Timing Control

The timing of DOTCLOCK, VCLK and SC are dependent upon the settings of the OSCSEL, OSC1DV2, LORES and PSIZE bits and the presence of VRAM1. The following tables show the relationship of these timings.

DOTCLK as a function of OSCSEL, OSC1DV2 and LORES bits and the oscillator inputs:

	DOTCLK			
	LORES = 0		LORES = 1	
OSCSEL	OSC1DV2 = 0	OSC1DV2 = 1	OSC1DV2 = 0	OSC1DV2 = 1
00	OSC0	OSC0	OSC0/2	OSC0/2
01	OSC1	OSC1/2	OSC1/2	OSC1/4
10	OSC2	OSC2	OSC2/2	OSC2/2
11	OSC3	OSC3	OSC3/2	OSC3/2

VCLK as a function of OSCSEL bits:

OSCSEL	Oscillator	VCLK
00	OSC0	DOTCLK/8
01	OSC1	DOTCLK/4
10	OSC2	DOTCLK/4
11	OSC3	DOTCLK/8

SC as a function of PSIZE and VRAM1 bits:

		SC	
PSIZE	Pixel Size	VRAM1 = 0	VRAM1 = 1
00	8	DOTCLK/2	DOTCLK/4
01	4	DOTCLK/4	DOTCLK/8
10	2	DOTCLK/8	DOTCLK/16
11	1	DOTCLK/16	DOTCLK/32

address multiplexing

The TMS34092 provides for the correct multiplexing of the logical addresses from the TMS34010 for the various memory organizations. The basic operational modes of the TMS34092 include:

a) 8 bit multiplexed addresses for DRAM0
b) 9 bit multiplexed addresses for DRAM and VRAM
c) Interleaved addressing for VRAM used as display memory
d) Stacked addressing for VRAM used as program memory
e) Serial Register Transfer cycles for one VRAM bank
f) Serial Register Transfer cycles for two VRAM banks

The TMS34092 uses the CAS-before-RAS refresh mode of the TMS34010 to provide refresh cycles to the memory; therefore it does not require special addressing for the refresh cycles.

The following figure illustrates the logical address bits output on each of the multiplexed address lines (MA0-MA8) during row and column intervals for each of the operational modes.

	DRAM0 only (Z8OR9=0) (64Kx4)		DRAM/VRAM (Z8OR9=1, VRAM1=0) (256Kx4)		VRAM (VRAM1=1, Interleave Display)		VRAM (VRAM1=1, Stacked Program)		Serial Register Transfer (VRAM1=0)		Serial Register Transfer (VRAM1=1)	
Bit	Row	Col	Row	Col	Row	Col	Row	Col	Row	Col	Row	Col
MA8	20	12	21	12	22	13	21	12	21	12	22	13
MA7	19	11	20	11	21	12	20#	11	20	"b"*	21	12
MA6	18	10	19	10	20	11	19	10	19	"a"*	20	"b"*
MA5	17	9	18	9	19	10	18	9	18	9	19	"a"*
MA4	16	8	17	8	18	9	17	8	17	8	18	9
MA3	15	7	16	7	17	8	16	7	16	7	17	8
MA2	14	6	15	6	16	7	15	6	15	6	16	7
MA1	13	5	14	5	15	6	14	5	14	5	15	6
MA0	12	4	13	4	14	5	13	4	13	4	14	5

When VRAM1 is present and either no DRAM or only DRAM0 is present, 128K from each VRAM bank is mapped to the upper address space (FFE0 0000 - FFFF FFFF). For VRAM0 this relocation requires that the logical address 20 presented on MA7 be forced high to the VRAM although the TMS34010 is accessing a memory location that outputs logical address 20 as low. This allows the upper 128K of VRAM0 to be mapped to FFE0 0000 - FFEF FFFF.

* The values for MA5, MA6 and MA7 during the column address of Serial Register Transfer cycles are dependent upon the state of FORCE, LORES, and the PSIZE bits. If both LORES and FORCE are high, then one of these multiplexed address bits will be forced to a "0" during the SRT cycle. The logical address is suppressed to force the same video data to be displayed on two horizontal scans. If the bit is not forced to a "0" it will display the logical address as on a normal access. The values for "a" and "b" are shown in the table below.

Address Forcing During Serial Register Transfer Cycles

		LORES = 0 OR FORCE = 0		LORES = 1 AND FORCE = 1	
PSIZE	Pixel Size	"a"	"b"	"a"	"b"
00	8	10	11	10	"0"
01	4	10	11	"0"	11
10	2	10	11	"0"	11
11	1	10	11	"0"	11

where for "a" and "b":
10 = logical address 10
11 = logical address 11
"0" = forced low

Memory Mapping and Sizing

In the minimum configuration of the TMS34092, 512K bytes of VRAM is present and a portion of the VRAM (128K bytes) is mapped to reside at the top of the address space. This is to provide for the program and interrupt vector requirements of the TMS34010. The remaining 384K bytes of the VRAM is available as display memory.

512K VRAM and 0K DRAM
(DRAM0=0, Z8OR9=0, DRAM1=0, DRAM2=0, DRAM3=0, VRAM1=0)

FFF0 0000 - FFFF FFFF	VRAM0 (128K)
D000 0000 - FFEF FFFF	Reserved
C000 3040 - CFFF FFFF	Reserved for external devices
C000 3000 - C000 303F	Palette
C000 2100 - C000 2FFF	Reserved for external devices
C000 2000 - C000 20FF	TMS34092 Internal Registers and Reserved
C000 0000 - C000 1FFF	TMS34010 Internal Registers and Reserved
1080 0000 - BFFF FFFF	Reserved
1030 0000 - 107F FFFF	Reserved for VRAM expansion
1000 0000 - 102F FFFF	VRAM0 (384K)
0000 0000 - 0FFF FFFF	Reserved

The addition of 128K of DRAM (using 64Kx4 devices) yields the following changes to the memory map:

512K VRAM and 128K DRAM
(DRAM0=1, Z8OR9=0, DRAM1=0, DRAM2=0, DRAM3=0, VRAM1=0)

FFF0 0000 - FFFF FFFF	VRAM0 (128K)
FFE0 0000 - FFEF FFFF	DRAM0 (128K)
D000 0000 - FFDF FFFF	Reserved

Note that the enabling of the DRAM (by setting DRAM0) does not affect the VRAM mapping. If DRAM0 is populated with 256K of DRAM (using 128Kx8 devices and indicated by Z8OR9 = 1) then the map changes to:

512K VRAM and 256K DRAM
(DRAM0=1, Z8OR9=1, DRAM1=0, DRAM2=0, DRAM3=0, VRAM1=0)

FFF0 0000 - FFFF FFFF	VRAM0 (128K)
FFD0 0000 - FFEF FFFF	DRAM0 (256K)
FFB0 0000 - FFCF FFFF	Shadow of FFD0 0000 - FFEF FFFF
D000 0000 - FFAF FFFF	Reserved

The shadow of the DRAM0 memory may be filled by using 256Kx4 devices for DRAM0 (for 512K of DRAM), in which case the map changes to:

512K VRAM and 512K DRAM
(DRAM0=1, Z8OR9=1, DRAM1=0, DRAM2=0, DRAM3=0, VRAM1=0)

FFF0 0000 - FFFF FFFF	VRAM0 (128K)
FFB0 0000 - FFEF FFFF	DRAM0 (512K)
D000 0000 - FFAF FFFF	Reserved

DRAM0 (if present) is always relocated to be the lowest addressable DRAM bank within TMS34092 address space. This is done to provide maximum contiguous program memory in minimum RAM configurations. When DRAM1 is present VRAM remapping to the top of the address space is disabled. Thus, for the case where DRAM0 is 128K and DRAM1 contains 512K of DRAM, the memory map becomes:

512K VRAM and 640K DRAM
(DRAM0=1, Z8OR9=0, DRAM1=1, DRAM2=0, DRAM3=0, VRAM1=0)

FFC0 0000 - FFFF FFFF	DRAM1 (512K)
FFB0 0000 - FFBF FFFF	DRAM0 (128K)
D000 0000 - FFAF FFFF	Reserved
C000 3040 - CFFF FFFF	Reserved for external devices
C000 3000 - C000 303F	Palette
C000 2100 - C000 2FFF	Reserved for external devices
C000 2000 - C000 20FF	TMS34092 Internal Registers and Reserved
C000 0000 - C000 1FFF	TMS34010 Internal Registers and Reserved
1080 0000 - BFFF FFFF	Reserved
1040 0000 - 107F FFFF	Reserved for VRAM expansion
1000 0000 - 103F FFFF	VRAM0 (512K)
0000 0000 - 0FFF FFFF	Reserved

Changing DRAM0 to 256K or 512K only slightly modifies the memory map:

512K VRAM and 768K DRAM
(DRAM0=1, Z8OR9=1, DRAM1=1, DRAM2=0, DRAM3=0, VRAM1=0)

FFC0 0000 - FFFF FFFF	DRAM1 (512K)
FFA0 0000 - FFBF FFFF	DRAM0 (256K)
FF80 0000 - FF9F FFFF	Shadow of FFA0 0000 - FFBF FFFF
D000 0000 - FF7F FFFF	Reserved

512K VRAM and 1024K DRAM
(DRAM0=1, Z8OR9=1, DRAM1=1, DRAM2=0, DRAM3=0, VRAM1=0)

FFC0 0000 - FFFF FFFF	DRAM1 (512K)
FF80 0000 - FFBF FFFF	DRAM0 (512K)
D000 0000 - FF7F FFFF	Reserved

The addition of DRAM memory banks causes relocation of the physical addressing of those banks. The process still takes effect such that any available DRAM is located at the top of memory space, and is contiguous. The relocation mechanism is analogous to physically stacking the additional DRAM banks, such that the last bank added "pushes" the previous banks "down" to lower address ranges. In the case where the maximum DRAM population supported by the TMS34092 is installed, the memory map appears as follows:

512K VRAM and 2048K DRAM
(DRAM0=1, Z8OR9=1, DRAM1=1, DRAM2=1, DRAM3=1, VRAM1=0)

FFC0 0000 - FFFF FFFF	DRAM3 (512K)
FF80 0000 - FFBF FFFF	DRAM2 (512K)
FF40 0000 - FF7F FFFF	DRAM1 (512K)
FFF0 0000 - FF3F FFFF	DRAM0 (512K)
D000 0000 - FFEF FFFF	Reserved
C000 3040 - CFFF FFFF	Reserved for external devices
C000 3000 - C000 303F	Palette
C000 2100 - C000 2FFF	Reserved for external devices
C000 2000 - C000 20FF	TMS34092 Internal Registers and Reserved
C000 0000 - C000 1FFF	TMS34010 Internal Registers and Reserved
1080 0000 - BFFF FFFF	Reserved
1040 0000 - 107F FFFF	Reserved for VRAM expansion
1000 0000 - 103F FFFF	VRAM0 (512K)
0000 0000 - 0FFF FFFF	Reserved

Note that as DRAM2 is added, it "pushes" DRAM1 and DRAM0 "down" in the addressing space just as DRAM3 has "pushed" DRAM2, DRAM1, and DRAM0 "down".

In addition to supporting DRAM expansion, the TMS34092 also supports a VRAM expansion option (VRAM1). There is no requirement that DRAM be installed prior to installing VRAM1; however, if no DRAM (or only DRAM0) is present and VRAM1 is installed, then 256KB of the VRAM is relocated to be contiguous at the top of memory as follows:

1024K VRAM and 0K DRAM
(DRAM0=0, Z8OR9=0, DRAM1=0, DRAM2=0, DRAM3=0, VRAM1=1)

FFF0 0000 - FFFF FFFF	VRAM1 (128K)
FFE0 0000 - FFEF FFFF	VRAM0 (128K)
D000 0000 - FFEF FFFF	Reserved
C000 3040 - CFFF FFFF	Reserved for external devices
C000 3000 - C000 303F	Palette
C000 2100 - C000 2FFF	Reserved for external devices
C000 2000 - C000 20FF	TMS34092 Internal Registers and Reserved
C000 0000 - C000 1FFF	TMS34010 Internal Registers and Reserved
1080 0000 - BFFF FFFF	Reserved
1060 0000 - 107F FFFF	not accessable
1000 0000 - 105F FFFF	VRAM0 & VRAM1 (768K Interleaved)
0000 0000 - 0FFF FFFF	Reserved

In this mode, the VRAM is split to provide contiguous address space at two locations within the memory map. Addressing through the memory in the display area (1000 0000 - 105F FFFF) will alternately access a 16-bit word from VRAM0 and then from VRAM1. The presence of VRAM1 also controls the pixel pipeline multiplexor to alternate between the serial data from VRAM0 and VRAM1 for successive groups of pixels.

The VRAM that is mapped to the top of the memory map is split such that VRAM1 occupies FFF0 0000 - FFFF FFFF and VRAM0 occupies FFE0 0000 - FFEF FFFF. The VRAMs are thus "stacked" within the address space.

If DRAM0 were present in this example, it would be mapped below VRAM0 to occupy FFD0 0000 - FFDF FFFF (128K of DRAM0), FFC0 0000 - FFDF FFFF (256K of DRAM0) or FFD0 0000 - FFDF FFFF (512K of DRAM0).

For the special case where DRAM0 and VRAM0 are the only installed memory, relocation of the VRAM to the top of the memory space is controlled by the VRAM relocation bit (CR1 bit 09). When this bit is "0" one quarter of the available VRAM is relocated to high memory. If this bit is set to "1" relocation is disabled.

512K VRAM and 128K DRAM (VRAMLO = 1)
(DRAM0=1, Z8OR9=0, DRAM1=0, DRAM2=0, DRAM3=0, VRAM1=0)

FFF0 0000 - FFFF FFFF	DRAM0 (128K)
D000 0000 - FFEF FFFF	Reserved
C000 3040 - CFFF FFFF	Reserved for external devices
C000 3000 - C000 303F	Palette
C000 2100 - C000 2FFF	Reserved for external devices
C000 2000 - C000 20FF	TMS34092 Internal Registers and Reserved
C000 0000 - C000 1FFF	TMS34010 Internal Registers and Reserved
1080 0000 - BFFF FFFF	Reserved
1040 0000 - 107F FFFF	Reserved for VRAM expansion
1000 0000 - 103F FFFF	VRAM0 (512K)
0000 0000 - 0FFF FFFF	Reserved

In an implementation taking full advantage of the TMS34092, the expanded memory map is:

1024K VRAM and 2048K DRAM
(DRAM0=1, Z8OR9=1, DRAM1=1, DRAM2=1, DRAM3=1, VRAM1=1)

FFC0 0000 - FFFF FFFF	DRAM3 (512K)
FF80 0000 - FFBF FFFF	DRAM2 (512K)
FF40 0000 - FF7F FFFF	DRAM1 (512K)
FFF0 0000 - FF3F FFFF	DRAM0 (512K)
D000 0000 - FFEF FFFF	Reserved
C000 3040 - CFFF FFFF	Reserved for external devices
C000 3000 - C000 303F	Palette
C000 2100 - C000 2FFF	Reserved for external devices
C000 2000 - C000 20FF	TMS34092 Internal Registers and Reserved
C000 0000 - C000 1FFF	TMS34010 Internal Registers and Reserved
1080 0000 - BFFF FFFF	Reserved
1040 0000 - 107F FFFF	Reserved for VRAM expansion
1000 0000 - 103F FFFF	VRAM0 & VRAM1 (1M Interleaved)
0000 0000 - 0FFF FFFF	Reserved

Designing for Expansion

Using the TMS34092 allows an expandable system to be built that starts with a minimum of VRAM memory and may be upgraded by adding the memory devices and reconfiguring the control registers. The physical connections to existing memory do not need to be modified to add additional DRAM or VRAM to the system since the TMS34092 manipulates the control signals appropriately.

absolute maximum ratings over operating free-air temperature range+

Supply voltage range, VCC	-0.5V to 7V
Input voltage range, VI	-0.5V to VCC
Output voltage range, VO	-0.5V to VCC
Operating free-air temperature range	0 C to 55 C
Storage temperature range	-10 C to 150 C

+ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification in not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Voltage values are with respect to the VSS pins of the chip.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.75	5.0	5.25	V
VSS	Supply voltage#	0	0	0	V
IOH	High-level output current			8.0	mA
IOL	Low-level output current			8.0	mA
TA	Operating free-air temperature	0		55	C

Care should be taken to provide a minimum inductance path between the VSS pins and system ground in order to minimize noise on VSS.

DC electrical characteristics

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
VIH		2.0		VCC+0.3	V
VIL		-0.3		0.8	V
VOH	VCC = min, IOH = max	2.6			V
VOL	VCC = max, IOL = max			0.5	V
IO (hiZ leakage)	VCC = max, VO = VCC			20	uA
IO (hiZ leakage)	VCC = max, VO = 0			-20	uA
II	VI = VSS to VCC			20	uA
ICC	VCC = max			250	mA
CI			10		pF
CO			15		pF

For conditions shown as "min" or "max", use the appropriate value specified under "Recommended Operating Conditions."

All typical values are at VCC=5V, TA=25 C.

signal transition levels

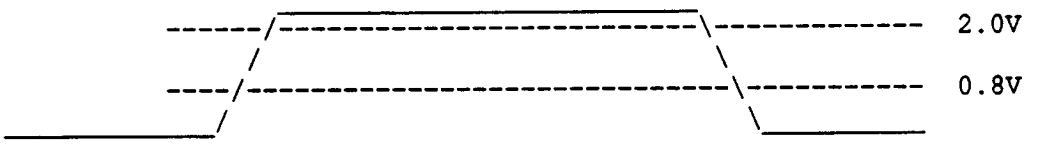


FIGURE xx. TTL-Level Inputs

For a high-to-low transition on a TTL-compatable input signal, the level at which the input is said to be "no longer high" is 2.0 volts, and the level at which the input is said to be "low" is 0.8 volts. For a low-to-high transition, the level at which the input is said to be "no longer low" is 0.8 volts, and the level at which the input is said to be "high" is 2.0 volts.

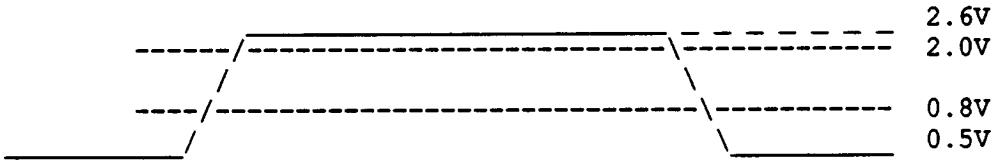


FIGURE xx. TTL-Level Outputs

TTL-level outputs are driven to a minimum logic-high level of 2.6 volts and to a maximum logic-low level of 0.5 volts. For a high-to-low transition on a TTL-compatable output signal, the level at which the output is said to be "no longer high" is 2.0 volts, and the level at which the output is said to be "low" is 0.8 volts. For a low-to-high transition, the level at which the output is said to be "no longer low" is 0.8 volts, and the level at which the output is said to be "high" is 2.0 volts.

test measurement

timing parameter symbology

In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meaning are:

a	access time
c	cycle time (period)
d	delay time
h	hold time
su	setup time
t	transition time
tf	transition, falling edge
tr	transition, rising edge
w	pulse duration (width)

The following letters and symbols and their meaning are:

H	High
L	Low
NV	Not Valid
V	Valid
Z	High Impedance
↑	No longer low
↓	No longer high

TIMING PARAMETERS ARE NOT AVAILABLE AT THIS TIME.

THIS DESIGN HAS BEEN VERIFIED BY SIMULATION
USING MODELS FOR:

TMS34010-50 (@ 50MHz)
TMS34010-60 (@ 60MHz)
TMS44C256-12
TMS41C251-12
BT477-80
and the
TMS34092-64

OPERATING AS AN ADD_IN BOARD FOR

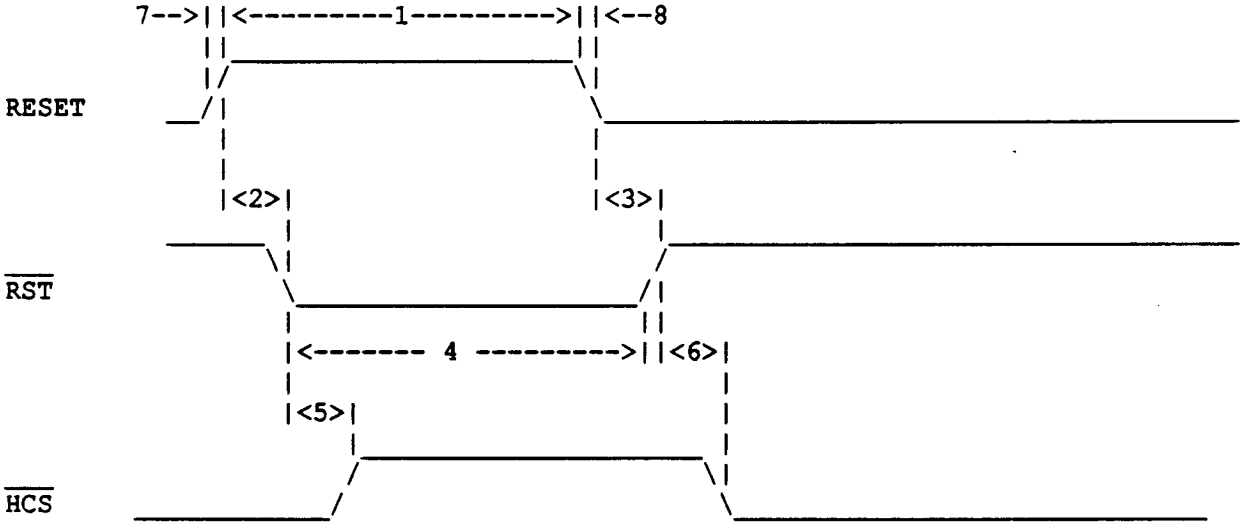
AN ISA COMPATIPLE COMPUTER.

For further information please contact:

Texas Instruments
Graphics Marketing
Attn: Phil Farr
(713) 274 - 3419

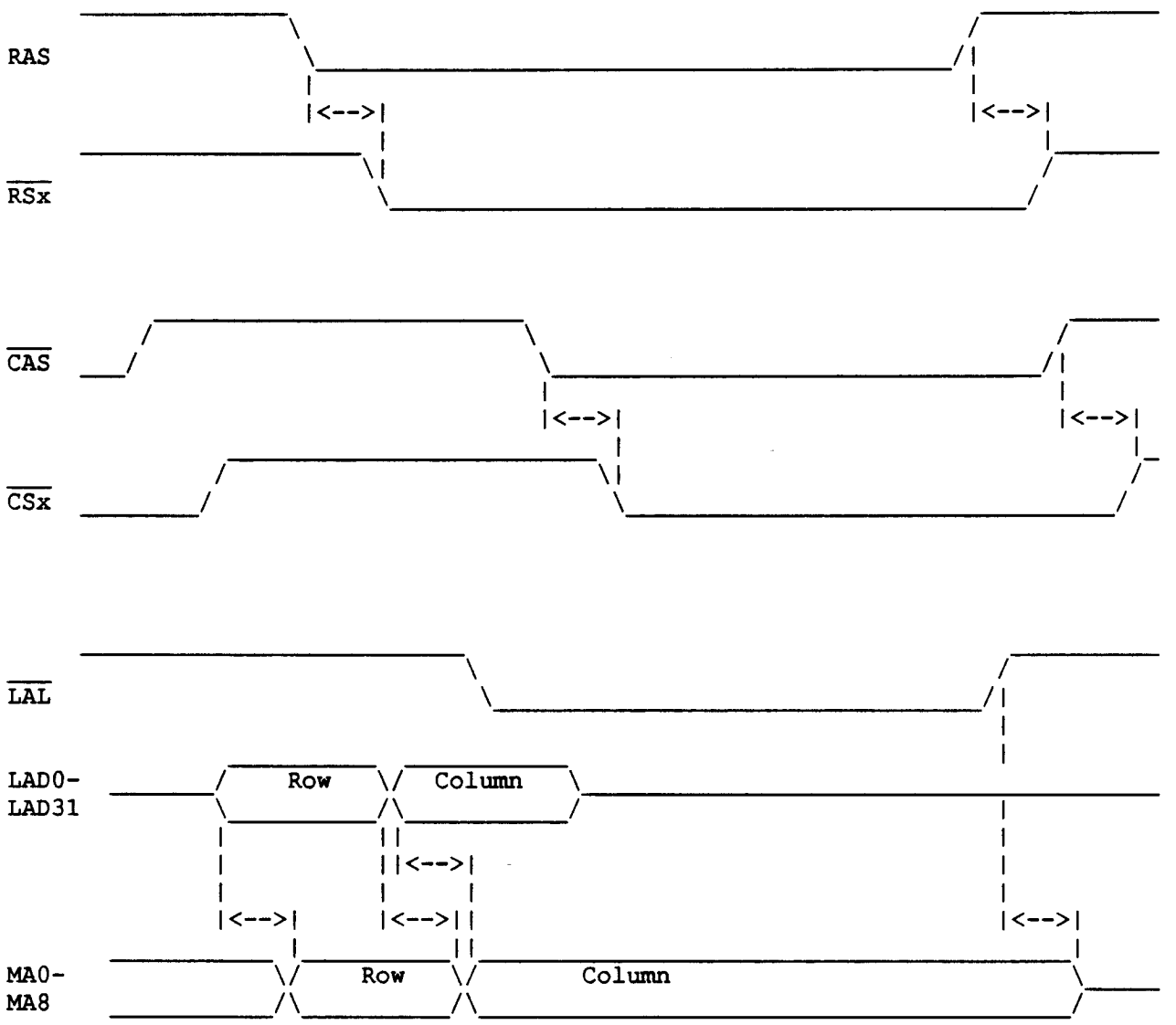
INCLK and RESET timing requirements

No.	Parameter	TMS34092-64 min	TMS34092-64 max
1	tw(RSH)	Duration of RESET high to reset TMS34092	
2	td(RSH-RL)	Delay from RESET high to RST* low	
3	td(RSL-RH)	Delay from RESET low to RST* high	
4	tw(RL)	Duration of RST* (low on programmed reset)	
5	td(RL-CSH)	Delay from RST* low to HCS* high	
6	td(RH-CSL)	Delay from RST* high to HCS* low	
7	ttr(RS)	Transition, RESET rising edge	
8	ttf(RS)	Transition, RESET falling edge	



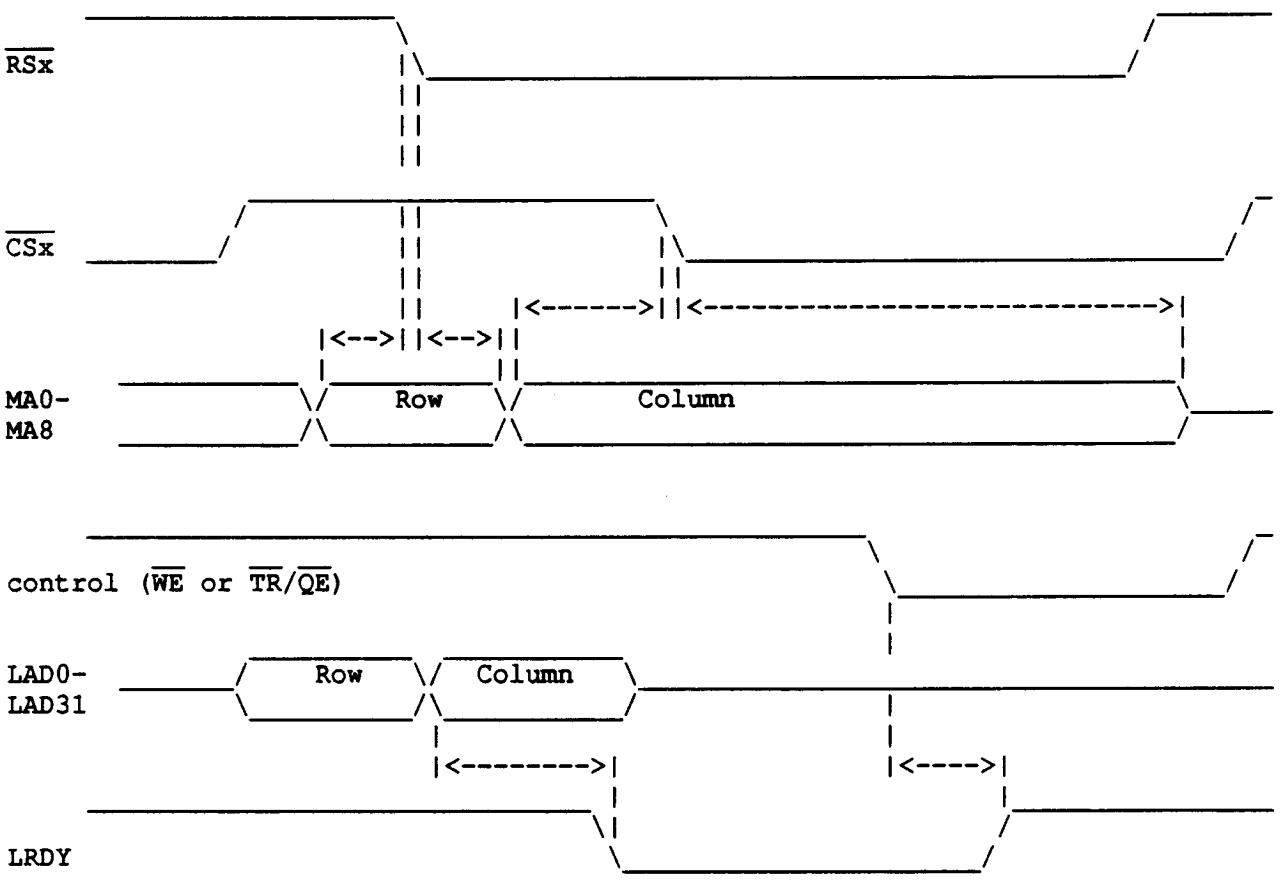
DRAM and VRAM Timing: RS, CS, and MA0-MA8

No.	Parameter	TMS34092-64 min	TMS34092-64 max
td(RSL-RL)	Delay RAS low to RSx low		
td(RSH-RH)	Delay RAS high to RSx high		
td(CSL-CL)	Delay CAS low to CSx low		
td(CSH-CH)	Delay CAS high to CSx high		
td(RAV-MV)	Delay Row address valid to MA0-MA8 valid		
th(MV-RANV)	Hold, MA0-MA8 valid after row address not valid		
td(CAV-MV)	Delay Column address valid to MA0-MA8 valid		
th(MV-LAH)	Hold, MA0-MA8 valid after LAL high		



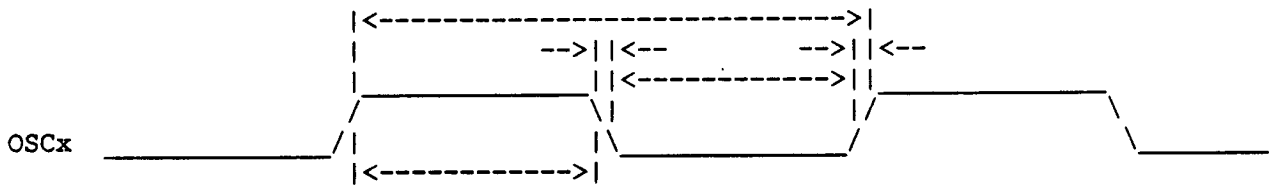
DRAM and VRAM Timing:

No.	Parameter	TMS34092-64 min	TMS34092-64 max
tsu(MAV-RS↓)	Setup of Row Address before RSx starts low		
th(MAV-RSL)	Hold of Row Address valid after RSx low		
tsu(MAV-CS↓)	Setup of column address before CSx starts low		
th(MAV-CSL)	Hold of column address valid after CSx low		
td(MAV-RYL)	Delay from LAL low to LRDY low		
td(CNL-RYL)	Delay from control low to LRDY (TR/QE is control for read cycle) (WE is control for write cycle)		



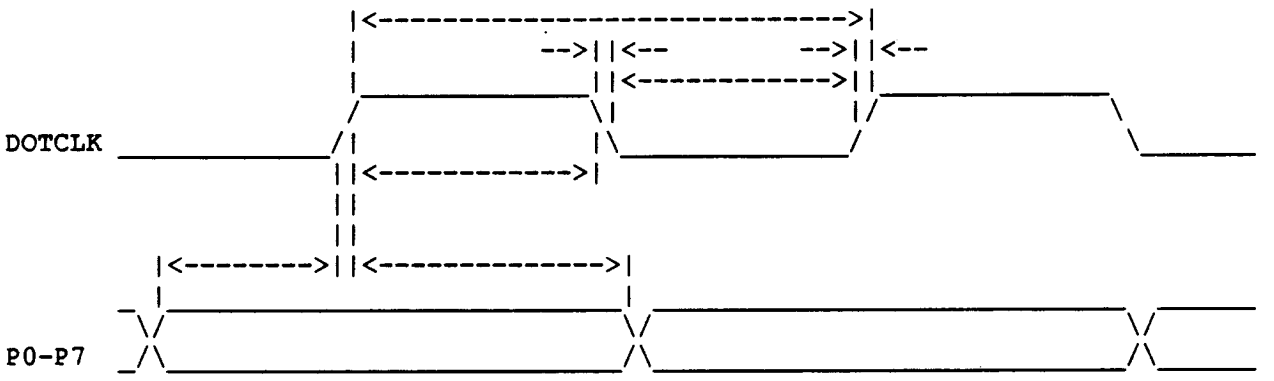
OScillator Timing:

No.	Parameter	TMS34092-64 min	TMS34092-64 max
tc(OSx)	Cycle time, OSCx inputs		
tw(OSxL)	Pulse width, OSCx low		
tw(OSxH)	Pulse width, OSCx high		
ttr(OSx)	Transition, OSCx rising edge		
ttf(OSx)	Transition, OSCx falling edge		



PIXEL DATA Timing: PD0-PD7 and DOTCLK

No.	Parameter	TMS34092-64 min	TMS34092-64 max
tc(DC)	Cycle time, DOTCLK		
tw(DCL)	Pulse width, DOTCLK low		
tw(DCH)	Pulse width, DOTCLK high		
ttr(DC)	Transition, DOTCLK rising edge		
ttf(DC)	Transition, DOTCLK falling edge		
tsu(PV-DC↑)	Setup of Pixel data before DOTCLK starts high		
th(PV-DCH)	Hold of Pixel data valid after DOTCLK high		



PALETTE Timing: PR0-PR1, PRD*, PWR* and PD0-PD7

No.	Parameter	TMS34092-64 min	TMS34092-64 max
	tsu(PRV-PC↓) Setup of Palette register select before PRD* or PWR* starts low		
	th(PRV-PCL) Hold of Palette register select after PRD* or PWR* low		
	tw(PCL) Pulse width, PRD* or PWR* low		
	tw(PCH) Pulse width, PRD* or PWR* high		
	tsu(PDV-PW↓) Setup of data before PWR* starts low		
	th(PDV-PWL) Hold of data after PWR* low		
	th(PDZ-PRL) Hold of data high impedance after PRD* low		
	td(PRL-PDV) Delay from PRD* low to data valid		
	th(PDV-PRH) Hold of data valid after PRD* high		
	td(PRH-PDZ) Delay from PRD* high to data high impedance