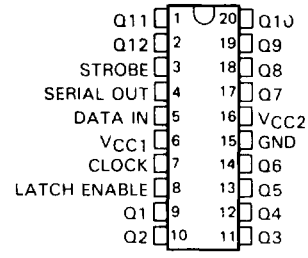
D2654, DECEMBER 1985 - REVISED OCTOBER 1989

- **Each Device Drives 12 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **TTL-Compatible Inputs**
- **Latches on All Driver Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

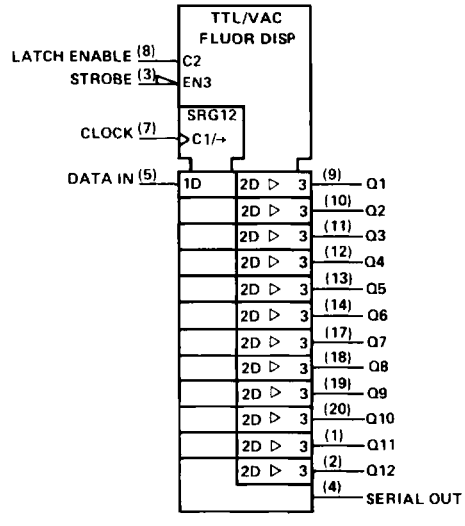
The SN65512B and SN75512B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 V. Outputs are totem-pole structures formed by an n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from −40°C to 85°C. The SN75512B is characterized for operation from 0°C to 70°C.

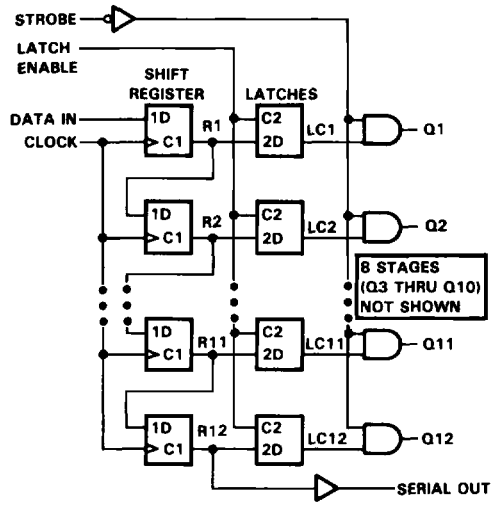
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

† BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

logic diagram (positive logic)



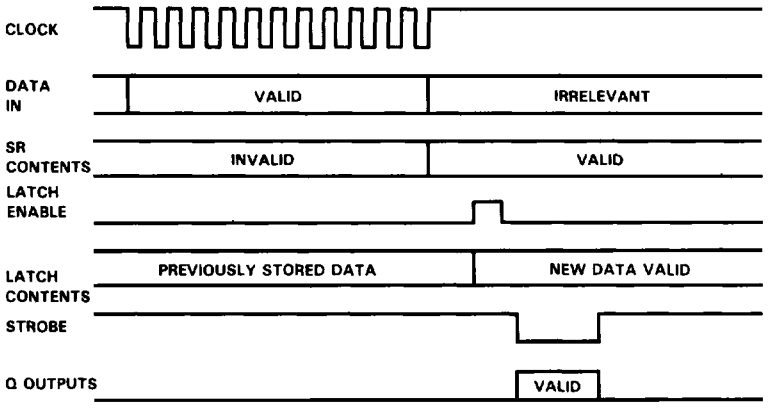
FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
LOAD	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡	R12	Determined by STROBE
	Not↑	X	X	No change	Determined by LATCH ENABLE‡	R12	Determined by STROBE
LATCH	X	L	X	As determined above	Stored data	R12	Determined by STROBE
	X	H	X		New data	R12	Determined by STROBE
STROBE	X	X	H	As determined above	Determined by LATCH ENABLE‡	R12	All L
	X	X	L		Determined by LATCH ENABLE‡	R12	LC1 thru LC12, respectively

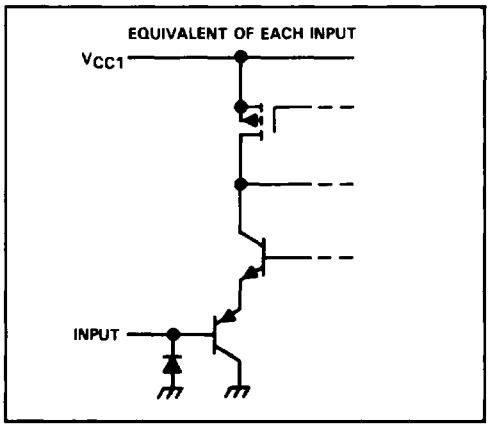
H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
† R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

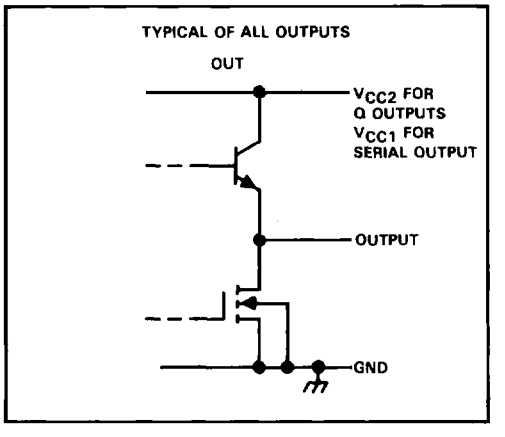
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

typical operating sequence



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 15 V
Supply voltage, V_{CC2} . . . . . 70 V
Input voltage . . . . . V_{CC1}
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: SN65512B . . . . . −40°C to 85°C
SN75512B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		SN65512B		SN75512B		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC1}		5	15	5	15	V
Supply voltage, V_{CC2}		0	60	0	60	V
High-level input voltage, V_{IH}		2		2		V
Low-level input voltage, V_{IL}			0.8		0.8	V
High-level output current, I_{OH}			−25		−25	mA
Low-level output current, I_{OL}	V_{CC1} = 10 V		5		5	mA
Clock frequency, f_{clock}	V_{CC1} = 15 V, T_A = 25°C	0	4	0	4	MHz
	V_{CC1} = 5 V, T_A = 25°C	0	1	0	1	
Pulse duration, CLOCK high or low, t_w	V_{CC1} = 15 V, T_A = 25°C	100		100		ns
	V_{CC1} = 5 V, T_A = 25°C	500		500		
Setup time, DATA IN before CLOCK↑, t_{su} (see Figure 1)	V_{CC1} = 15 V, T_A = 25°C	100		100		ns
	V_{CC1} = 5 V, T_A = 25°C	250		250		
Hold time, DATA IN after CLOCK↑, t_h (see Figure 1)	V_{CC1} = 15 V, T_A = 25°C	50		50		ns
	V_{CC1} = 5 V, T_A = 25°C	250		250		
Operating free-air temperature, T_A		−40	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		V
		Serial output	I_{OH} = −200 μA, V_{CC1} = 10 V		9	9.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 5 mA, V_{CC1} = 10 V			2.6	5	V
		Serial output	I_{OL} = 200 μA, V_{CC1} = 10 V			0.05	0.2	
I_{IH}	High-level input current		V_{CC1} = 15 V, V_I = 5 V			0.01	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V, V_I = 0.8 V			−25	−150	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 5 V		80	500	μA
				V_I = 0.8 V		2	6	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V	All outputs high		10	100	μA
				STROBE at 2 V		0.8	3	mA

†All typical values are at V_{CC1} = 10 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high-level output			300	ns
t_{THL}	Transition time, high-to-low-level output			500	ns
t_{TLH}	Transition time, low-to-high-level output			500	ns

PARAMETER MEASUREMENT INFORMATION

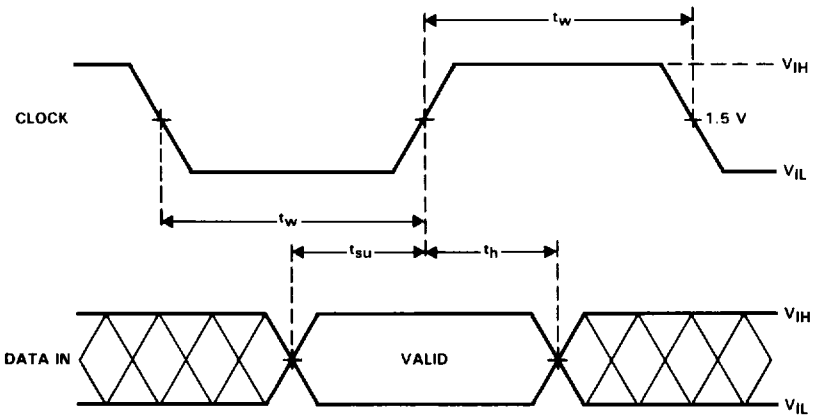


FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

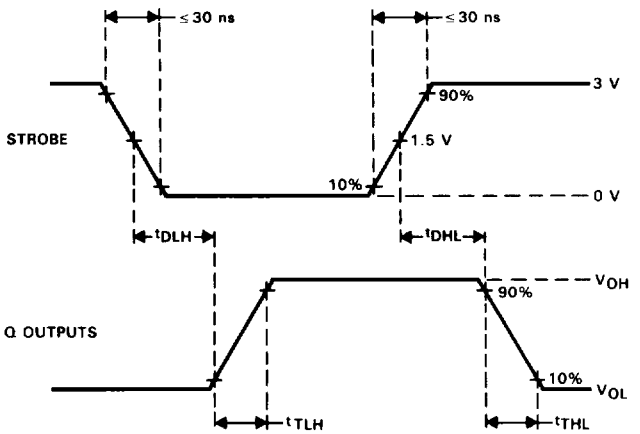


FIGURE 2. SWITCHING-TIME VOLTAGE WAVEFORMS