



Half-Bridge N-Channel MOSFET Driver for DC/DC Conversion

FEATURES

- Gate Drive Supply Voltages of 8 V to 12 V
- Undervoltage Lockout
- Internal Bootstrap Diode
- PWM Pin Tristate Enable Feature
- Switching Frequency Up to 1 MHz
- 30-ns Max Propagation Delay
- Drive MOSFETs In 5- to 50-V Systems
- Adaptive Shoot-Through Protection

APPLICATIONS

- Multi-Phase DC/DC Conversion
- High Current Low Voltage DC/DC Converters
- High Frequency DC/DC Converters
- Mobile and Desktop Computer DC/DC Converters
- Core Voltage Supplies for PC Micro-Processors

DESCRIPTION

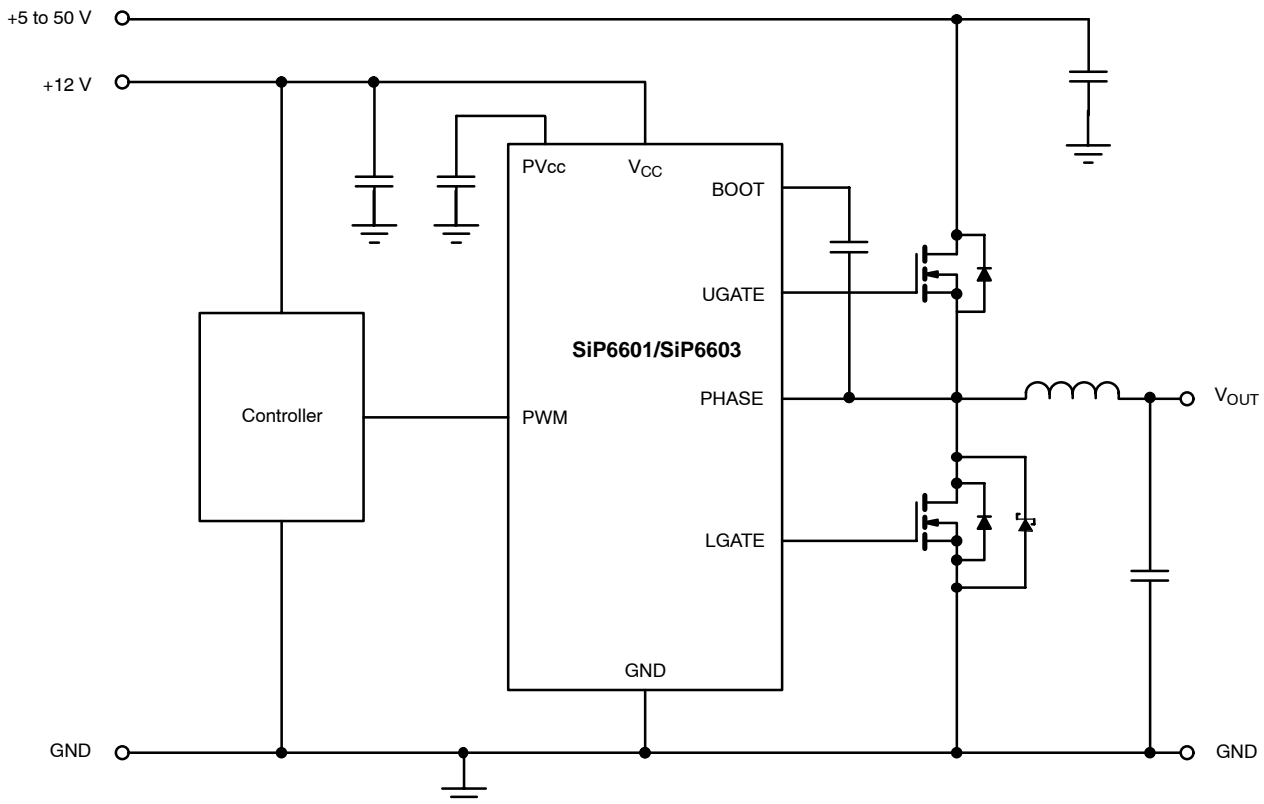
The SiP6601 and SiP6603 are high-speed half-bridge MOSFET drivers for use in high frequency, high current, multiphase dc-to-dc synchronous rectifier buck power supplies. They are designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving n-channel MOSFETs.

They feature adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs. There are two options available for the voltage of the high-side and

low-side drivers. In the SiP6601, the regulator supplies gate drive voltage to the high-side driver and V_{CC} supplies the low-side driver. In the SiP6603, the regulator supplies the high- and low-side gate drive voltage.

The SiP6601 and SiP6603 are available in a lead (Pb)-free 8-pin SOIC package for operation over the industrial operating range ($-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$).

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{CC}, PV_{CC}	-0.3 to 15 V	Thermal Impedance (θ_{JA}) ^b	
BOOT, PHASE	-0.3 to 55 V	SO-8	130°C/W
BOOT to PHASE	-0.3 to 15 V	Notes	
Storage Temperature	-40 to 150°C	a. Device mounted with all leads soldered or welded to PC board.	
Operating Junction Temperature	125°C	b. Derate 7.7 mW/°C	
Power Dissipation ^a			
SO-8	770 mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{CC}	10.8 to 13.2 V	BOOT to PHASE	13.2 V
V_{BOOT}85 to 50 V	Operating Temperature Range	-40 to 85°C

SPECIFICATIONS^a

Parameter	Symbol	Test Conditions Unless Specified $V_{CC} = 12\text{ V}, V_{BOOT} - V_{PHASE} = 8\text{ V}$ $T_A = -40\text{ to }85^\circ\text{ C}$		Limits			Unit
				Min ^a	Typ ^b	Max ^a	
Power Supplies							
Supply Voltage	V_{CC}			10.8		13.2	V
Supply Quiescent	I_{CCQ}		$f_{PWM} = 1\text{ MHz}, C_{LOAD} = 0$			12.0	mA
Tristate (Shutdown) Current	I_{CCT}		PWM = Open		850	1200	μA
Reference Voltage							
Break-Before-Make	V_{BBM}				2.5		V
PWM Input							
Input High	V_{IH}			4.5		V_{CC}	V
Input Low	V_{IL}					0.5	
Bias Current	I_B				± 600	± 1000	μA
Tristate Threshold	High	V_{TSH}		3.0			V
	Low	V_{TSL}				2.0	
Tristate Holdoff Timeout ^c	t_{TST}				240		ns
Bootstrap Diode							
Forward Voltage	V_F		$I_F = 40\text{ mA}, T_A = 25^\circ\text{ C}$	0.70	0.85	1.0	V
MOSFET Drivers							
High-Side Drive Current ^c	$I_{PKH}(\text{source})$	$V_{BOOT} - V_{PHASE} = 8\text{ V}$			0.8		A
	$I_{PKH}(\text{sink})$				1.0		
Low-Side Drive Current ^c	$I_{PKL}(\text{source})$	$V_{PVCC} = 8\text{ V}$	SiP6603		0.9		
	$I_{PKL}(\text{sink})$				1.2		
	$I_{PKL}(\text{source})$	$V_{PVCC} = 12\text{ V}$	SiP6601		1.4		
	$I_{PKL}(\text{sink})$				1.8		
High-Side Driver Impedance	$R_{DH}(\text{source})$	$V_{BOOT} - V_{PHASE} = 8\text{ V}, \text{ PHASE} = \text{GND}$			2.3	3.5	Ω
	$R_{DH}(\text{sink})$				2.1	3.2	
Low-Side Driver Impedance	$R_{DL}(\text{source})$	$V_{PVCC} = 8\text{ V}$	SiP6603		2.9	4.4	
	$R_{DL}(\text{sink})$				1.3	2.2	
	$R_{DL}(\text{source})$	$V_{PVCC} = 12\text{ V}$	SiP6601		2.6	4.0	
	$R_{DL}(\text{sink})$				1.3	2.2	

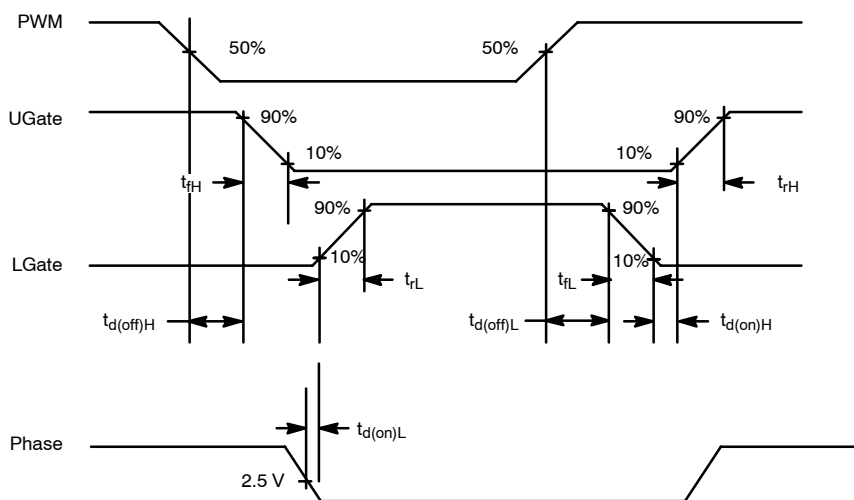


SPECIFICATIONS ^a							
Parameter	Symbol	Test Conditions Unless Specified $V_{CC} = 12\text{ V}$, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $T_A = -40\text{ to }85^\circ\text{C}$		Limits			Unit
				Min ^a	Typ ^b	Max ^a	
MOSFET Drivers							
High-Side Rise Time	t_{rH}	10% – 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$, $C_{LOAD} = 3\text{ nF}$			40		ns
High-Side Fall Time	t_{fH}				30		
High-Side Rise Time Bypass		10% – 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$, $C_{LOAD} = 3\text{ nF}$			35		
High-Side Fall Time Bypass					25		
High-Side Propagation Delay ^c	$t_{d(off)H}$	See Timing Waveforms			25		
	$t_{d(on)H}$				25		
Low-Side Rise Time	t_{rL}	10% – 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP6603		35		
		10% – 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP6601		30		
Low-Side Fall Time	t_{fL}	10% – 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP6603		30		
		10% – 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP6601		25		
Low-Side Propagation Delay ^c	$t_{d(off)L}$	See Timing Waveforms			20		
	$t_{d(on)L}$				20		
PHASE Timer							
PHASE Falling Timeout ^c	t_{PHASE}				380		ns
PV_{CC} Regulator							
Output Voltage	PV_{CC}			7.6	8	8.4	V
Output Current						100	mA
Line Regulation		$V_{CC} = 10.8\text{ V to }13.2\text{ V}$			0.2	0.5	%/V
Load Regulation		5 mA to 80 mA			0.5	2.0	%
PV_{CC} Regulator UVLO							
PV _{CC} Rising	V_{UVLO2}				6.7	7.2	V
PV _{CC} Falling					6.4	6.9	
Hysteresis	Hyst			100	300	500	mV
High-Side Undervoltage Lockout							
Threshold	V_{UVHS}	Rising or Falling		2.5	3.35	4.0	V
V_{CC} Undervoltage Lockout							
Threshold	V_{UVLO1}			5.0	5.3	5.6	V
Power on Reset Time					2.5		ms
Thermal Shutdown							
Temperature	T_{SD}	Temperature Rising			165		°C
Hysteresis	T_H	Temperature Falling			25		

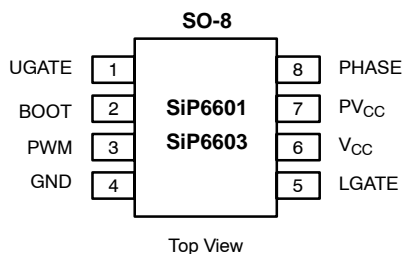
Notes

- a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at $V_{CC} = 12\text{ V}$ unless otherwise noted.
- c. Guaranteed by design.

TIMING WAVEFORMS



PIN CONFIGURATION AND TRUTH TABLE



TRUTH TABLE		
PWM	UGATE	LGATE
L	L	H
H	H	L
TriState	L	L

ORDERING INFORMATION

Part Number	Temperature Range	Marking
SiP6601DY-T1—E3	-40 to 85°C	6601
SiP6603DY-T1—E3		6603

Eval Kit	Temperature Range
SiP6601DB	-40 to 85°C
SiP6603DB	

PIN DESCRIPTION

Pin Number	Name	Function
1	UGATE	High-side MOSFET gate drive
2	BOOT	Bootstrap supply for high-side driver. The bootstrap capacitor is connected between BOOT and PHASE.
3	PWM	Input signal for the MOSFET drivers
4	GND	Ground
5	LGATE	Synchronous or low-side MOSFET gate drive
6	V _{CC}	12-V supply. Connect a bypass capacitor (1-μF min) from here to ground
7	PV _{CC}	8-V Voltage Regulator Output. Connect a bypass capacitor (1-μF min) from here to ground
8	PHASE	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor

FUNCTIONAL BLOCK DIAGRAM

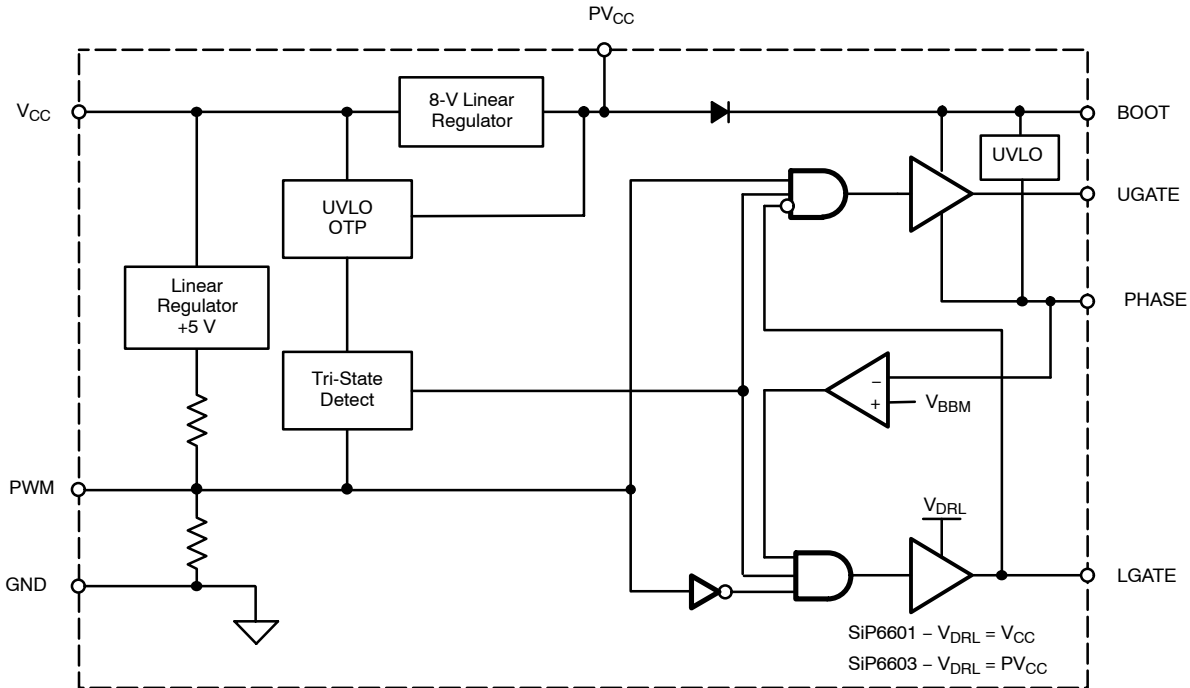


Figure 1.

DETAILED OPERATION

PWM

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (<200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached.

Shutdown

The SiP6601/03 enters shutdown mode when the signal driving PWM enters HiZ or “tristate” mode for more than 240 ns. If the PWM pin is left open, the pin is held to 2.5 V by an internal voltage divider, thus forcing the the “tristate” mode.

Low-Side Driver

In the SiP6601, the low-side driver voltage is supplied by V_{CC}. In the SiP6603, the low-side driver voltage is supplied by PV_{CC}. During shutdown, LGATE is held low.

High-Side Driver

The high-side driver is isolated from the substrate to create a floating high-side driver so that an n-channel MOSFET can be

used for the high-side switch. The high-side driver voltage is supplied by PV_{CC}. The voltage is maintained by a floating bootstrap capacitor, which is continually recharged by the switching action of the output. During shutdown UGATE is held low.

Gate Drive Voltage (PV_{CC}) Regulator

An integrated 80-mA, 8-V regulator supplies voltage to the PV_{CC} pin. A capacitor (1 μF minimum) must be connected to the PV_{CC} pin to stabilize the regulator output. The voltage on PV_{CC} is supplied to the integrated bootstrap diode. PV_{CC} is used to recharge the bootstrap capacitor and can be used to power the low-side driver.

Bootstrap Circuit

The internal bootstrap diode and an external bootstrap capacitor supply voltage to the BOOT pin. An integrated bootstrap diode replaces the external diode normally needed for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to,

$$C_{BOOT} = (Q_{GATE} / (\Delta V_{BOOT} - V_{PHASE})) \times 10$$

where Q_{GATE} is the gate charge needed to turn on the high-side MOSFET and $\Delta V_{BOOT-PHASE}$ is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1 μF to 1 μF . The bootstrap capacitor voltage rating must be greater than $V_{CC} + 12\text{ V}$ to withstand transient spikes and ringing.

Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the PHASE pin and the LGATE pin and control the switching as follows: When the signal on PWM goes low, UGATE will go low after an internal propagation delay. After the voltage on PHASE falls below 2.5 V by the inductor action, the low-side driver is enabled and LGATE goes high after some delay. When the signal on PWM goes high, LGATE will go low after an internal propagation delay. After the voltage on LGATE drops below 2.5 V the high-side driver is enabled and UGATE will go high after an internal propagation delay. If PHASE does not drop below 2.5 V within 380 ns after UGATE goes low, LGATE is forced high until the next PWM transition.

V_{CC} Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1- μF ceramic capacitor as close as practical between the V_{CC} and GND pins.

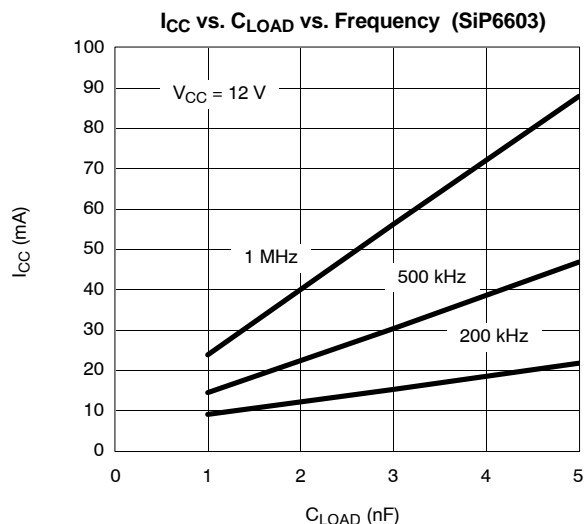
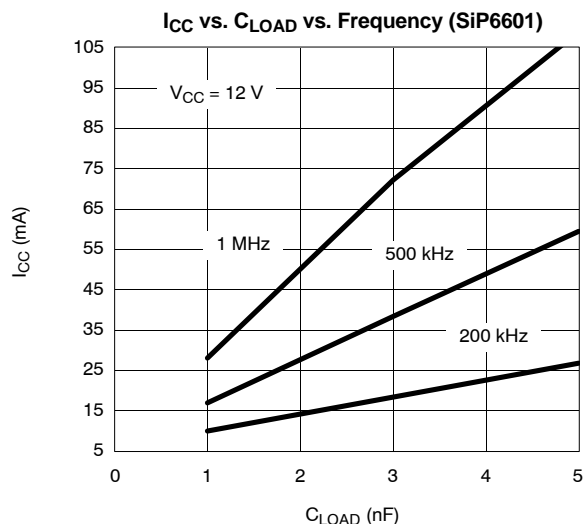
Undervoltage Lockout

Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces LGATE and UGATE to low when V_{CC} is below its specified voltage. A separate UVLO forces UGATE low when the voltage between BOOT and PHASE is below the specified voltage.

Thermal Protection

If the die temperature rises above 165°C, the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140°C.

TYPICAL CHARACTERISTICS



TYPICAL WAVEFORMS

Figure 2. PWM Signal vs. HS Gate, LS Gate and PHASE (Rising)

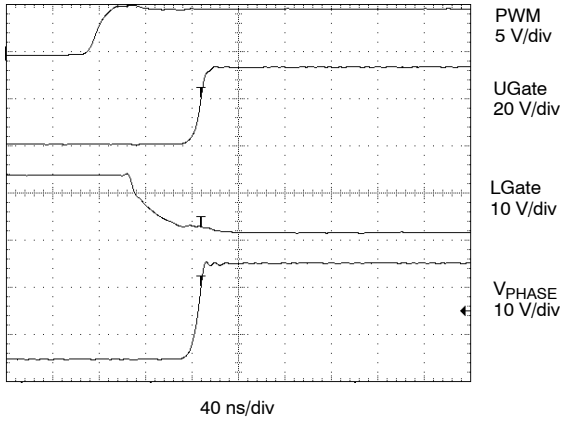
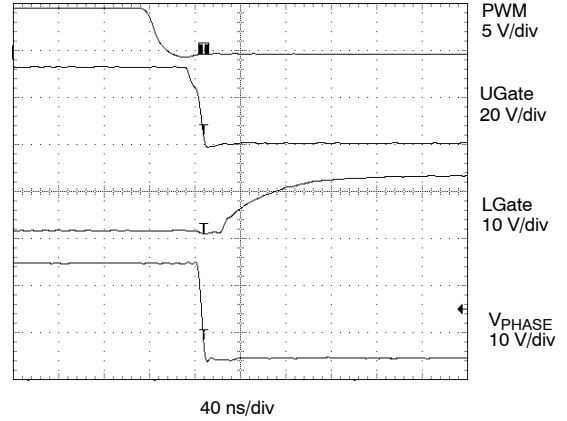


Figure 3. PWM Signal vs. HS Gate, LS Gate and PHASE (Falling)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73023>.