OKI Semiconductor

MSM6549

160-DOT SEGMENT DRIVER (TCP)

GENERAL DESCRIPTION

The MSM6549 is an LCD dot matrix segment driver of a CMOS IC which consists of a 160-bit unidirectional shift register, a 160-bit latch circuit, each bit level shifter, and a 4-level driver. The MSM6549 latches display data, which is transferred from a microcomputer or a liquid crystal display controller in 4-bit parallel, and generates a liquid crystal driver signal.
It has a power-save function, to put all drivers except one, independently of the number of drivers, into the low supply current state (I_{DD} SBY). The bias voltage to specify the drive level can optionally be supplied externally. The MSM6549 is suitable for driving various liquid crystal display panels.

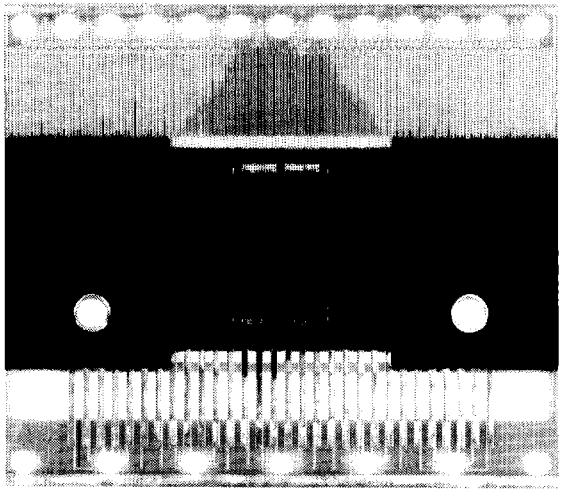
FEATURES

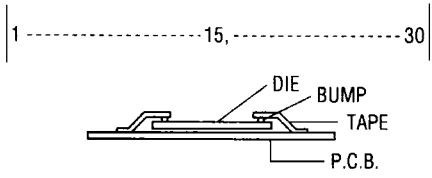
- Logic supply voltage : 4.5 to 5.5V
- Liquid crystal drive voltage : A wide range from 20 to 40V
- Suitable for liquid crystal panels using a duty ratio of 1/200 to 1/480
- The bias voltage can be externally supplied.
- Liquid crystal output : 160
- The power-save function can reduce power consumption of a large-screen liquid crystal panel unit.
- The 4-bit parallel data transfer reduces its transfer speed to 1/4 of that of conventional serial transfer, and enables low power consumption.
- An LCD controller MSM6355 can be interfaced with the MSM6549.

STRUCTURE

- Film width 35mm, TAB mounting
- Gold or solder plating

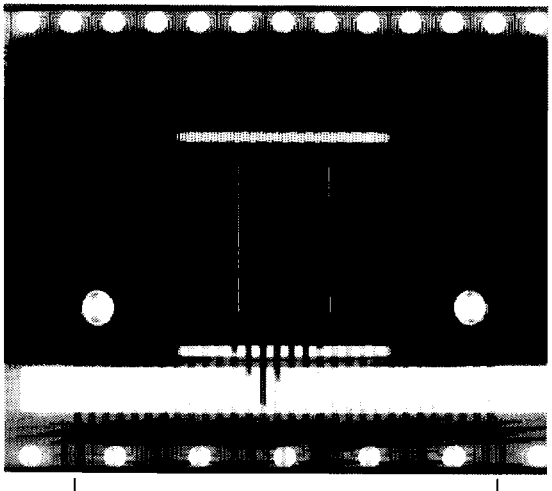
FACE-UP TYPE

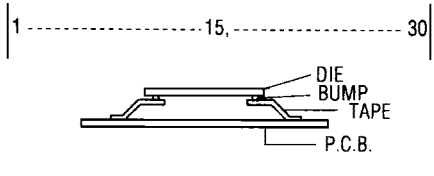




Pin No.	Pin Name	Pin No.	Pin Name
1	NC	16	NC
2	OUT160	17	NC
3	EI	18	D3
4	V1L	19	D2
5	V3L	20	D1
6	V4L	21	D0
7	VEEL	22	CP
8	NC	23	NC
9	V_{DD}	24	VEER
10	V_{SS}	25	V4R
11	DF	26	V3R
12	DISP OFF	27	V1R
13	LOAD	28	E0
14	NC	29	OUT1
15	NC	30	NC

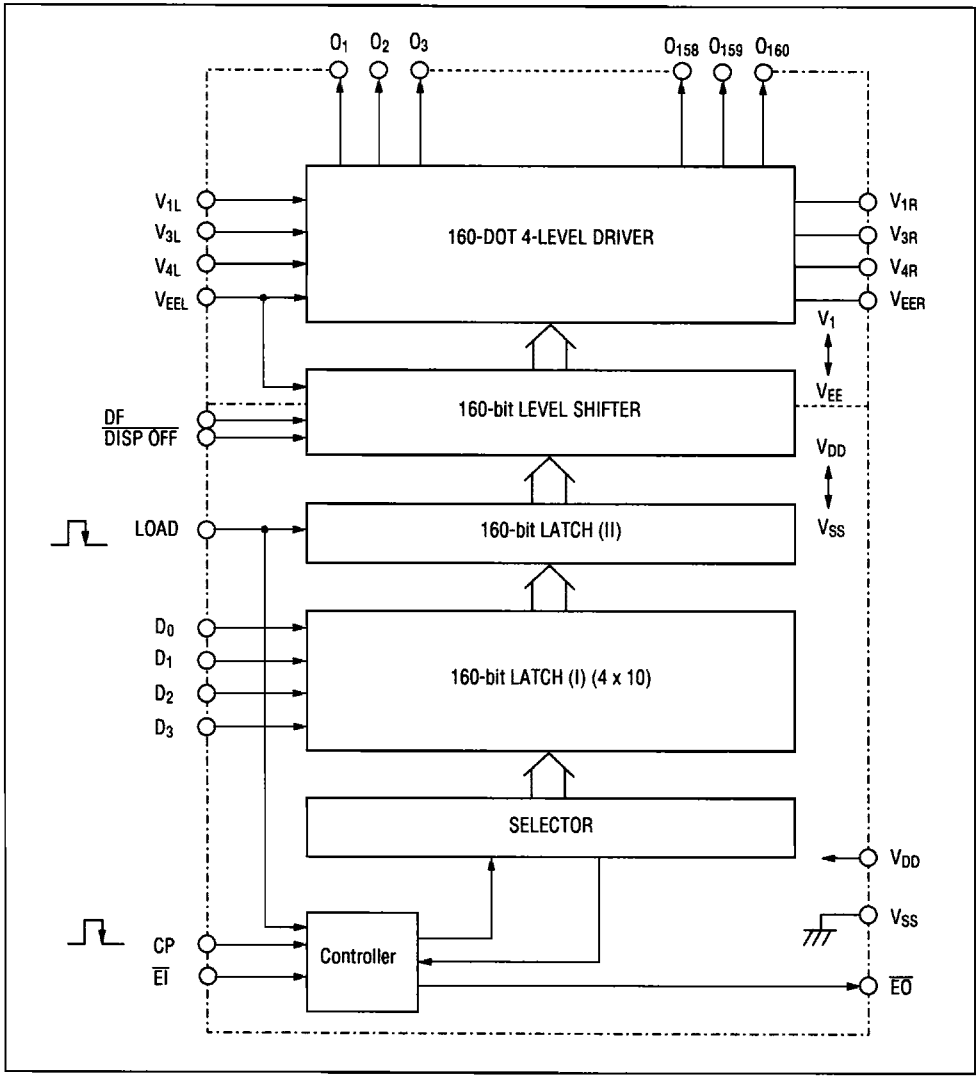
FACE-DOWN TYPE





Pin No.	Pin Name	Pin No.	Pin Name
1	NC	16	NC
2	OUT1	17	NC
3	E0	18	LOAD
4	V1R	19	DISP OFF
5	V3R	20	DF
6	V4R	21	V_{SS}
7	VEER	22	V_{DD}
8	NC	23	NC
9	CP	24	VEEL
10	D0	25	V4L
11	D1	26	V3L
12	D2	27	V1L
13	D3	28	EI
14	NC	29	OUT160
15	NC	30	NC

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

DF	LATCH DATA	$\overline{\text{DISP OFF}}$	DRIVER OUT (O_1~O_{160})
L	L	H	V_3
L	H	H	V_1
H	L	H	V_4
H	H	H	V_{EE}
X	X	L	V_1

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

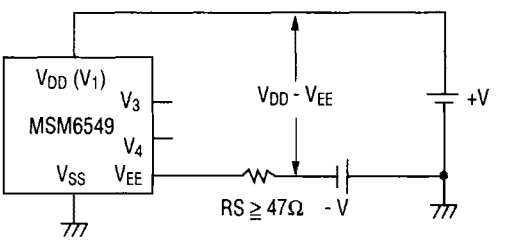
Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage (1)	V_{DD}	T_a = 25°C	-0.3 ~ 6	V
Power Supply Voltage (2)	V_{DD} - V_{EE} *1	T_a = 25°C	0 ~ 40	V
	V_{DD} - V_{EE} *1 *2	T_a = 25°C	0 ~ 42	
Input Voltage	V_I	T_a = 25°C	-0.3 ~ V_{DD}+0.3	V
Storage Temperature	T_{stg}	-	-40 ~ +150	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

*2 A resistor of 47 ohm or higher is connected in series between V_{EE} and the supply voltage as shown in the right figure.

$V_1 = V_{1L} + V_{1R}$ $V_3 = V_{3L} + V_{3R}$

$V_4 = V_{4L} + V_{4R}$ $V_{EE} = V_{EEL} + V_{EER}$



• Operating Range

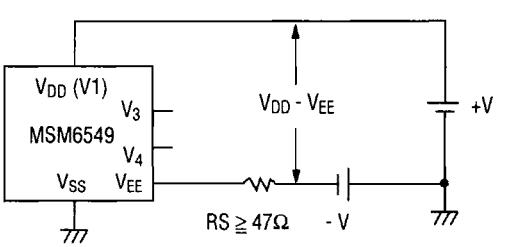
Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage (1)	V_{DD}	-	4.5 ~ 5.5	V
Power Supply Voltage (2)	V_{DD} - V_{EE} *1	-	25 ~ 38	V
	V_{DD} - V_{EE} *1 *2	-	25 ~ 40	
Operating Temperature	Top	-	-20 ~ +75	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

*2 A resistor of 47 ohm or higher is connected in series between V_{EE} and the supply voltage as shown in the right figure.

$V_1 = V_{1L} + V_{1R}$ $V_3 = V_{3L} + V_{3R}$

$V_4 = V_{4L} + V_{4R}$ $V_{EE} = V_{EEL} + V_{EER}$



• DC Characteristics

(V_{DD} = 5V ±10%, Ta = -20 ~ +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max	Unit
"H" Input Voltage	V_{IH} *1	-	0.8V_{DD} -	-	-	V
"L" Input Voltage	V_{IL} *1	-	-	-	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	V_{IH} = V_{DD} V_{DD} = 5.5V	-	-	1	µA
"L" Input Current	I_{IL} *1	V_{IL} = 0V V_{DD} = 5.5V	V_{DD} - 0.4	-	-1	µA
"H" Output Voltage	V_{OH} *2	I_O = -0.2mA V_{DD} = 4.5V	-	-	-	V
"L" Output Voltage	V_{OL} *2	I_O = 0.2mA V_{DD} = 4.5V	-	-	0.4	V
ON Resistance	R_{ON} *4	V_{DD} - V_{EE} = 35V V_{DD} = 4.5V IV_N - V_OI = 0.25V *3	-	-	3	kΩ
Stand-by Supply Current	I_{DD} SBY	CP = 6.0MHz V_{DD} = 5.5V V_{DD} - V_{EE} = 35V No Load *5	-	2.0 / 0.3	4.0 / 0.6	mA
Supply Current (1)	I_{DD1}	CP = 6.0MHz V_{DD} = 5.5V V_{DD} - V_{EE} = 35V No Load *6	-	3.0 / 1.0	6.0 / 2.0	mA
Supply Current (2)	IV	CP = 6.0MHz V_{DD} = 5.5V V_{DD} - V_{EE} = 35V No Load *7	-	-	200	µA
Input Capacity	C_I	f = 1MHz		5	-	pF

*1 Applicable to pins LOAD, CP, D0 ~ D3, $\overline{EI}$, DF, $\overline{DISP\ OFF}$

*2 Applicable to pin $\overline{EO}$

*3 VN = V_{DD} ~ V_{EE}, V_4 = 19/21(V_{DD} - V_{EE}), V_3 = 2/21(V_{DD} - V_{EE}), V_{DD} = V_1

*4 Applicable to pins O_1 to O_{160}

*5 Display data 1010 : DF=45Hz, current flowing from V_{DD} to V_{SS} when no data is fetched

1st Stage
2nd Stage

*6 Display data 1010 : DF=45HZ, current from V_{DD} to V_{EE} or from V_{DD} to V_{SS} when data is fetched

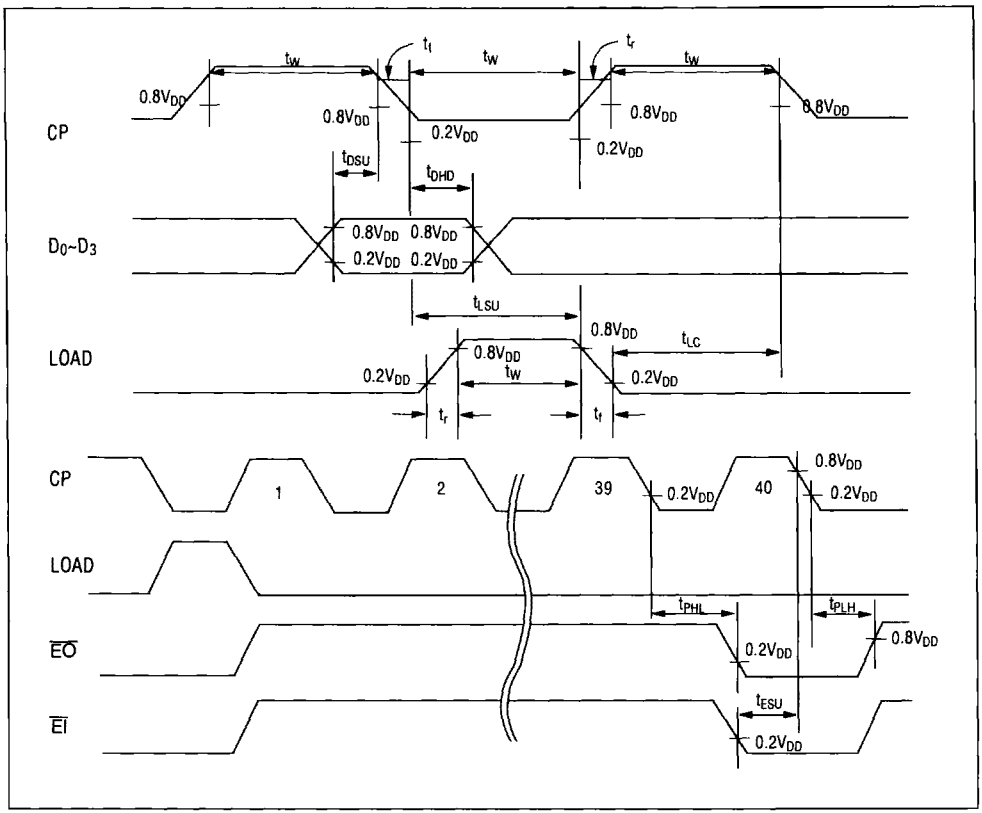
V_{DD}
V_{EE}

*7 Display data 1010 : DF=45Hz, current flowing through each of pins V_1, V_3, V_4, and V_{EE}

• AC Characteristics

(V_{DD} = 5V ±10%, Ta = -20 ~ +75°C, CL = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum clock frequency	f_{CP}	DUTY = 50%	8	-	-	MHz
Clock load pulse width	t_W	-	50	-	-	ns
Rising/Falling time	t_r, t_f	-	-	-	20	ns
Data set-up time	t_{DSU}	-	30	-	-	ns
Data hold time	t_{DHD}	-	50	-	-	ns
Load pulse width	t_W	-	63	-	-	
Load set-up time	t_{LSU}	-	80	-	-	ns
Load → Clock time	t_{LC}	-	80	-	-	ns
Propagation delay time	t_{PLH} t_{PHL}	-	-	-	100	ns
$\overline{EI}$ set-up time	t_{ESU}	-	25	-	-	ns



PIN DESCRIPTION

- **$\overline{EI}$**
  This is a control input pin for the enable F/F of the IC. When the pin goes high, the built-in counter stops. When the pin goes low, the counter is ready for operation.

- **$\overline{EO}$**
  This is an output pin for the enable F/F of the IC. When a cascade connection is required, connect this pin to the EI pin on the next stage.
  When the internal counter is reset by a load pulse, the pin goes high simultaneously. When Serial or Parallel is selected by a shift clock pulse, which is input from the CP pin, and 160 bits are converted, this output pin goes low and the internal counter stops. The pin waits for the next load pulse.
  For cascade connection, see the application circuit example.

- **CP**
  This is a 4-bit parallel shift register clock input pin. Data is shifted at the trailing edge of a clock pulse.
  A clock pulse from this pin is valid when the enable F/F is in the set state, while invalid when it is in the non-set state.

- **LOAD**
  This is an input pin to latch the display data stored in the shift register. At the trailing edge of a load pulse, the display data stored in the shift register is latched. At the trailing edge ($\_\square\!\!\downarrow\_$) of a load pulse, the built-in counter of this IC is reset.

- **DF**
  This is an input pin for a liquid crystal drive waveform AC synchronization signal, which generally inputs a frame inversion signal.

- **V_{DD}, V_{SS}**
  These are power pins of this IC. The V_{DD} pin is generally set to 4.5 to 5.5V. V_{SS} is a grounding pin, which is generally set to 0V.

  Take note when turning power on and off
  The liquid crystal drive on this IC chip requires a high voltage. When a high voltage is applied to it with the logic power supply floated, an overcurrent flows. This may damage the IC chip. Be sure to carry out the following power-on and power-off sequences:

  When turning power on:
  First V_{DD} ON, next V_{EE}, V_4, V_3, V_1 ON. Or both at the same time.

  When turning power off:
  First V_{EE}, V_4, V_3, V_1 OFF, next V_{DD} OFF. Or both at the same time.

- **V_{1L}, V_{3L}, V_{4L}, V_{EEL}, V_{1R}, V_{3R},V_{4R}, V_{EER}**

These are liquid crystal drive bias voltage pins. Bias voltages by resistance division are generally used. Fig. 1 shows an example of supply of liquid crystal drive bias voltages by resistance division. The V_1 pin may be separated from the V_{DD} pin.
V_{1L} ~ V_{EEL} and V_{1R} ~ V_{EER} are connected as shown in Fig. 1, since they are not connected within IC.

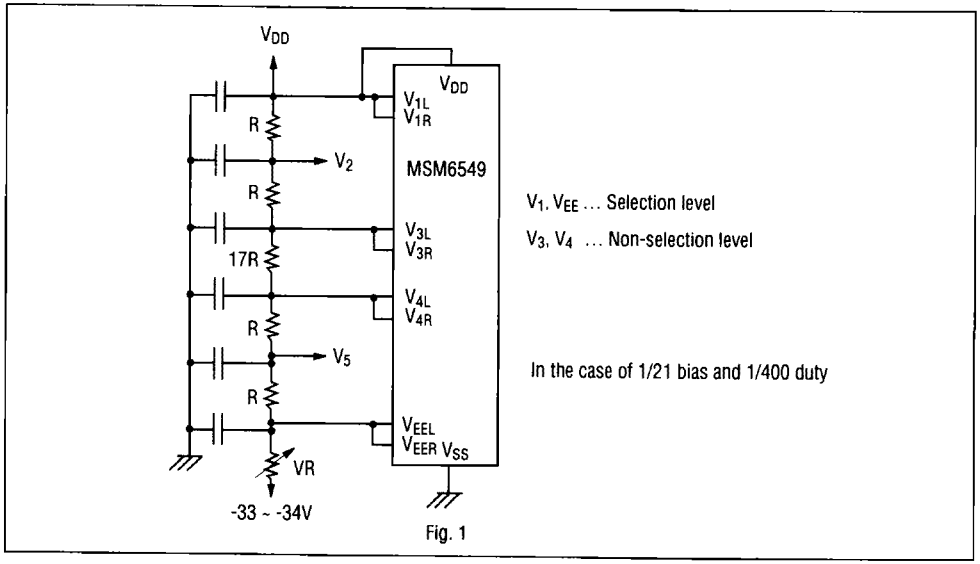


Fig. 1

Fig. 2 shows an example of supply of bias voltages using an operational amplifier. The use of an operational amplifier reduces the bias impedance and the supply current.

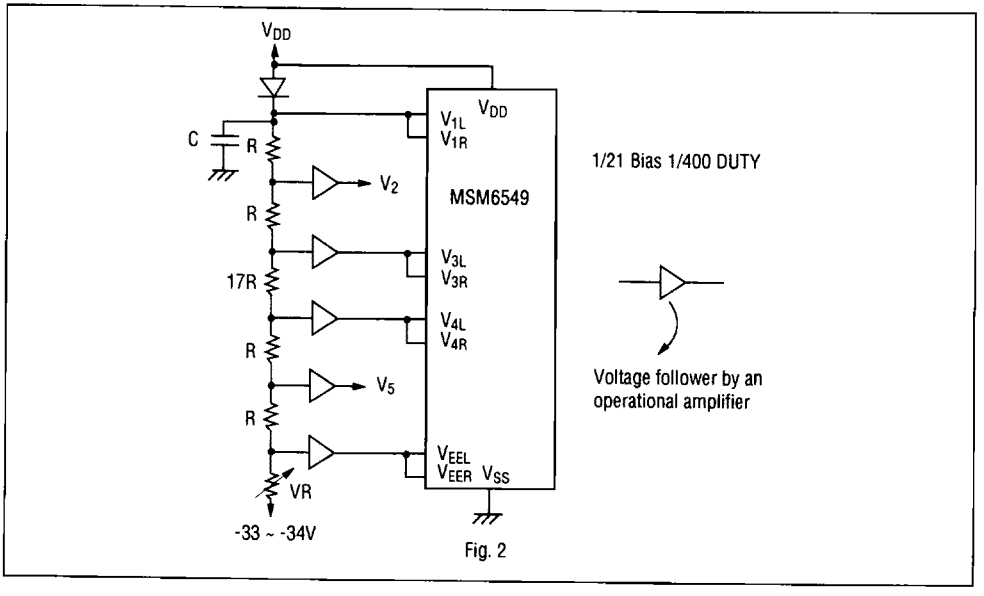


Fig. 2

- **D_0, D_1, D_2, D_3**

These are 4-bit parallel shift register data input pins. Display data is input in synchronization with a clock pulse. Table 1 gives the relation between D_0 to D_3 or DF and the liquid crystal drive output or liquid crystal display.

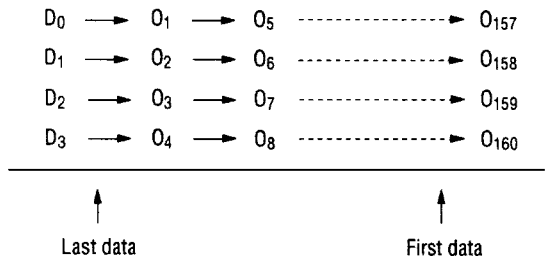
Table 1

D_0 ~ D_3	DF	Liquid crystal drive output		Liquid crystal display
L	L	Non-selection level	(V_3)	OFF
H	L	Selection level	(V_1)	ON
L	H	Non-selection level	(V_4)	OFF
H	H	Selection level	(V_{EE})	ON

Table 2 gives the relation between the display data input pins D_0, D_1, D_2, and D_3 and the liquid crystal drive output pins O_1 to O_{160}.

Table 2

Shift direction



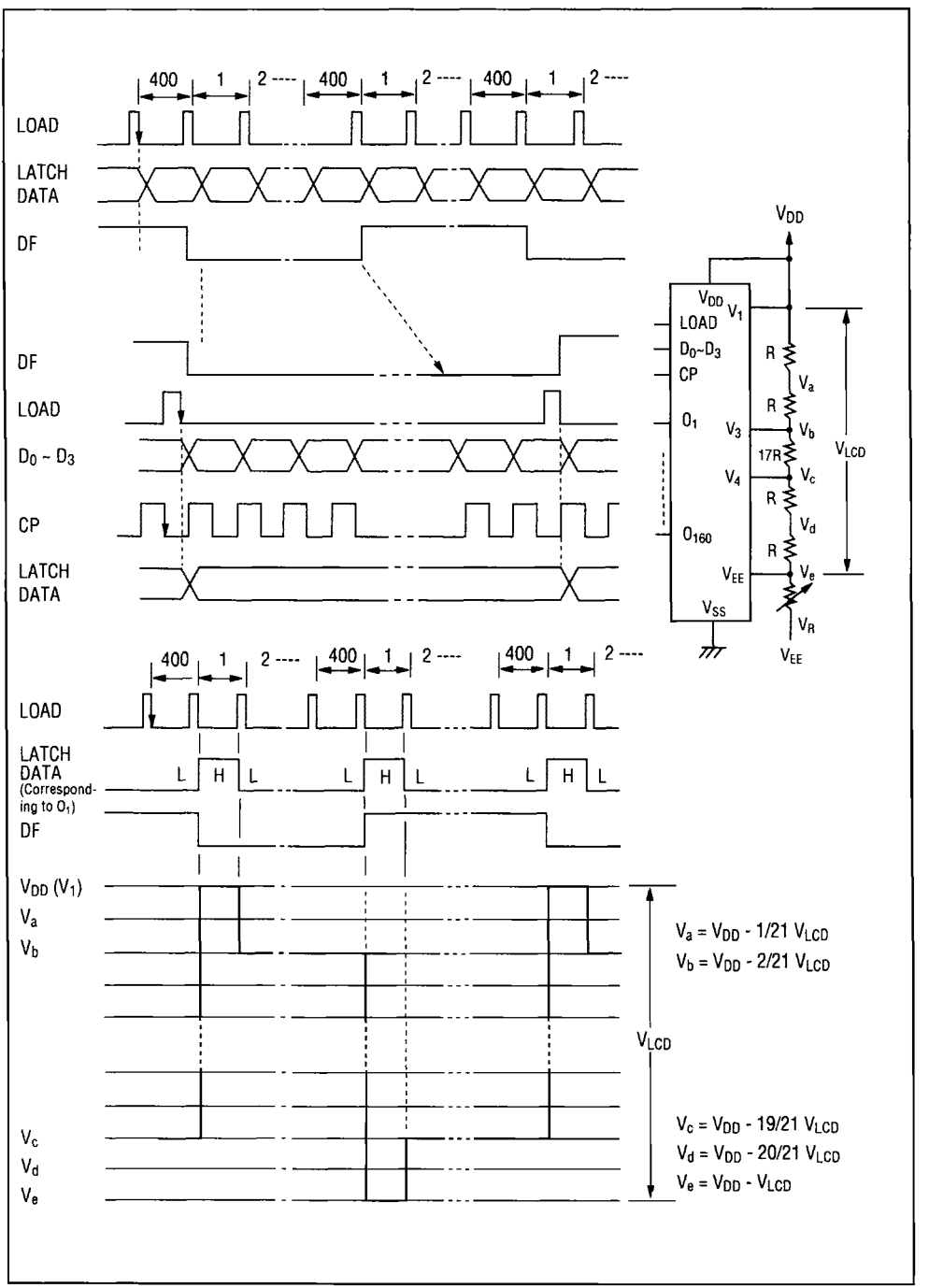
- **O_1 to O_{160}**

These are output pins of the 4-level driver of this IC, which correspond directly to the bits of the shift register. One of the four levels V_1, V_3, V_4, and V_{EE} is selected and output by a combination of the latch contents (display data) and a DF signal. See the truth table. Connect the output pins to the liquid crystal panel on the segment side.

- **$\overline{\text{DISP OFF}}$**

This is an input pin to control the output pins O_1 to O_{160}. During low signal input, signals on the V1 level are output from the output pins O_1 to O_{160}. See the truth table.

TIMING CHART (1/400 duty, 1/21 bias)



POWER SAVE FUNCTION

To reduce the power consumption in the case of cascade connection, an enable F/F is installed within the IC (see Fig. 1). When an IC contains this type of enable F/F, display data is transferred. An IC, which does not contain such an enable F/F, enters the non-fetch state and is kept in the low supply current (I_{DD}SBY). The enable F/F setting state is shifted to the next stage sequentially by the pins $\overline{EI}$ and $\overline{EO}$ and the internal counter so that the enable F/F exists in one IC.

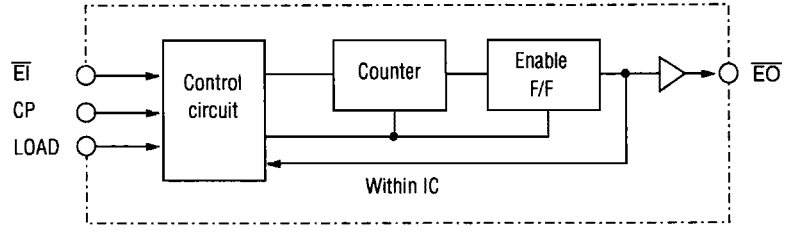
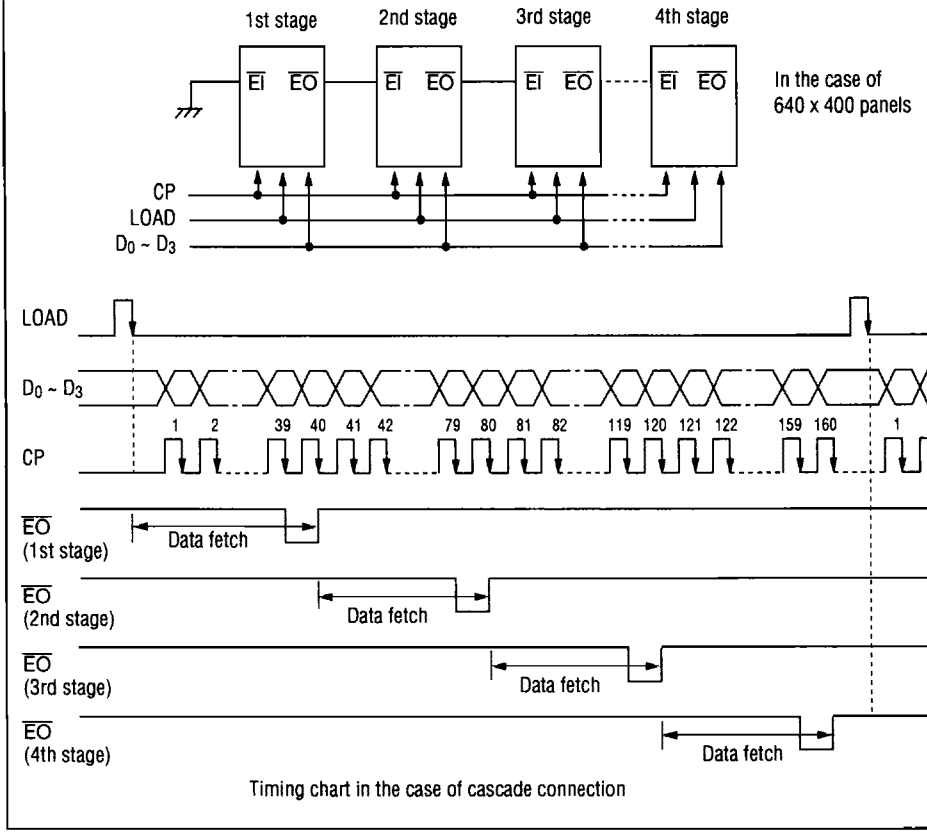


Fig. 1



Timing chart in the case of cascade connection

APPLICATION CIRCUIT