8288-A,F,W

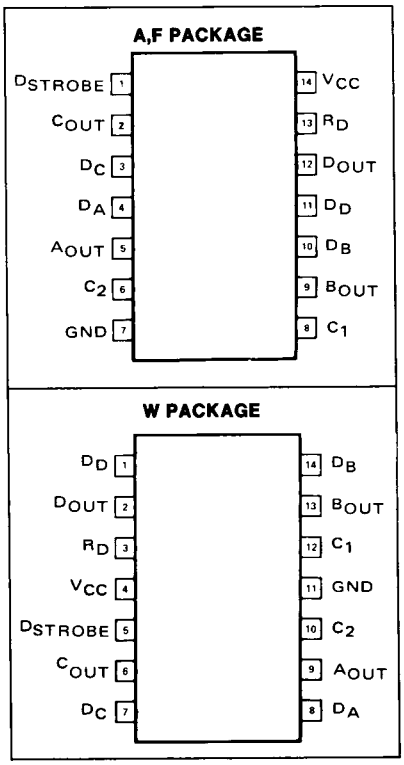
DESCRIPTION

The 8288 Divide by Twelve Counter is a four-bit subsystem consisting of divide by two and divide by six counters in a 14 pin package. For Divide-by-Twelve operation, output A is connected externally to the clock 2 input.

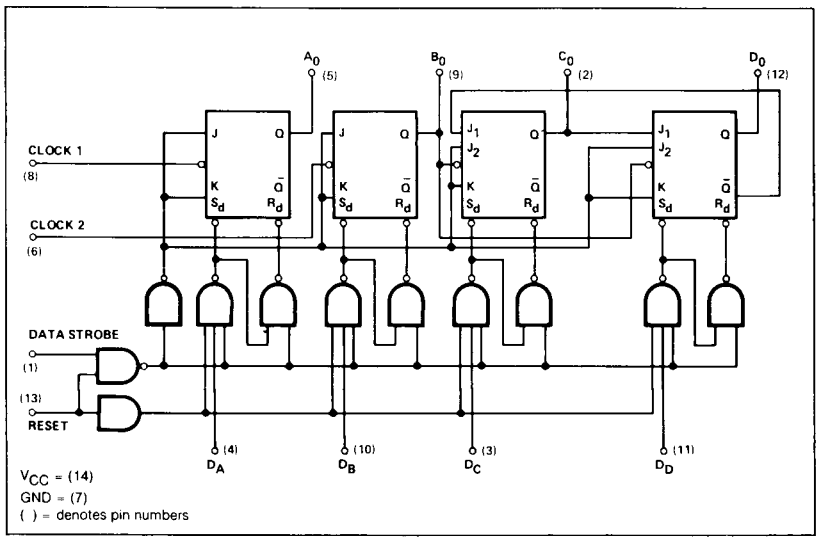
The 8288 has strobed paralleled data entry capability so that the counter may be preset to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at a "0" level. For additional flexibility, the 8288 is provided with a common reset. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative going) edge of the input clock pulse, however, there is no restriction on transition time since the individual binaries are level sensitive. The data strobe and reset functions are asynchronous with respect to the clock.

PIN CONFIGURATION



LOGIC DIAGRAM



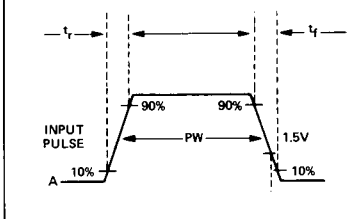
TRUTH TABLE

	OUTPUT			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

PARAMETER		TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_{on}	Turn-on delay time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			20	35	
t_{off}	Turn-off time					
	Clock mode	Bit A,B,C,D		15	25	ns
	Data/strobe			25	40	
Toggle rate			20	25		MHz
t_{hold}	Hold time	V_{IN} = 0.8V:Reset=2V:				
	Strobe	Clock 1 = 2V: Clock 2 = Output A		25	35	ns
	Reset	Data strobe = 2V: V_{IN} = 0.8V: Clock 1 = 2V: Clock 2 = Output A		20	35	
$t_{release}$	Release time			30	40	ns
	Strobe					
	Reset			50	75	

AC WAVEFORMS

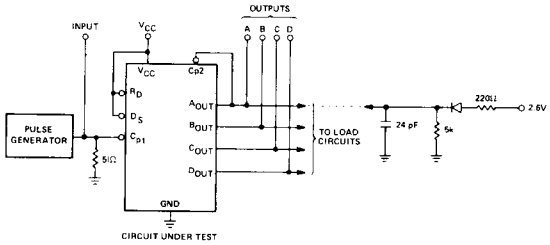


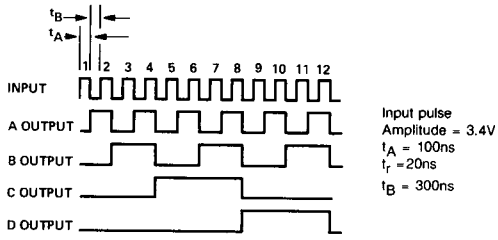
NOTE:
Input pulse notations apply unless otherwise specified.

LOGIC

AC TEST FIGURES AND WAVEFORMS

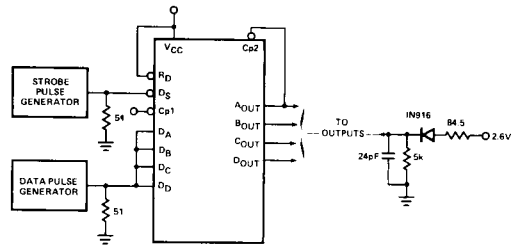
TOGGLE RATE

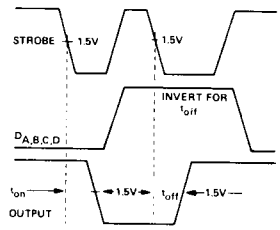




Input pulse
Amplitude = 3.4V
t_A = 100ns
t_r = 20ns
t_B = 300ns

DATA/STROBE t_{on} t_{off}

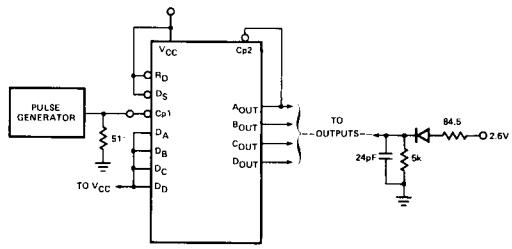


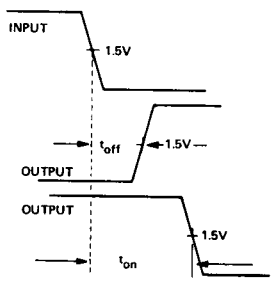


Input Pulse
Amplitude = 2.6V
t_r = t_f = 5ns

CLOCK MODE t_{on}/t_{off} DELAY

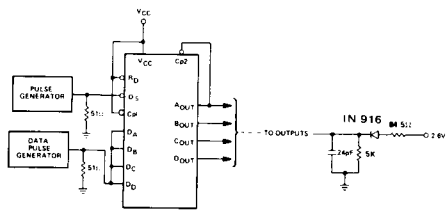
1. t_{on} and t_{off} are measured from the clock input of each binary to the Q output of that binary.
2. Each Q output will be loaded with the following load circuit:

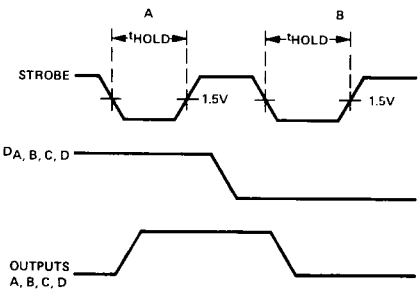




Input pulse:
Amplitude = 2.6V
P.W. = 30ns
t_r = t_f = 5ns

STROBE HOLD TIME





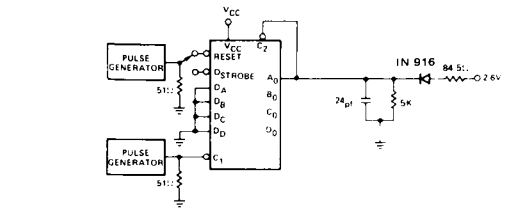
Input pulse
Amplitude=2.6V
t_r=t_f=5ns

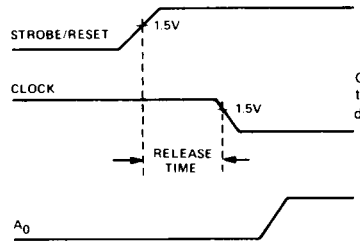
NOTES:
1. All resistor values are in ohms.
2. All capacitance values are in picofarads and include jig and probe capacitance.

8288-A,F,W

AC TEST FIGURES AND WAVEFORMS (CONT'D)

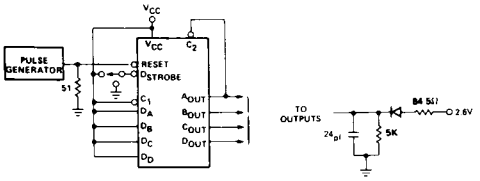
STROBE/RESET RELEASE TIME

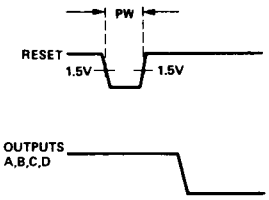




Clock, strobe/reset amplitude = 2.6V
$t_r = t_f$ = 5ns max. PRR = 1MHz 50% duty cycle.

MINIMUM RESET PULSE WIDTH





Input pulse:
Amplitude = 2.6V
$t_r = t_f$ = 5ns max.

Note: outputs must be previously brought high by placing a "0" on the D strobe input. A pulse generator may be substituted for the switch.

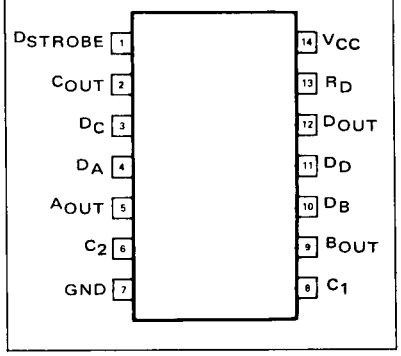
PRESETTABLE HIGH SPEED DECADE/BINARY COUNTER 8290/91

SPEED/PACKAGE AVAILABILITY

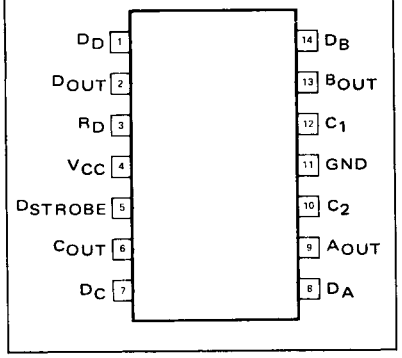
8290, 8291 A,F,W
82S90, 82S91 A,F

PIN CONFIGURATION

8290/91 82S90/82S91
A,F PACKAGE



8290/91
W PACKAGE



PIN DESIGNATIONS

CP1	Clock input to counter first stage (active low going edge)
CP2	Clock input to counter last three stages (active low going edge)
DS	Data Strobe Input for enabling data entry (active low)
RS	Reset Input for resetting all stages and outputs to zero (active low)
DA, DB, DC, DD	Data Inputs
AO, BO, CO, DO	Data Outputs