

## 8M-WORD BY 64-BIT

## VIRTUAL CHANNEL SYNCHRONOUS DYNAMIC RAM MODULE

## UNBUFFERED TYPE

### Description

The MC-45V8AB641 is a 8,388,608 words by 64 bits virtual channel synchronous dynamic RAM module on which 8 pieces of 64M virtual channel SDRAM :  $\mu$ PD4565821 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

### Features

- 8,388,608 words by 64 bits organization
- Clock frequency and access time from CLK

★

Part number	Read latency	Clock frequency (MAX.)	Access time from CLK (MAX.)	Maximum supply current				
				Operating			Refresh	
				Prefetch	Restore	Channel read / write (Burst)	Auto	Self
MC-45V8AB641KF-A75	2	133 MHz	5.4 ns	680 mA		520 mA	1080 mA	8 mA
MC-45V8AB641KF-A10		100 MHz	6 ns	640 mA		400 mA	920 mA	
MC-45V8AB641KF-A15	1	67 MHz	12 ns	560 mA		320 mA	880 mA	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Dual internal banks controlled by BA0 (Bank Select)
- Programmable burst-length : 1, 2, 4, 8 or 16
- Programmable wrap sequence : sequential or interleave
- Prefetch read latency : 4
- Auto precharge and without auto precharge
- Auto refresh and self refresh
- Single 3.3 V  $\pm$  0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Unbuffered type
- Serial PD

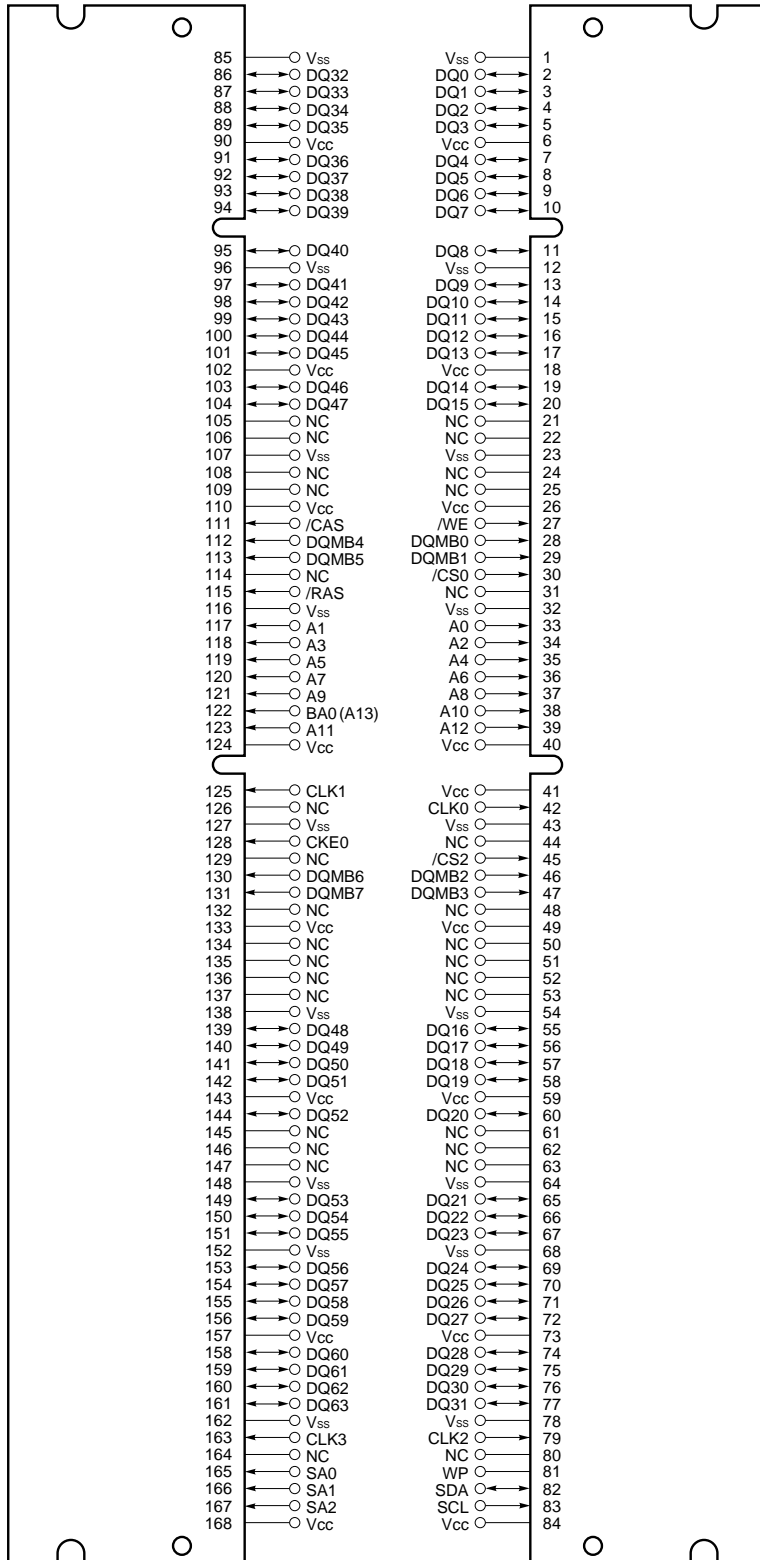
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ **Ordering Information**

Part number	Clock frequency MHz (MAX.)	Read latency	Prefetch read latency	Package	Mounted devices
MC-45V8AB641KF-A75	133 MHz	2	4	168-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 34.93 mm (1.375 inch) height	8 pieces of $\mu$ PD4565821G5 (400 mil TSOP (II))
MC-45V8AB641KF-A10	100 MHz				
MC-45V8AB641KF-A15	67 MHz	1			

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

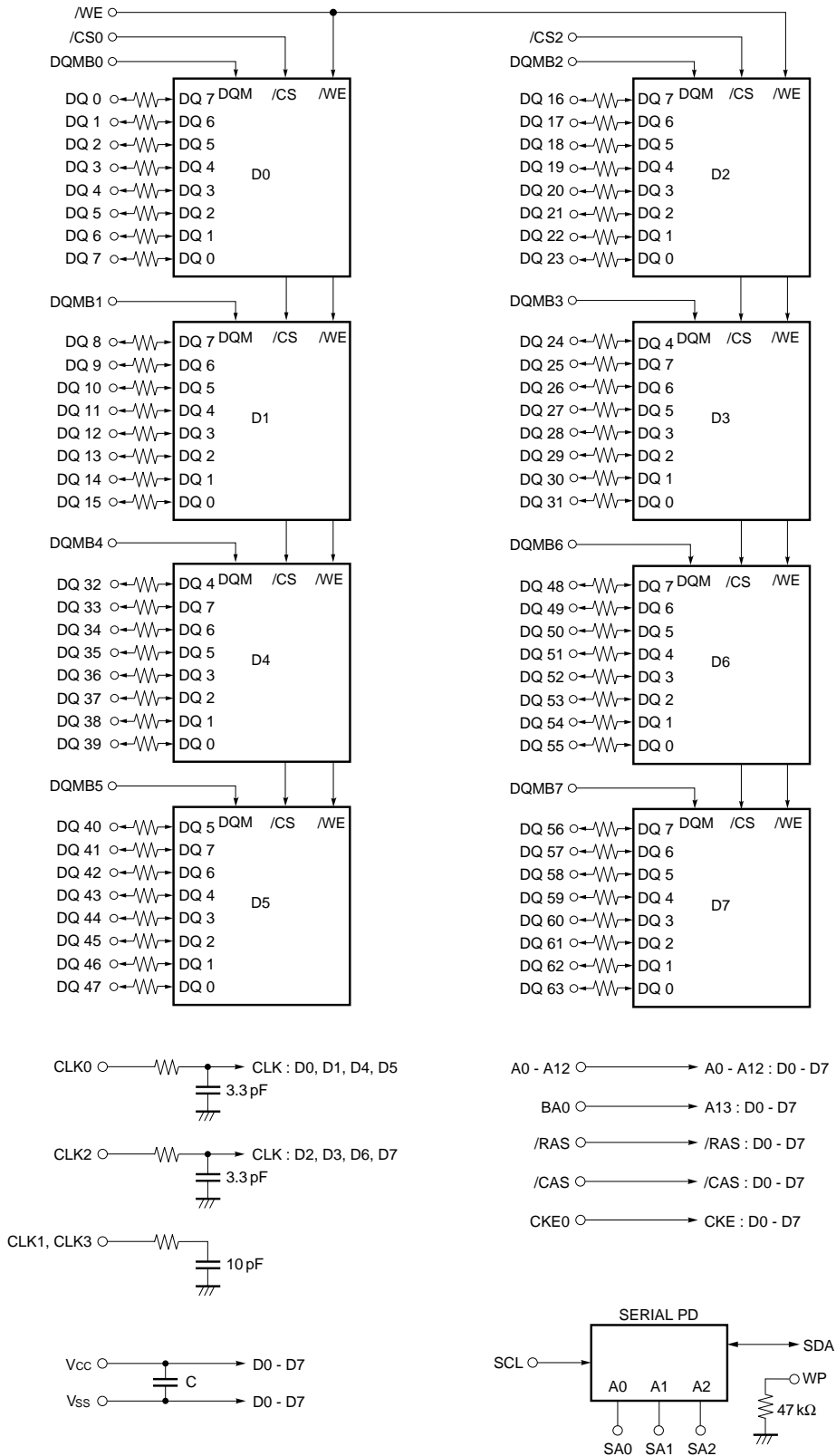


/xxx indicates active low signal.

- A0 - A12 : Address Inputs  
[Row: A0 - A12, Column: A0 - A6]
- BA0 (A13) : Virtual Channel SDRAM Bank Select
- DQ0 - DQ63 : Data Inputs/Outputs
- CLK0 - CLK3 : Clock Input
- CKE0 : Clock Enable Input
- /CS0, /CS2 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SA0 - SA2 : Address Input for EEPROM
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- WP : Write Protect <sup>Note</sup>
- NC : No Connection

**Note** WP is not used yet. It is connected to ground.

Block Diagram



- Remarks**
1. The value of all resistors is 10 Ω except WP.
  2. WP is not used yet. It is connected to ground.
  3. D0 - D7: μPD4565821 (4M words × 8 bits × 2 banks)

**Electrical Specifications**

- All voltages are referenced to V<sub>SS</sub> (GND).
- After power up, wait more than 100  $\mu$ s and then, execute power on sequence and auto refresh before proper device operation is achieved.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V <sub>CC</sub>		-0.5 to +4.6	V
Voltage on input pin relative to GND	V <sub>T</sub>		-0.5 to +4.6	V
Short circuit output current	I <sub>O</sub>		50	mA
Power dissipation	P <sub>D</sub>		8	W
Operating ambient temperature	T <sub>A</sub>		0 to +70	°C
Storage temperature	T <sub>sig</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V <sub>CC</sub>		3.0	3.3	3.6	V
High level input voltage	V <sub>IH</sub>		2.0		V <sub>CC</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3		+0.8	V
Operating ambient temperature	T <sub>A</sub>		0		70	°C

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	A0 - A12, BA0 (A13), /RAS, /CAS, /WE, CLK0-CLK3, CKE0, /CS0, /CS2, DQMB0 - DQMB7	TBD	TBD	TBD	pF
Data input/output capacitance	C <sub>I/O</sub>	DQ0 - DQ63	TBD	TBD	TBD	pF

★ DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

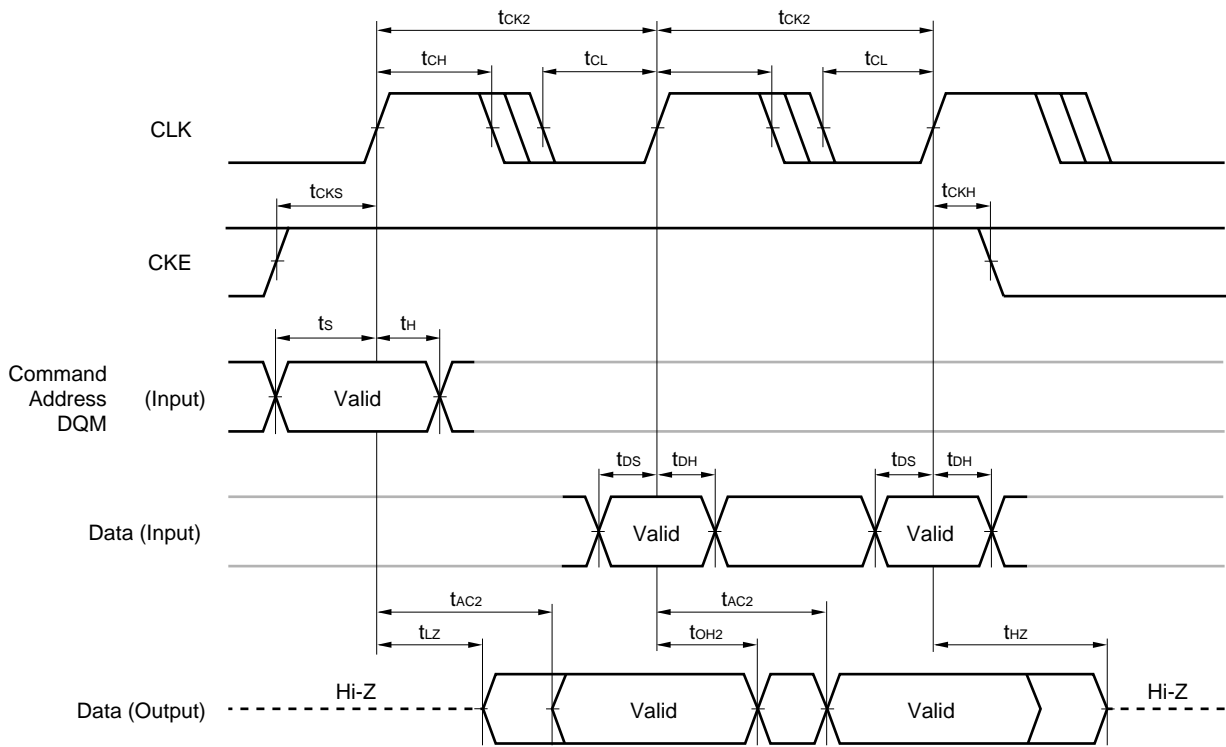
Parameter	Symbol	Test condition	Grade	MIN.	MAX.	Unit	Notes
Operating current (Prefetch mode at one bank active)	I <sub>CC1P</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub> Prefetch is executed one time during t <sub>RC</sub> .	-A75		680	mA	1
			-A10		640		
			-A15		560		
Operating current (Restore mode at one bank active)	I <sub>CC1R</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub>	-A75		680	mA	1
			-A10		640		
			-A15		560		
Precharge standby current in power down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns			8	mA	
	I <sub>CC2PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞			4		
Precharge standby current in non power down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.			200	mA	
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞, Input signals are stable.			64		
Active standby current in power down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = 15 ns			40	mA	
	I <sub>CC3PS</sub>	CKE ≤ V <sub>IL (MAX.)</sub> , t <sub>CK</sub> = ∞			32		
Active standby current in non power down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = 15 ns, /CS ≥ V <sub>IH (MIN.)</sub> , Input signals are changed one time during 30 ns.			200	mA	
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH (MIN.)</sub> , t <sub>CK</sub> = ∞. Input signals are stable.			80		
Operating current (Burst mode)	I <sub>CC4</sub>	t <sub>CK</sub> ≥ t <sub>CK (MIN.)</sub> , I <sub>O</sub> = 0 mA Background : precharge standby	-A75		520	mA	2
			-A10		400		
			-A15		320		
Auto Refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC (MIN.)</sub>	-A75		1,080	mA	3
			-A10		920		
			-A15		880		
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2 V	-A75		8	mA	
			-A10		8		
			-A15		8		
Input leakage current	I <sub>I (L)</sub>	V <sub>I</sub> = 0 to 3.6 V, All other pins not under test = 0 V		-8	+8	μA	
Output leakage current	I <sub>O (L)</sub>	D <sub>OUT</sub> is disabled, V <sub>O</sub> = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> = -4.0 mA		2.4		V	
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> = +4.0 mA			0.4	V	

- Notes**
- I<sub>CC1</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC1</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  - I<sub>CC4</sub> depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I<sub>CC4</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.
  - I<sub>CC5</sub> is measured on condition that addresses are changed only one time during t<sub>CK (MIN.)</sub>.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

Test Conditions

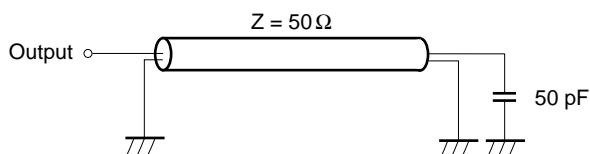
- AC measurements assume  $t_r = 1$  ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- If  $t_r$  is longer than 1 ns, reference level for measuring timing of input signals is  $V_{IH(MIN.)}$  and  $V_{IL(MAX.)}$ .
- An access time is measured at 1.4 V.



★ AC characteristics

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	t <sub>CK</sub>	7.5	–	10	–	15	–	ns	
Access time from CLK	t <sub>AC</sub>	–	5.4	–	6	–	12	ns	1
CLK high level width	t <sub>CH</sub>	2.5	–	3	–	3	–	ns	
CLK low level width	t <sub>CL</sub>	2.5	–	3	–	3	–	ns	
Data-out hold time	t <sub>OH</sub>	2.7	–	3	–	3	–	ns	1
Data-out low-impedance time	t <sub>LZ</sub>	0	–	0	–	0	–	ns	
Data-out high-impedance time	t <sub>HZ</sub>	2.5	5.5	3	6	3	6	ns	
Data-in setup time	t <sub>DS</sub>	1.5	–	2	–	2	–	ns	
Data-in hold time	t <sub>DH</sub>	0.8	–	1	–	1	–	ns	
Address, Command, DQM setup time	t <sub>S</sub>	1.5	–	2	–	2	–	ns	
Address, Command, DQM hold time	t <sub>H</sub>	0.8	–	1	–	1	–	ns	
CKE setup time	t <sub>CKS</sub>	1.5	–	2	–	2	–	ns	
CKE hold time	t <sub>CKH</sub>	0.8	–	1	–	1	–	ns	
CKE setup time (Power down exit)	t <sub>CKSP</sub>	1.5	–	2	–	2	–	ns	
Transition time	t <sub>T</sub>	0.8	30	1	30	1	30	ns	
Refresh time (4,096 refresh cycles)	t <sub>REF</sub>	–	64	–	64	–	64	ms	
Mode register set cycle time	t <sub>RSC</sub>	2	–	2	–	2	–	CLK	

★ Note 1. Output load.



★ AC characteristics (Background to Background operation)

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
<b>Same Bank Operation</b>									
ACT to ACT/REF Command period	t <sub>RC</sub>	67.5	–	80	–	90	–	ns	
REF to REF/ ACT Command period	t <sub>RCF</sub>	67.5	–	80	–	90	–	ns	
ACT to PRE Command period	t <sub>RAS</sub>	52	120,000	60	120,000	60	120,000	ns	
PRE to ACT / REF Command period	t <sub>RP</sub>	20	–	20	–	30	–	ns	
ACT to PFC/PFCA/PPF/PPFA Command delay time	t <sub>APD</sub>	15	–	20	–	30	–	ns	
ACT to PFR Command delay time (Prefetch Read Operation)	t <sub>APRD</sub>	20	–	20	–	TBD	–	ns	3
PFC to PRE Command delay time	t <sub>PPL</sub>	22.5	–	30	–	30	–	ns	
PFCA / PFR to ACT/REF Command delay time	t <sub>PAL</sub>	45	–	50	–	60	–	ns	
PPF to PRE Command delay time	t <sub>PPP</sub>	45	–	60	–	75	–	ns	
PPFA to ACT/REF Command delay time	t <sub>PPA</sub>	67.5	–	80	–	90	–	ns	
RST / RSTA to ACT(R) <sup>Note1</sup> Command delay time	t <sub>RAD</sub>	7.5	30	10	40	10	60	ns	2
<b>Same, Other Bank Operation</b>									
ACT(R) <sup>Note1</sup> to PFC/PFCA/PFR/PPF/PPFA Command delay time	t <sub>RPD</sub>	37.5	–	40	–	45	–	ns	
PFC to PFC / PFCA Command delay time	t <sub>PPD</sub>	22.5	–	30	–	30	–	ns	
PPF to PPF / PPFA Command delay time	t <sub>PPPD</sub>	45	–	60	–	75	–	ns	
<b>Other Bank Operation</b>									
ACT to ACT/ACT(R) or ACT(R) to ACT Command delay time	t <sub>RRD</sub>	15	–	20	–	30	–	ns	
ACT(R) to ACT(R) Command delay time	t <sub>RRDR</sub>	30	–	40	–	45	–	ns	
PFC /PFCA to RST /RSTA Command delay time	t <sub>PRD</sub>	22.5	–	30	–	30	–	ns	
PPF /PPFA to RST /RSTA Command delay time	t <sub>PPRD</sub>	45	–	60	–	75	–	ns	

- Notes**
1. ACT (R) command is ACT command after RST command.
  2. The another background operation and same channel foreground operation are illegal while t<sub>RAD</sub> period.
  3. When Read latency of SCLR (Set Channel Latency Register) is set up 1, this operation can not be used.

★ AC characteristics (Foreground to Foreground operation)

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
READ/WRITE to READ/WRITE Command delay time	t <sub>CCD</sub>	7.5	–	10	–	15	–	ns	

★ AC characteristics (Background to Foreground operation)  
(after same channel Prefetch/Restore)

Parameter	Symbol	-A75		-A10		-A15		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
PFC/PFCA/PPF/PPFA to READ/WRITE Command delay time	t <sub>PCD</sub>	15	–	20	–	30	–	ns	
PPF/PPFA to READ/WRITE Command delay time (2nd prefetch channel read write)	t <sub>PPCD</sub>	37.5	–	50	–	75	–	ns	
ACT(R) to READ/WRITE Command delay time	t <sub>RCD</sub>	30	–	40	–	45	–	ns	1

**Note 1.** ACT (R) command is ACT command after RST command.

★ Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	08H	0	0	0	0	1	0	0	0	VC SDRAM	
3	Number of row addresses	0DH	0	0	0	0	1	1	0	1	13 rows	
4	Number of column addresses	07H	0	0	0	0	0	1	1	1	7 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	40H	0	1	0	0	0	0	0	0	64 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface standard	01H	0	0	0	0	0	0	0	1	LVTTL	
9	Read latency (/CAS latency) = 2 cycle time	-A75	75H	0	1	1	1	0	1	0	1	7.5 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
		-A15	F0H	1	1	1	1	0	0	0	0	15 ns
10	Read latency (/CAS latency) = 2 access time	-A75	54H	0	1	0	1	0	1	0	0	5.4 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
		-A15	C0H	1	1	0	0	0	0	0	0	12 ns
11	DIMM configuration type	00H	0	0	0	0	0	0	0	0	None	
12	Refresh rate / type	80H	1	0	0	0	0	0	0	0	Normal	
13	VC SDRAM width	08H	0	0	0	0	1	0	0	0	×8	
14	Error checking SDRAM width	00H	0	0	0	0	0	0	0	0	None	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	1FH	0	0	0	1	1	1	1	1	1, 2, 4, 8, 16	
17	Number of banks on each VC SDRAM	02H	0	0	0	0	0	0	1	0	2 banks	
18	Read latency (/CAS latency) supported	03H	0	0	0	0	0	0	1	1	1, 2	
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	
21	VC SDRAM module attributes	00H	0	0	0	0	0	0	0	0		
22	VC SDRAM device attributes : general	0EH	0	0	0	0	1	1	1	0		
23	Read latency (/CAS latency) = 1 cycle time	-A75	00H	0	0	0	0	0	0	0	0	Not supported
		-A10	00H	0	0	0	0	0	0	0	0	Not supported
		-A15	F0H	1	1	1	1	0	0	0	0	15 ns
24	Read latency (/CAS latency) = 1 access time	-A75	00H	0	0	0	0	0	0	0	0	Not supported
		-A10	00H	0	0	0	0	0	0	0	0	Not supported
		-A15	C0H	1	1	0	0	0	0	0	0	12 ns
25-26		00H	0	0	0	0	0	0	0	0		
27	t <sub>RP</sub> (MIN.)	-A75	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns

(2/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
28	t <sub>RRD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
29	t <sub>APD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
30	t <sub>RAS</sub> (MIN.)	-A75	34H	0	0	1	1	0	1	0	0	52 ns
		-A10	3CH	0	0	1	1	1	1	0	0	60 ns
		-A15	3CH	0	0	1	1	1	1	0	0	60 ns
31	Module bank density	10H	0	0	0	1	0	0	0	0	64M bytes	
32	Address and command signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
33	Address and command signal input hold time	10H	0	0	0	1	0	0	0	0	1 ns	
34	Data signal input setup time	20H	0	0	1	0	0	0	0	0	2 ns	
35	Data signal hold setup time	10H	0	0	0	1	0	0	0	0	1 ns	
36	Prefetch read latency	-A75	04H	0	0	0	0	0	1	0	0	4 clocks
		-A10	04H	0	0	0	0	0	1	0	0	4 clocks
		-A15	00H	0	0	0	0	0	0	0	0	Not supported
37	t <sub>PCD</sub> (MIN.)	-A75	0FH	0	0	0	0	1	1	1	1	15 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A15	1EH	0	0	0	1	1	1	1	0	30 ns
38	Number of segment addresses	02H	0	0	0	0	0	0	1	0	2 bits	
39	Number of channels	04H	0	0	0	0	0	1	0	0	16	
40	Depth of channels	07H	0	0	0	0	0	1	1	1	128 bits	
41-61												
62	SPD revision	02H	0	0	0	0	0	0	1	0	2.0	
63	Checksum for bytes 0 - 62	-A75	64H	0	1	1	0	0	1	0	0	
		-A10	B2H	1	0	1	1	0	0	1	0	
		-A15	36H	0	0	1	1	0	1	1	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											

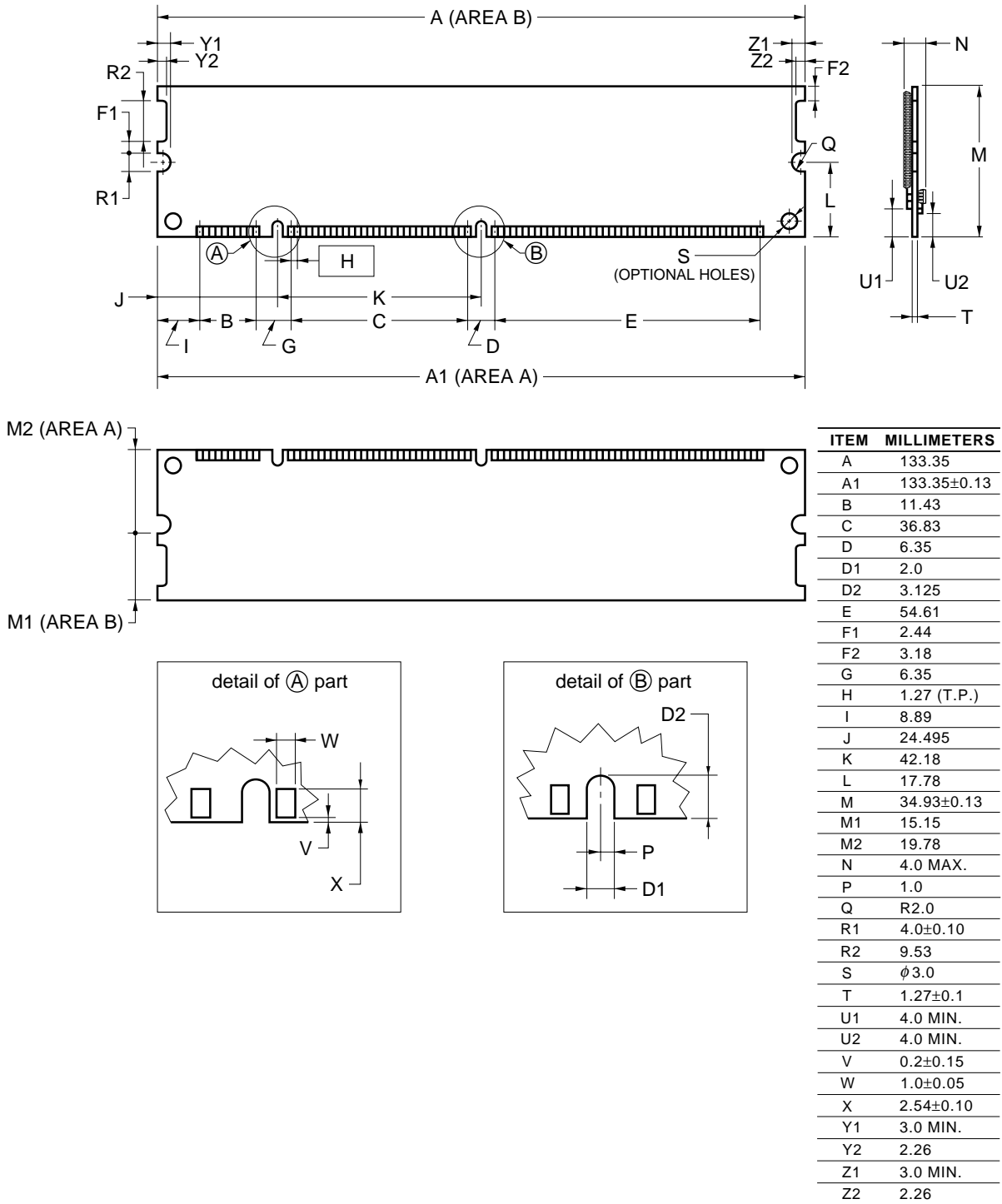
**Timing Charts**

Please refer to the **μPD4565421, 4565821, 4565161 Data sheet (M13022E)**.

Package Drawing

[ MC-45V8AB641KF ]

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



★ Revision History

Edition / Date	Page		Description	
	This edition	Previous edition	Type of edition	Location
4th edition / June 1999	p.1	p.1	Deletion	-A70
	p.2	p.2		
	p.6	p.6		
	p.8	p.8		
			Modification	Note1
	p.9	p.9	Deletion	-A70 , t <sub>RCPD</sub> , t <sub>DAL</sub>
			Modification	t <sub>APD</sub> (Parameter) , t <sub>RPD</sub> (Parameter)
	p.10	p.10	Deletion	-A70
			Modification	t <sub>PCD</sub> (Parameter)
	p.11	p.11	Deletion	-A70
p.12	p.12			
p.14	p.14	Addition	Revision History	

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

### CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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