HM5112805TD-5,
HM5113805TD-5

128M EDO DRAM (16-Mword × 8-bit)
8k refresh/4k refresh

HITACHI

ADE-203-936A (Z)
Rev. 1.0
June 22, 1998

Description

The Hitachi HM5112805 Series, HM5113805 Series are 128M-bit dynamic RAMs organized as 16,777,216-word × 8-bit. They have realized high performance and low power by employing CMOS process technology. HM5112805 Series, HM5113805 Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They are packaged in 32-pin plastic TSOPII.

Features

- Single 3.3 V supply: 3.3 V ± 0.15 V
- Access time: 50 ns (max)
- Power dissipation
  - Active: 759 mW (max) (HM5112805 Series)
    897 mW (max) (HM5113805 Series)
  - Standby : 3.5 mW (max) (CMOS interface)
- EDO page mode capability
- Refresh cycles
  - $\overline{\text{RAS}}$-only refresh
    8192 cycles/64 ms (HM5112805)
    4096 cycles/64 ms (HM5113805)
  - CBR/Hidden refresh
    4096 cycles/64 ms (HM5112805, HM5113805)

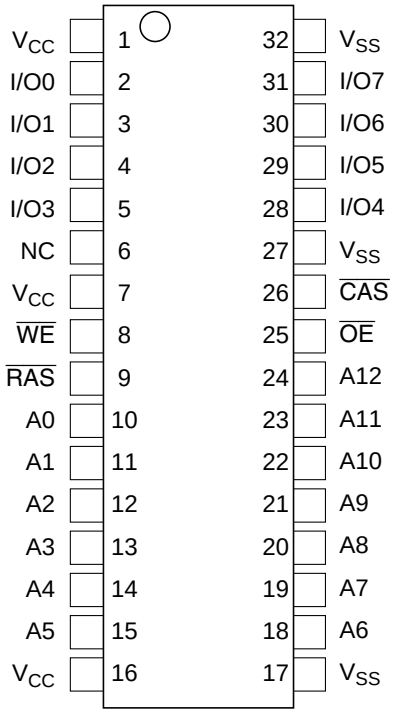
- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh

Ordering Information

Type No.	Access time	Package
HM5112805TD-5	50 ns	400-mil 32-pin plastic TSOP II (TTP-32DF)
HM5113805TD-5	50 ns	

Pin Arrangement (HM5112805 Series)

32-pin TSOP



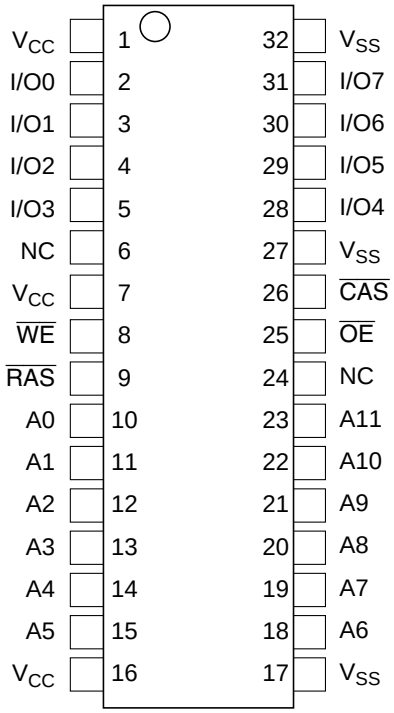
(Top view)

Pin Description

Pin name	Function
A0 to A12	Address input • Row/Refresh address A0 to A12 • Column address A0 to A10
I/O0 to I/O7	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Pin Arrangement (HM5113805 Series)

32-pin TSOP

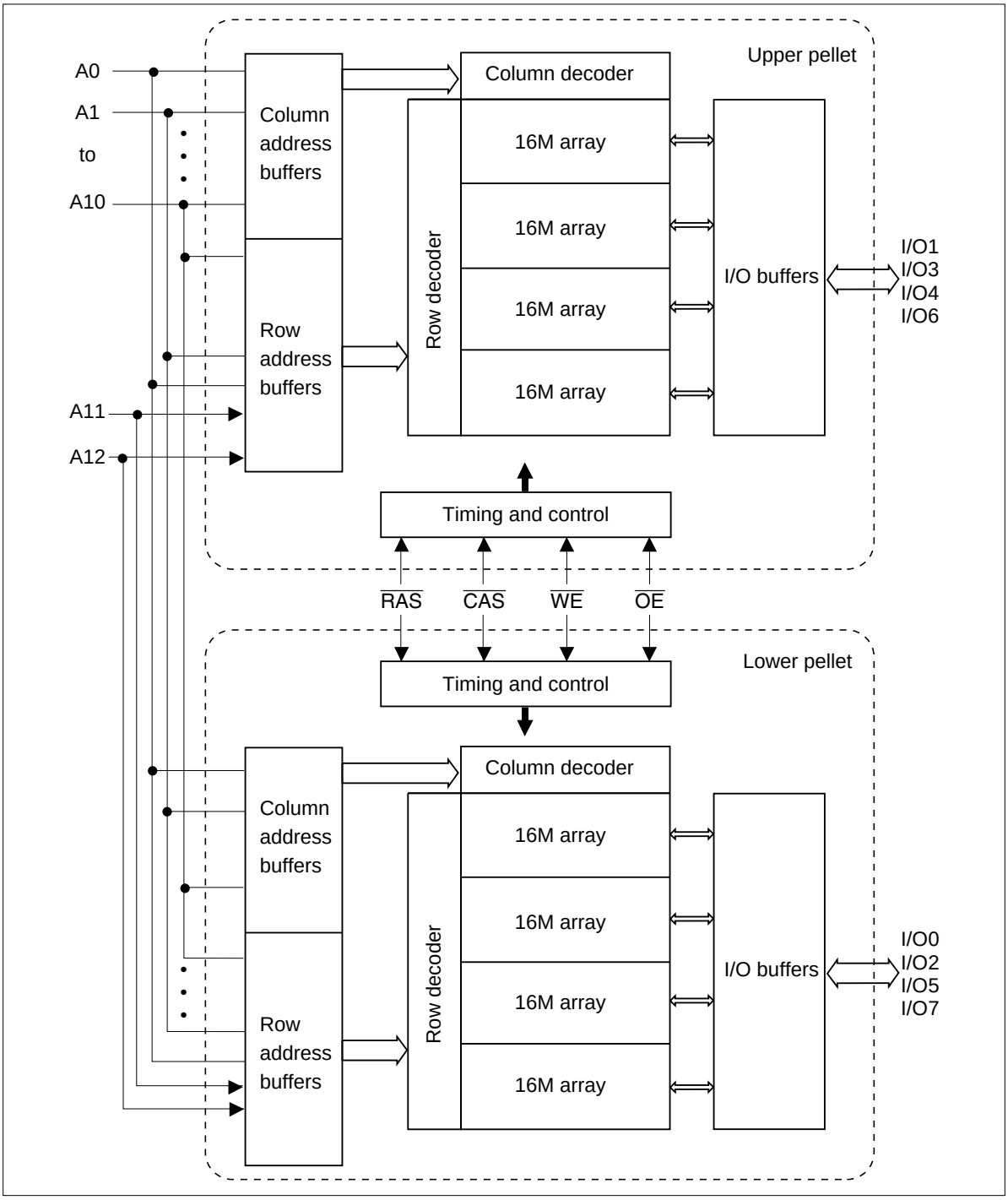


(Top view)

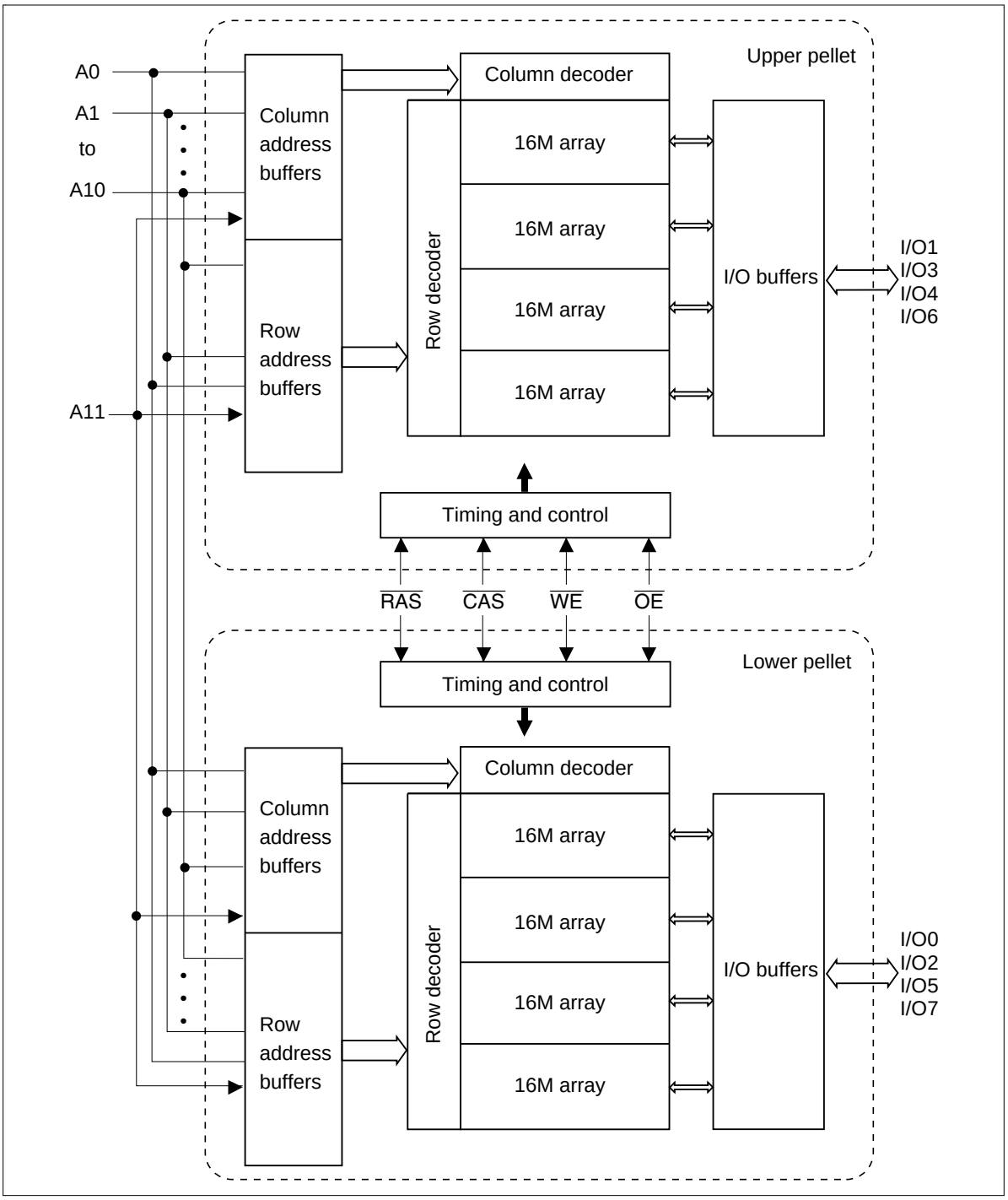
Pin Description

Pin name	Function
A0 to A11	Address input • Row/Refresh address A0 to A11 • Column address A0 to A11
I/O0 to I/O7	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram (HM5112805 Series)



Block Diagram (HM5113805 Series)



Operation Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	I/O 0 to I/O 7	Operation
H	×	×	×	High-Z	Standby
L	L	H	L	Dout	Read cycle
L	L	L*[2]	×	Din	Early write cycle
L	L	L*[2]	H	Din	Delayed write cycle
L	L	H to L	L to H	Dout/Din	Read-modify-write cycle
L	H	×	×	High-Z	$\overline{RAS}$-only refresh cycle
H to L	L	H	×	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle
L	L	H	H	High-Z	Read cycle (Output disabled)

Notes: 1. H: V_{IH} (inactive), L: V_{IL} (active), ×: V_{IH} or V_{IL}
2. $t_{WCS} \geq 0$ ns: Early write cycle
$t_{WCS} < 0$ ns: Delayed write cycle

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 V (max))	V
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Storage temperature	Tstg	–55 to +125	°C

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.15	3.3	3.45	V	1, 2
	V_{SS}	0	0	0	V	2
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	0	—	70	°C	

Notes: 1. All voltage referred to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (HM5112805 Series)

		HM5112805			
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Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	220	mA	t_{RC} = min
Standby current	I_{CC2}	—	4	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	220	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	10	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	220	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	220	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Input leakage current	I_{LI}	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Measured with one sequential address change per EDO cycle, t_{HPC}.

DC Characteristics (HM5113805 Series)

		HM5113805 -5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Operating current*1, *2	I_{CC1}	—	260	mA	t_{RC} = min
Standby current	I_{CC2}	—	4	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*2	I_{CC3}	—	260	mA	t_{RC} = min
Standby current*1	I_{CC5}	—	10	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	260	mA	t_{RC} = min
EDO page mode current*1, *3	I_{CC7}	—	220	mA	$\overline{RAS}$ = V_{IL} , $\overline{CAS}$ cycle, t_{HPC} = t_{HPC} min
Input leakage current	I_{LI}	–5	5	µA	0 V ≤ Vin ≤ V_{CC} + 0.3 V
Output leakage current	I_{LO}	–5	5	µA	0 V ≤ Vout ≤ V_{CC} Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Measured with one sequential address change per EDO cycle, t_{HPC}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.15 V)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	7	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	8	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$ and $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.15 V, V_{SS} = 0 V) *1, *2, *19

Test Conditions

- Input rise and fall time: 2 ns
- Input pulse levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5112805/HM5113805			
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Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10000	ns	
Row address setup time	t_{ASR}	0	—	ns	
Row address hold time	t_{RAH}	8	—	ns	
Column address setup time	t_{ASC}	0	—	ns	
Column address hold time	t_{CAH}	8	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	ns	7

Read Cycle

		HM5112805/HM5113805			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	50	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	13	ns	9, 10, 17
Access time from address	t_{AA}	—	25	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	13	ns	9
Read command setup time	t_{RCS}	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	50	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	15	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	ns	
Output data hold time	t_{OH}	3	—	ns	21
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	ns	13, 21
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	13	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	13	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	ns	21
Output buffer turn-off to $\overline{RAS}$	t_{OFR}	—	13	ns	13, 21
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	13	ns	13
$\overline{WE}$ to Din delay time	t_{WED}	13	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	13	—	ns	

Write Cycle

		HM5112805/HM5113805			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	ns	14
Write command hold time	t_{WCH}	8	—	ns	
Write command pulse width	t_{WP}	8	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	ns	
Data-in setup time	t_{DS}	0	—	ns	15
Data-in hold time	t_{DH}	8	—	ns	15

Read-Modify-Write Cycle

		HM5112805/HM5113805			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	116	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	ns	

Refresh Cycle

		HM5112805/HM5113805			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	ns	

EDO Page Mode Cycle

		HM5112805/HM5113805			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	20	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	28	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	28	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	ns	9, 22
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	8	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	28	—	ns	
Write pulse width during $\overline{CAS}$ precharge	t_{WPE}	8	—	ns	
$\overline{OE}$ precharge time	t_{OEP}	8	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM5112805/HM5113805			
		-5			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPRWC}	57	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	ns	14

Refresh(HM5112805 Series)

Parameter	**Symbol**	**Max**	**Unit**	**Notes**
Refresh period	t_{REF}	64	ms	8192 cycles

Refresh(HM5113805 Series)

Parameter	**Symbol**	**Max**	**Unit**	**Notes**
Refresh period	t_{REF}	64	ms	4096 cycles

Notes: 1. AC measurements assume t_T = 2 ns.

2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).

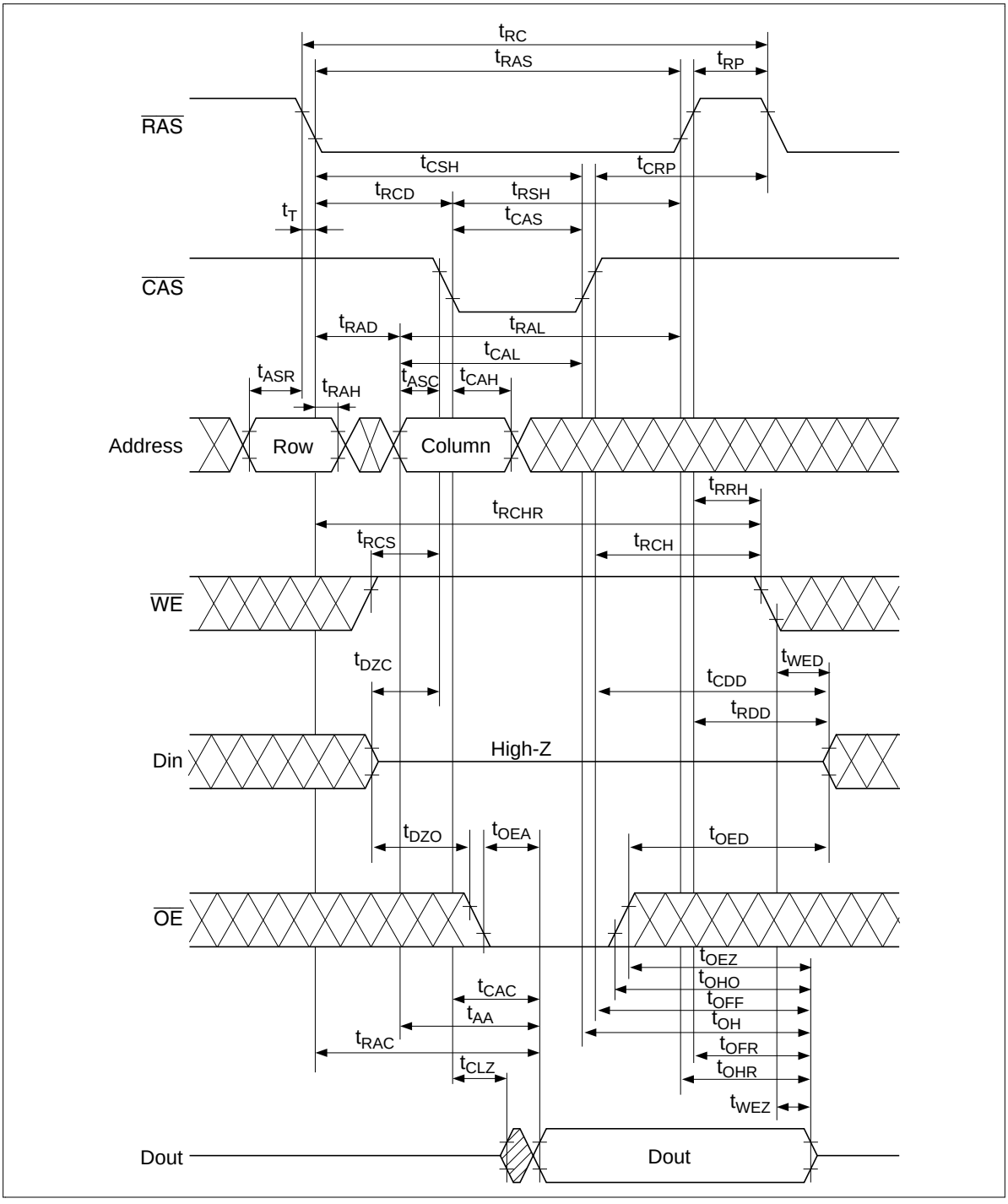
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, than the access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. t_{DS} and t_{DH} are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}.
22. t_{DOH} defines the time at which the output level go cross. V_{OL} = 0.8 V, V_{OH} = 2.0 V of output timing reference level.
23. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))

    ///////: Invalid Dout

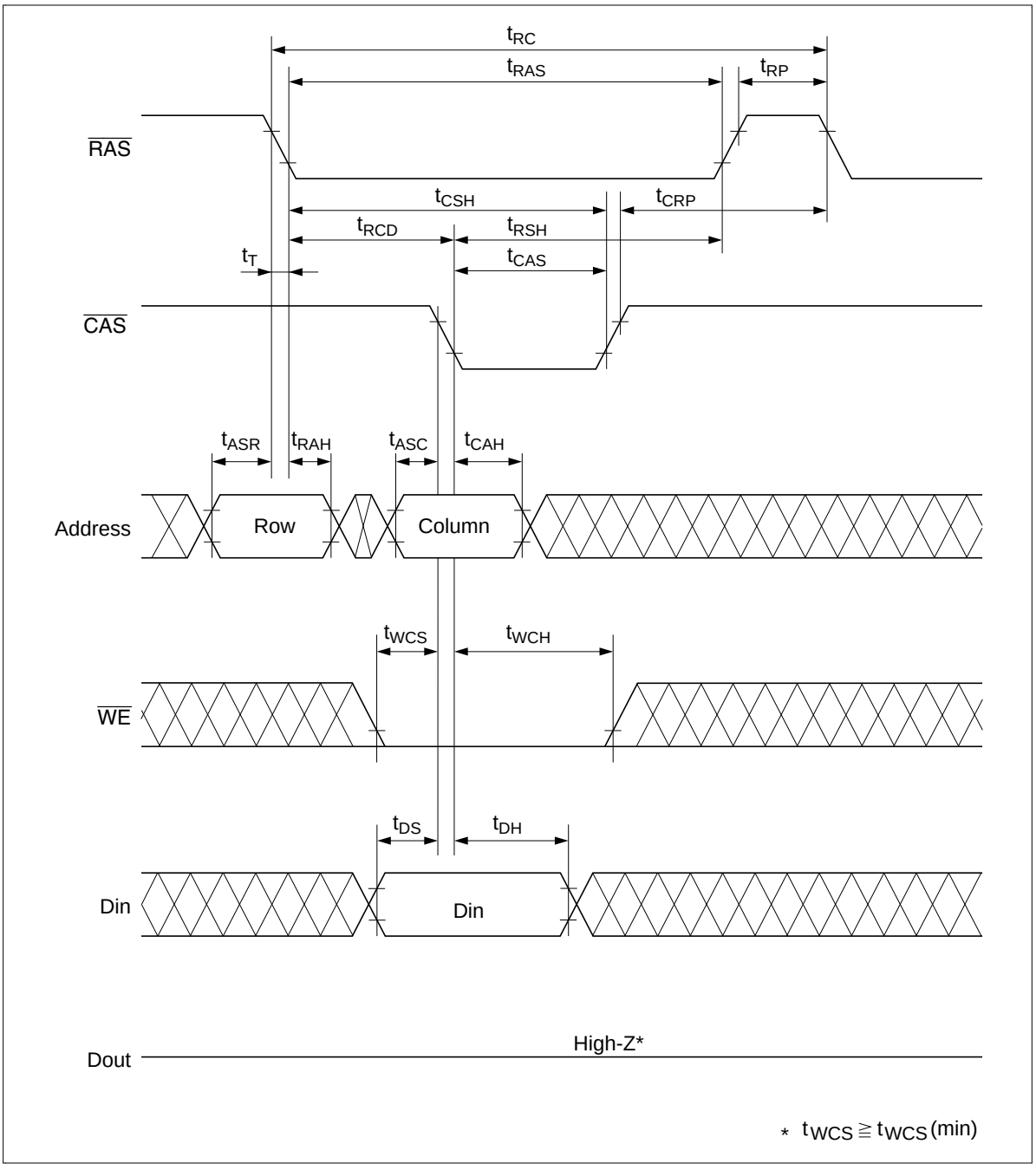
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms*[23]

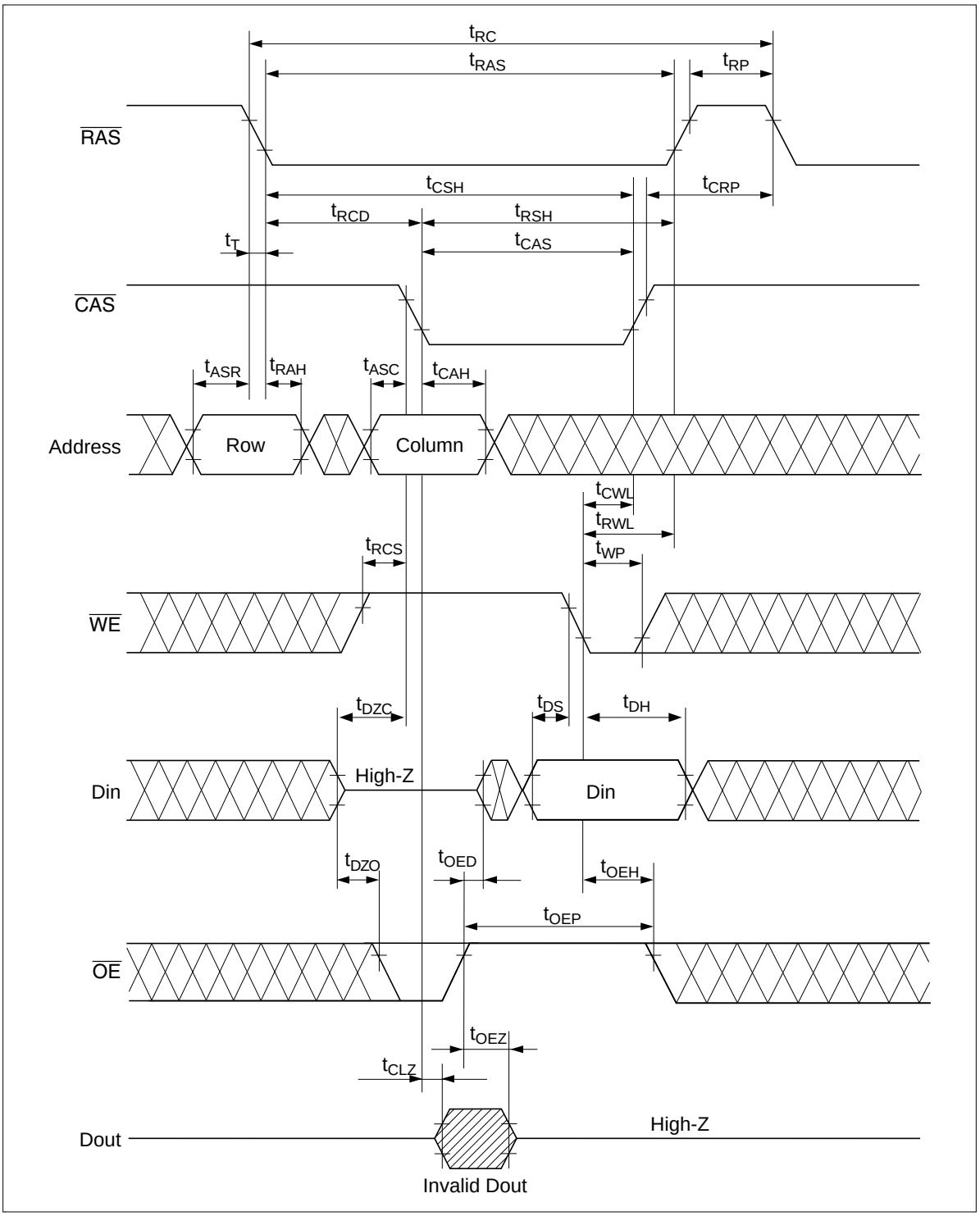
Read Cycle



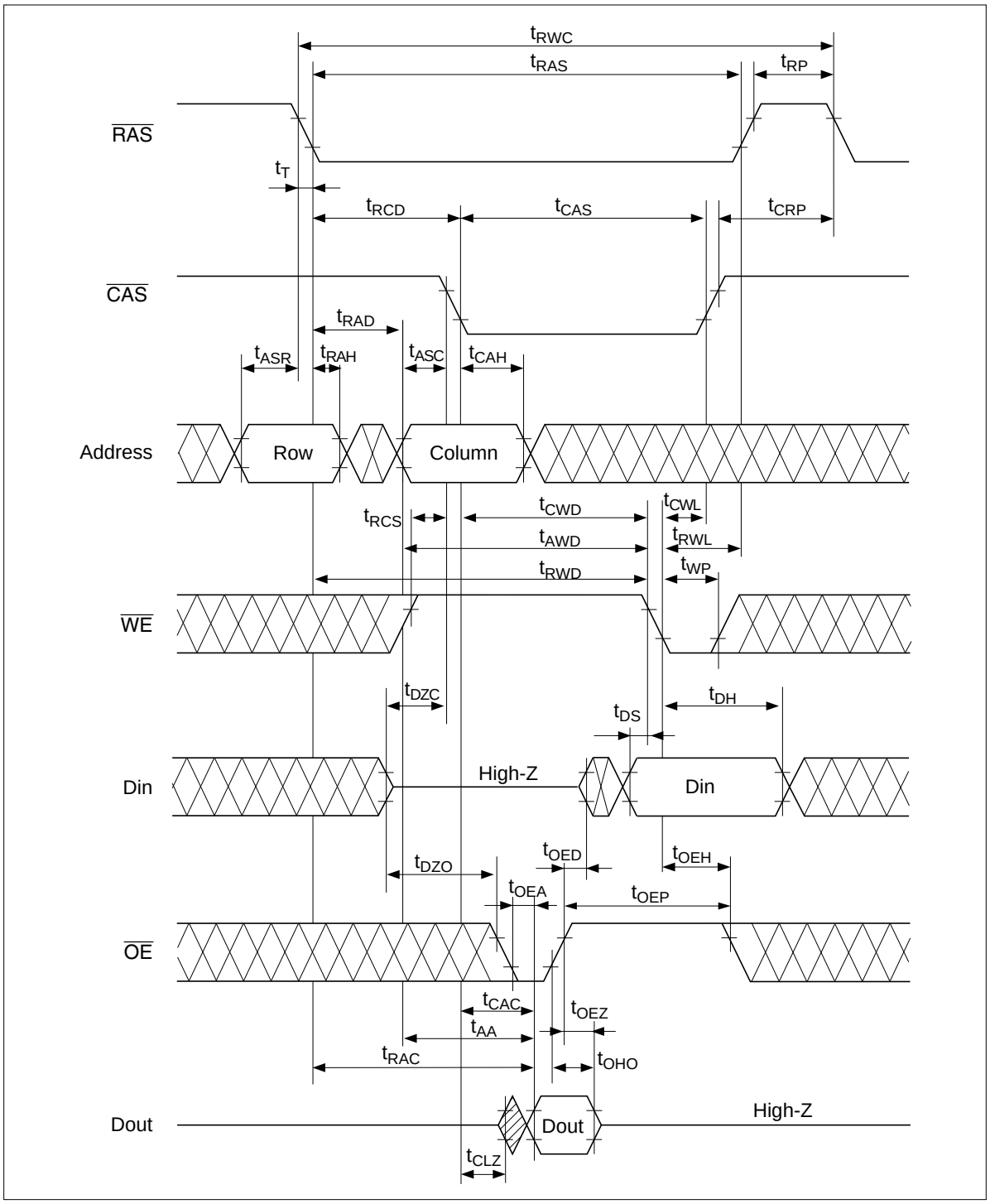
Early Write Cycle



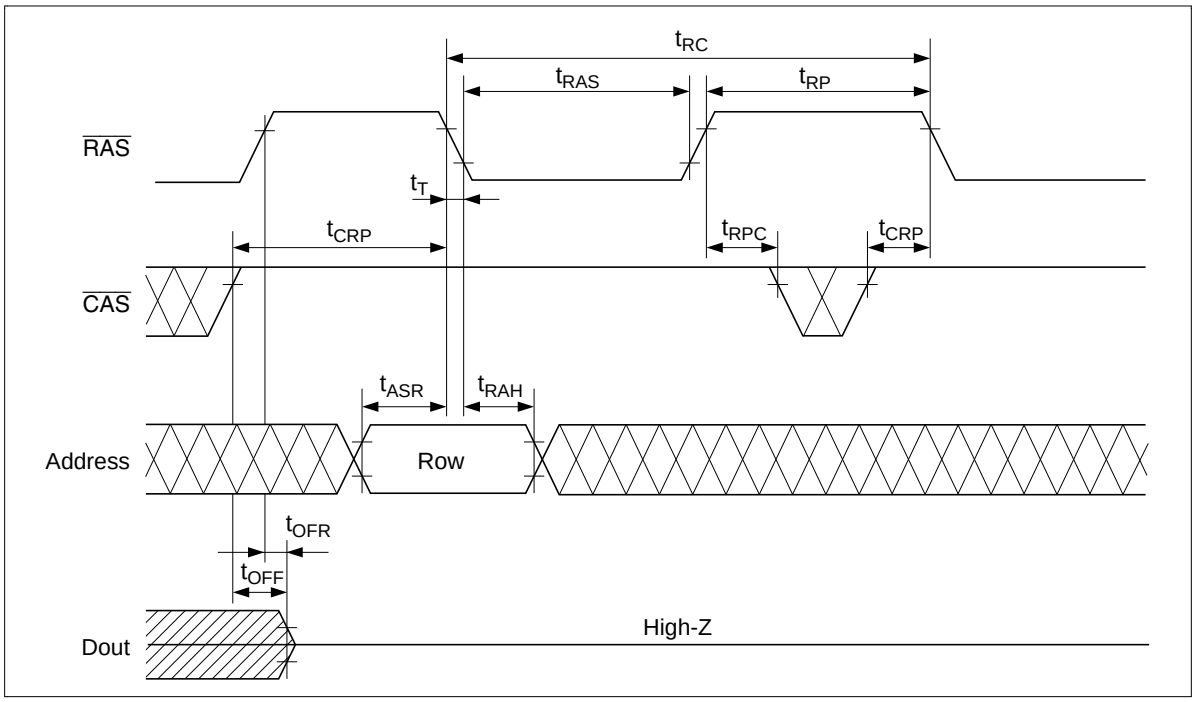
Delayed Write Cycle*[18]



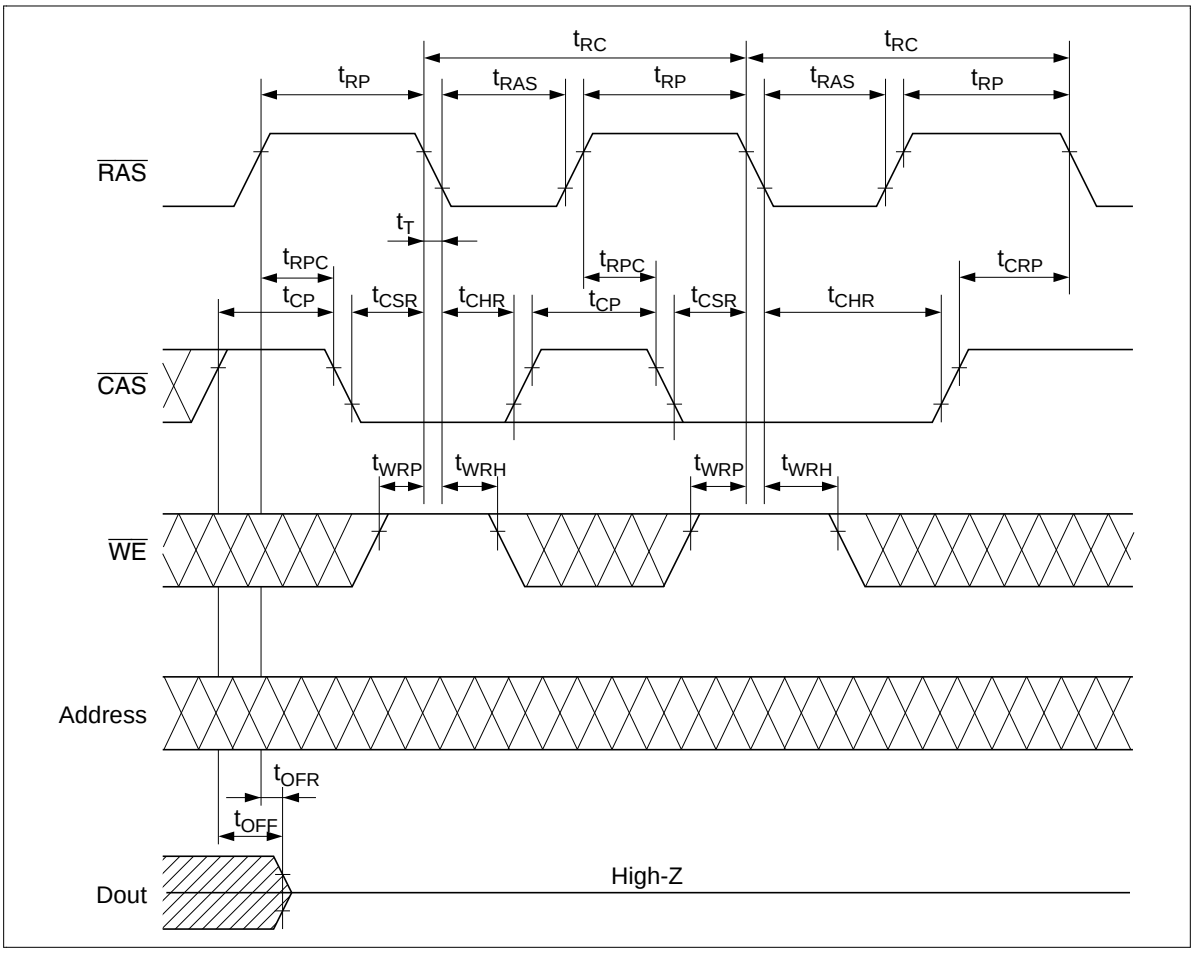
Read-Modify-Write Cycle*[18]



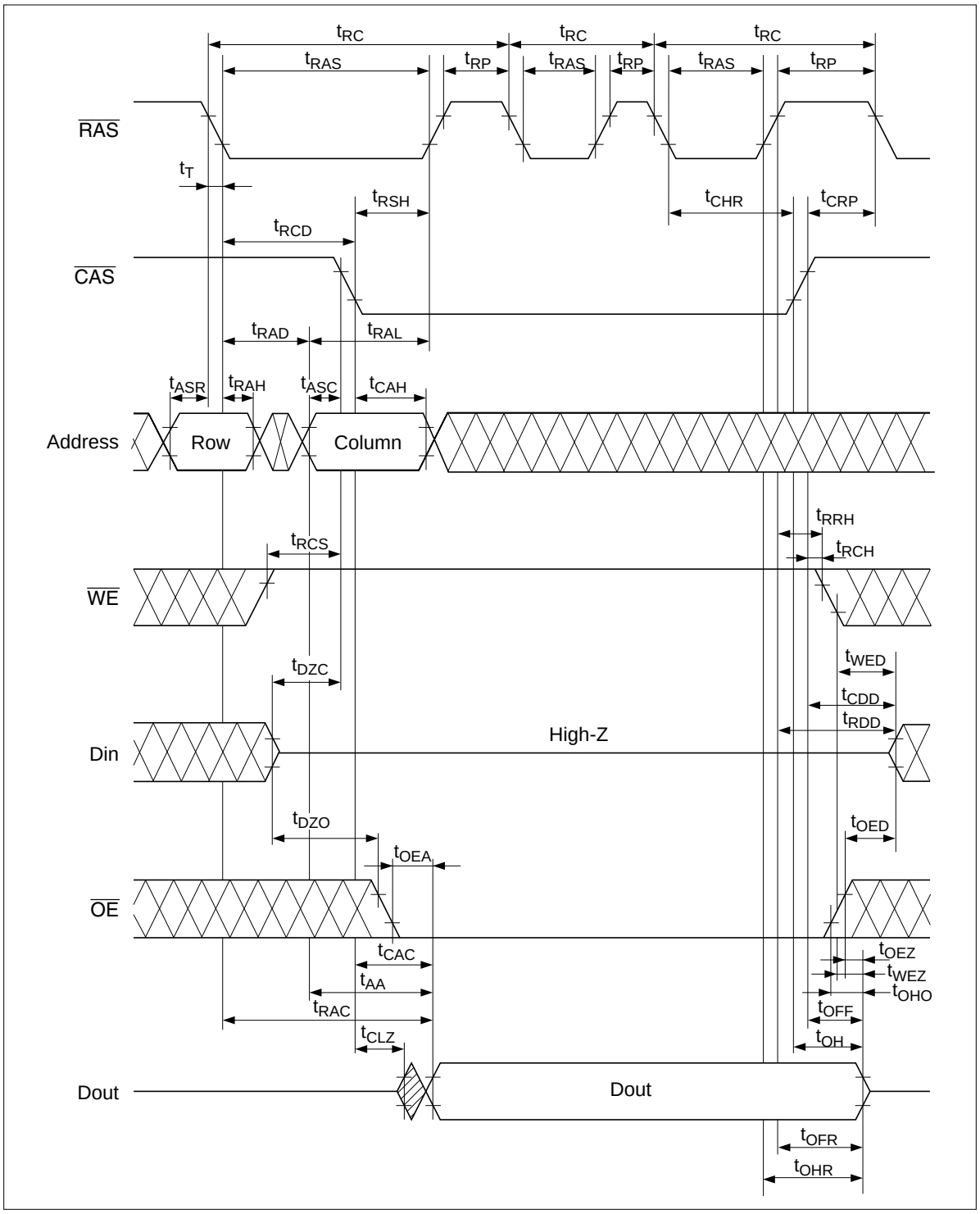
$\overline{\text{RAS}}$-Only Refresh Cycle



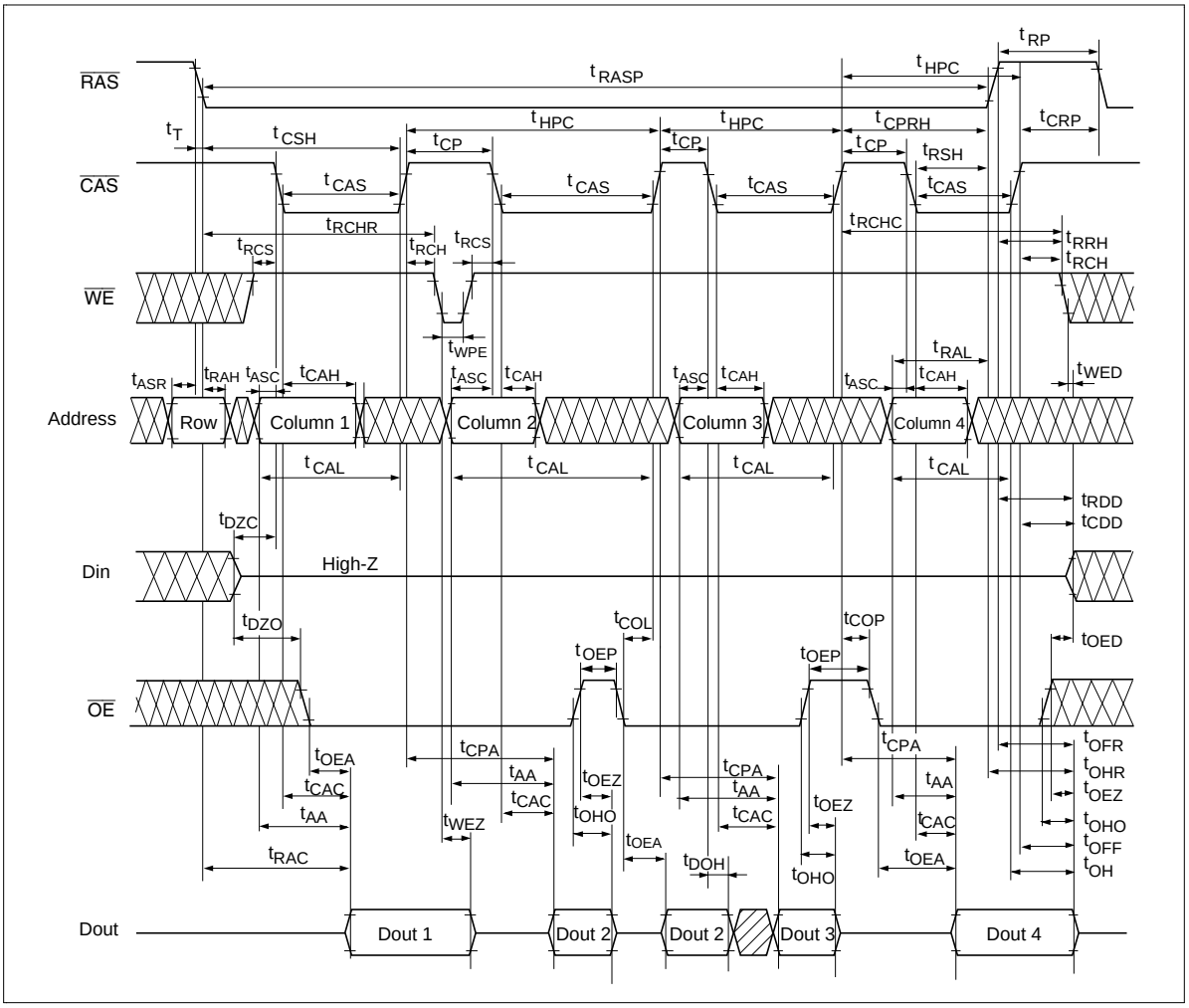
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



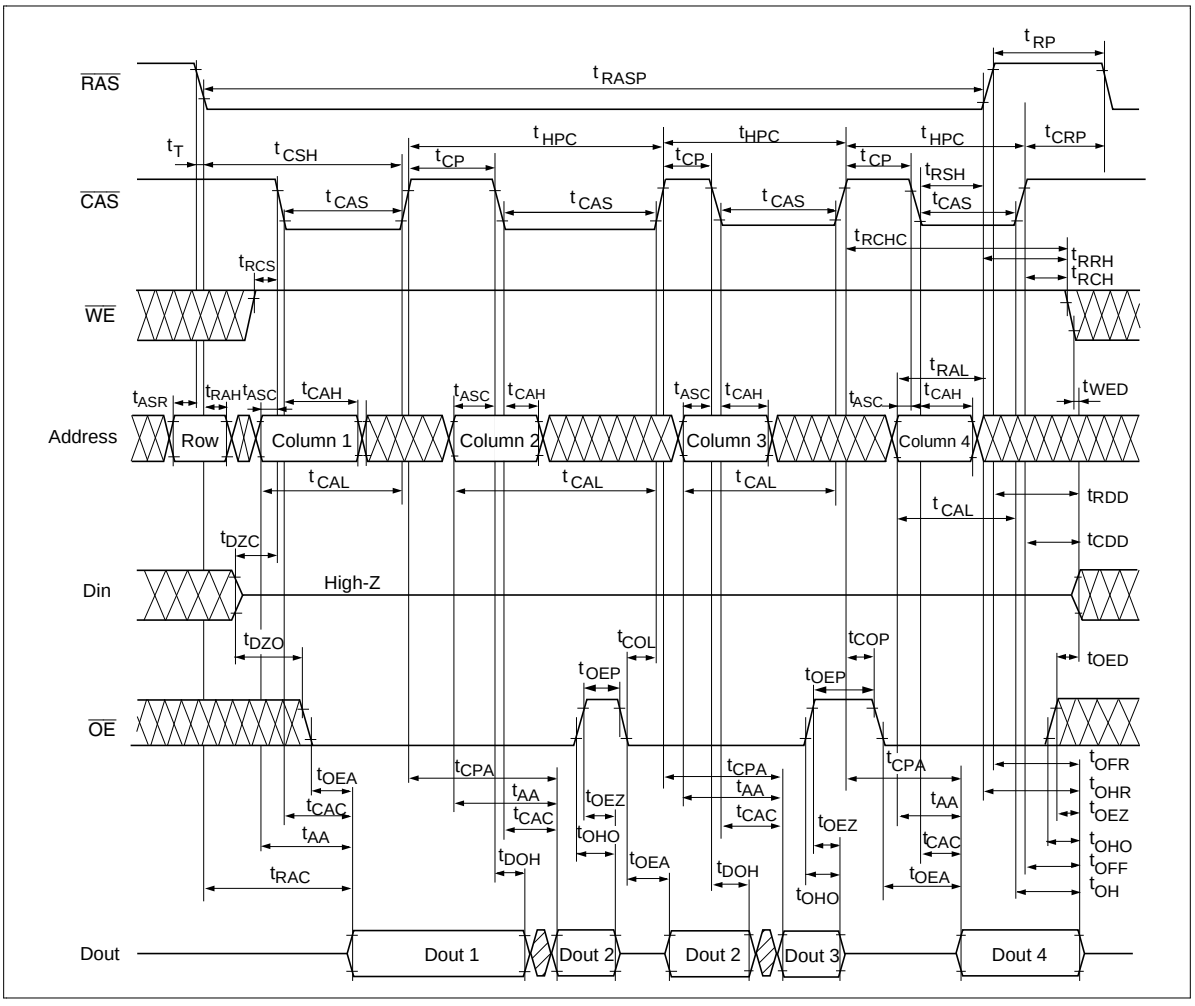
Hidden Refresh Cycle



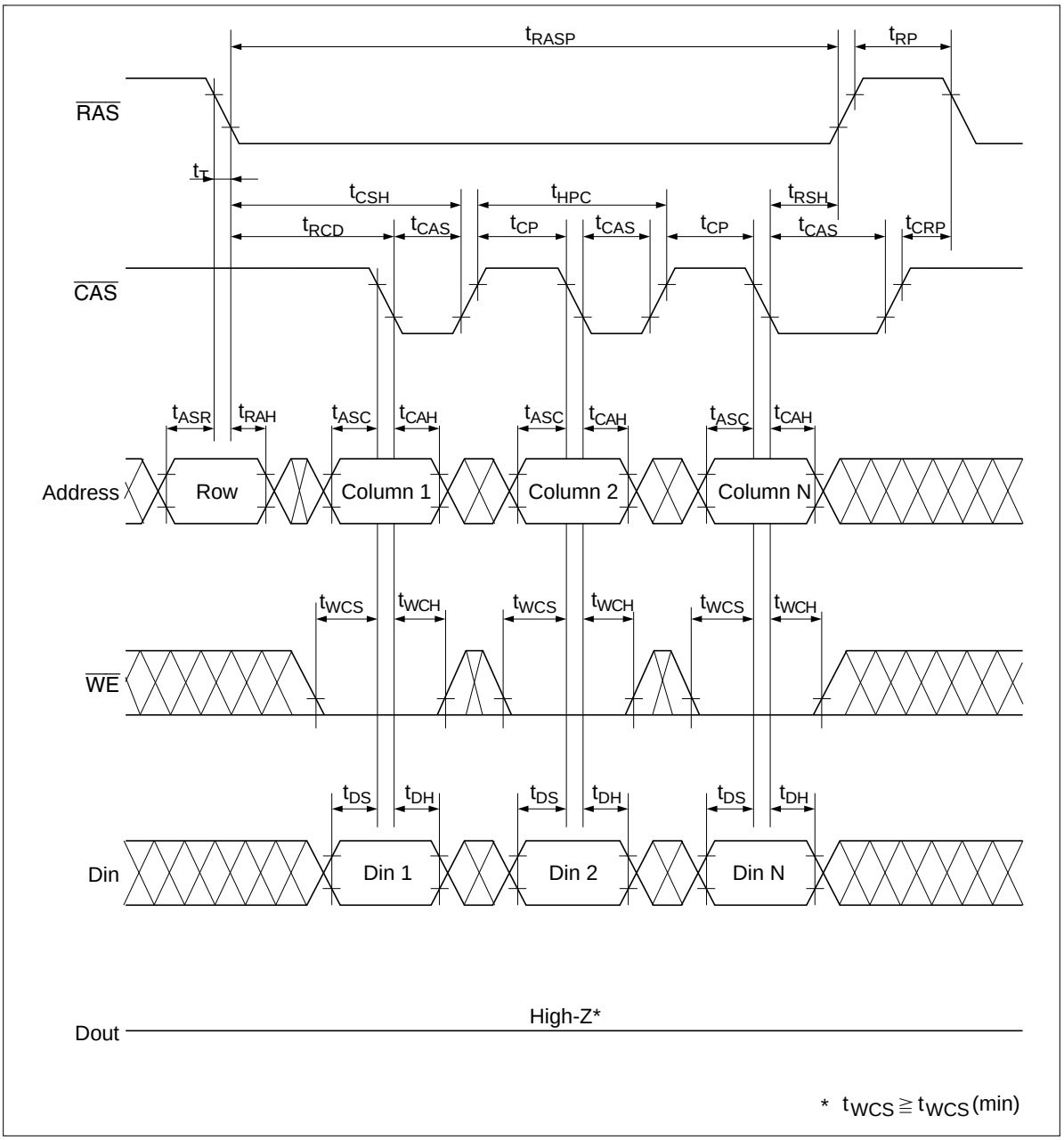
EDO Page Mode Read Cycle (1)



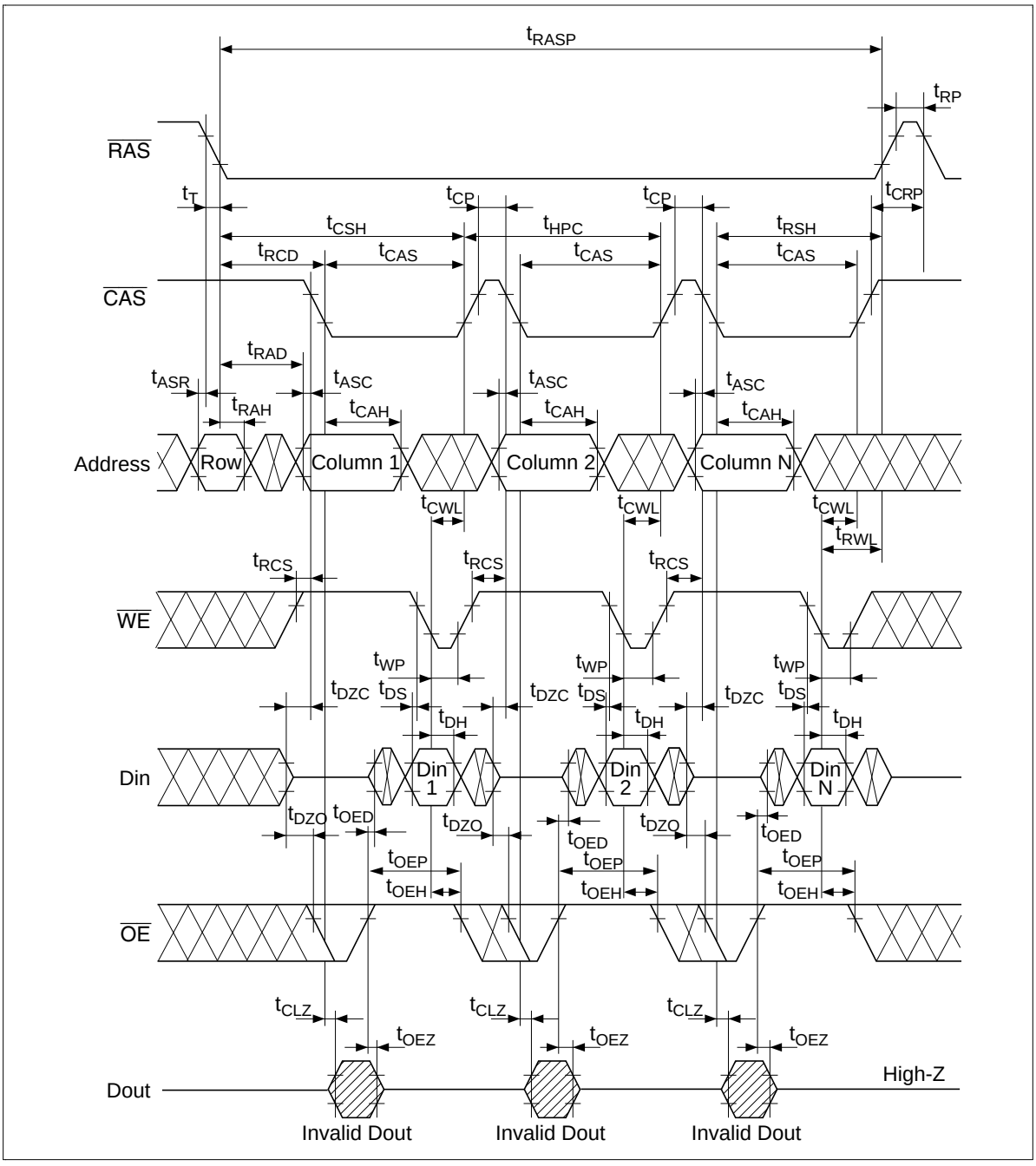
EDO Page Mode Read Cycle (2)



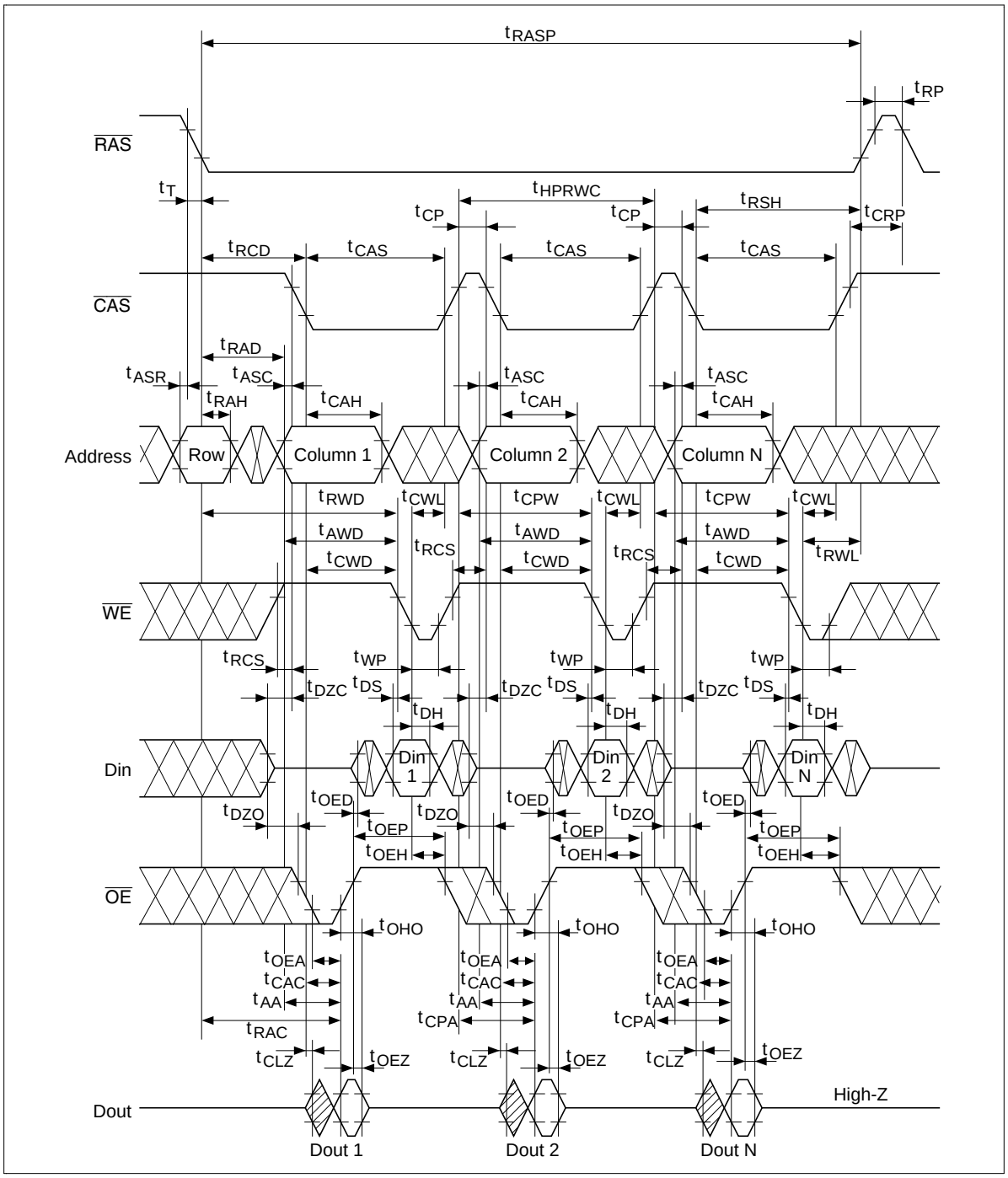
EDO Page Mode Early Write Cycle



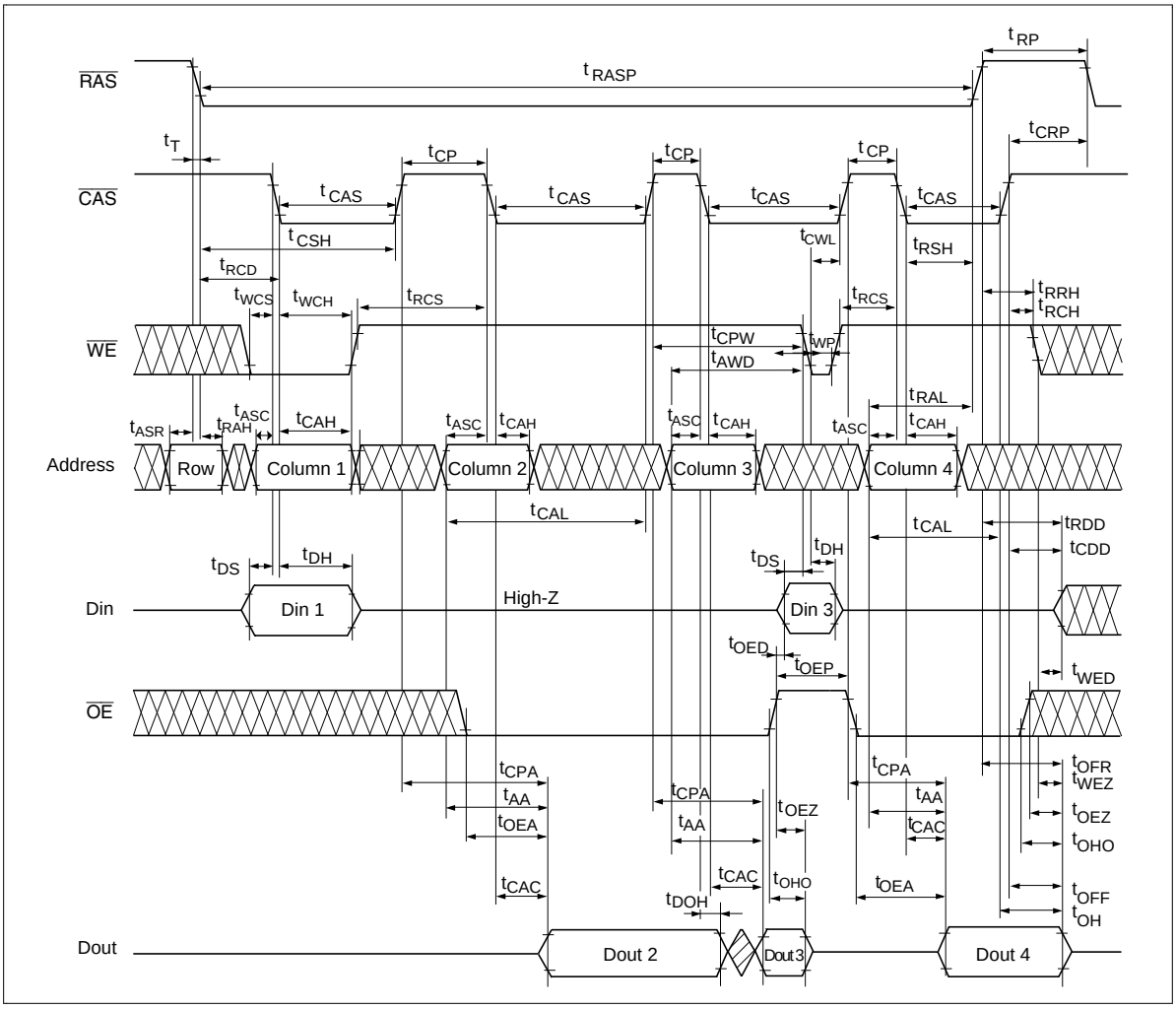
EDO Page Mode Delayed Write Cycle*[18]



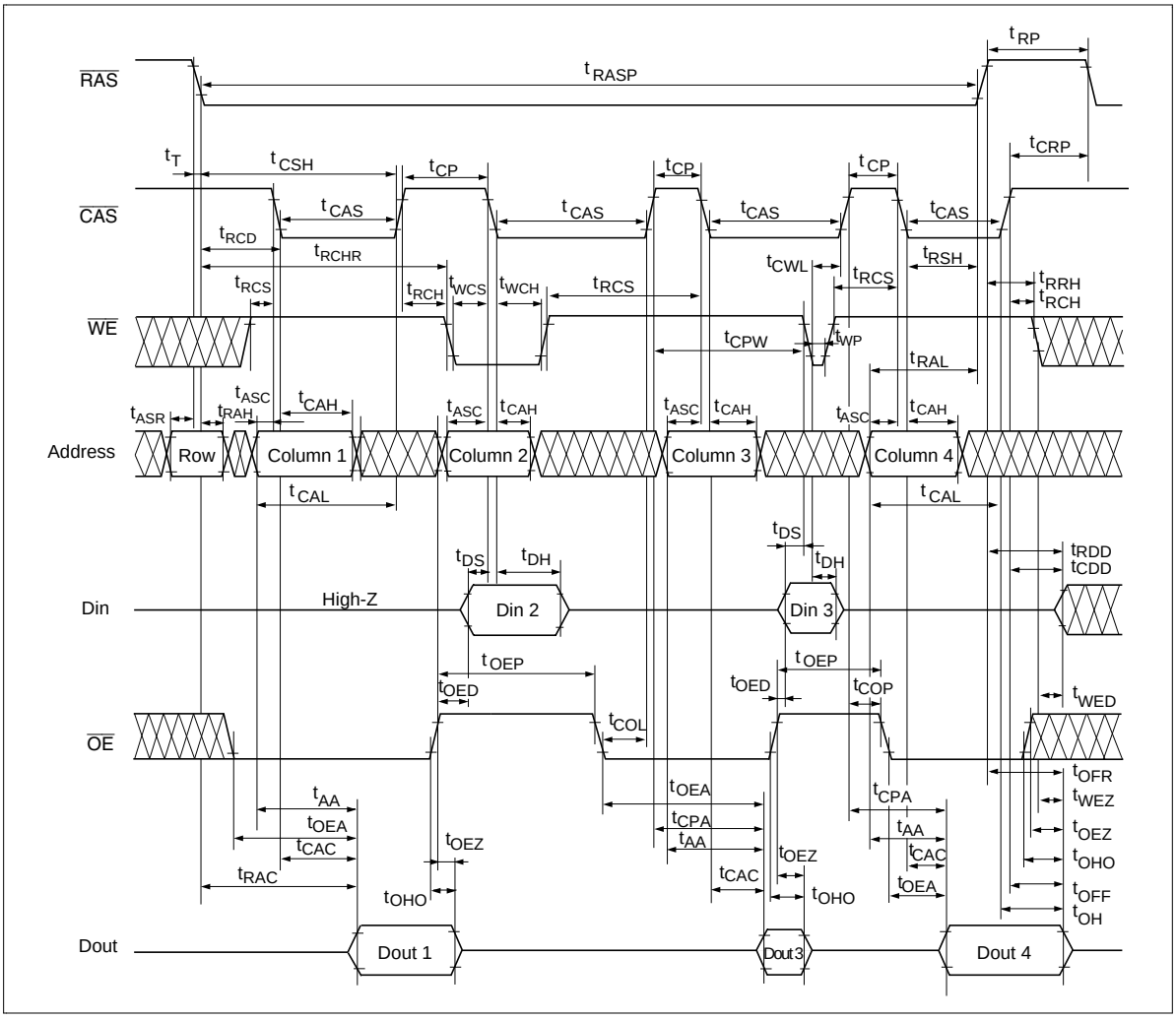
EDO Page Mode Read-Modify-Write Cycle*[18]



EDO Page Mode Mix Cycle (1)*[20]



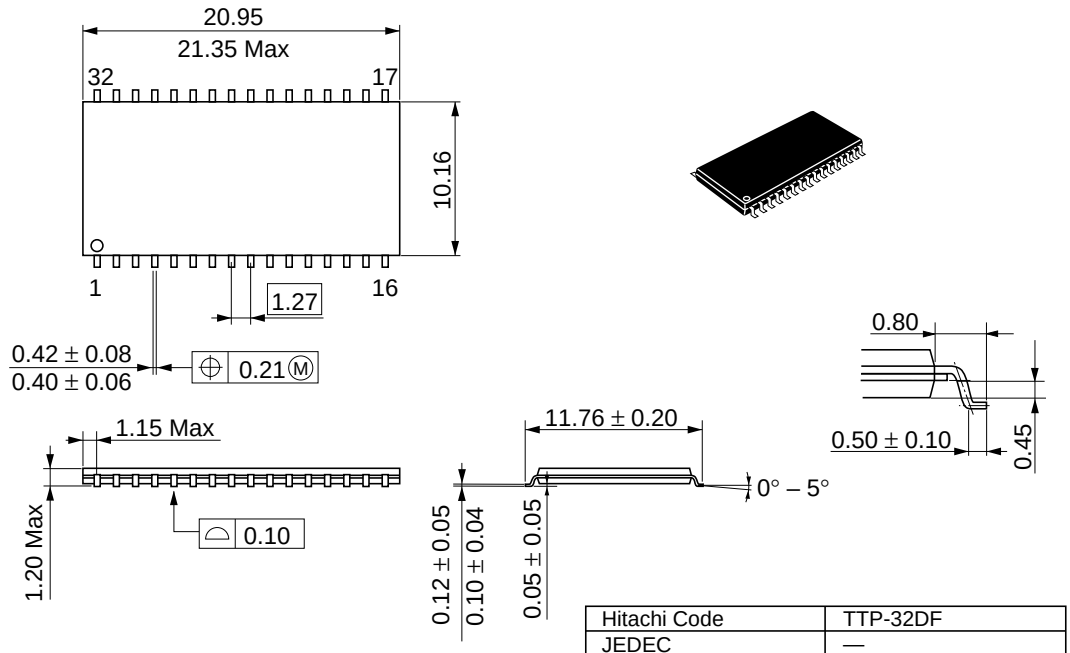
EDO Page Mode Mix Cycle (2) *[20]



Package Dimensions

HM5112805TD Series
HM5113805TD Series (TTP-32DF)

Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32DF
JEDEC	—
EIAJ	—
Weight (reference value)	0.54 g

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Jun. 22, 1998	Initial issue		