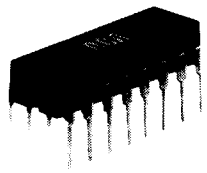
CA3159E



16-Lead Dual-In-Line
Plastic Package
"E" Suffix H-1622

Horizontal Processor and AGC Detector

FEATURES:

- *AGC voltage*
- *Separated sync*
- *31.5 kHz oscillator*
- *Gates AGC and sync for noise immunity*

The CA3159E is a monolithic integrated circuit designed for use as a horizontal processor and AGC detector in color or black-and-white TV receivers. It performs the functions of AGC, sync separation, and noise immunity, and a 31.5 kHz oscillator is provided for use with vertical-countdown circuits.

The CA3159E is supplied in a 16-lead dual-in-line plastic package.

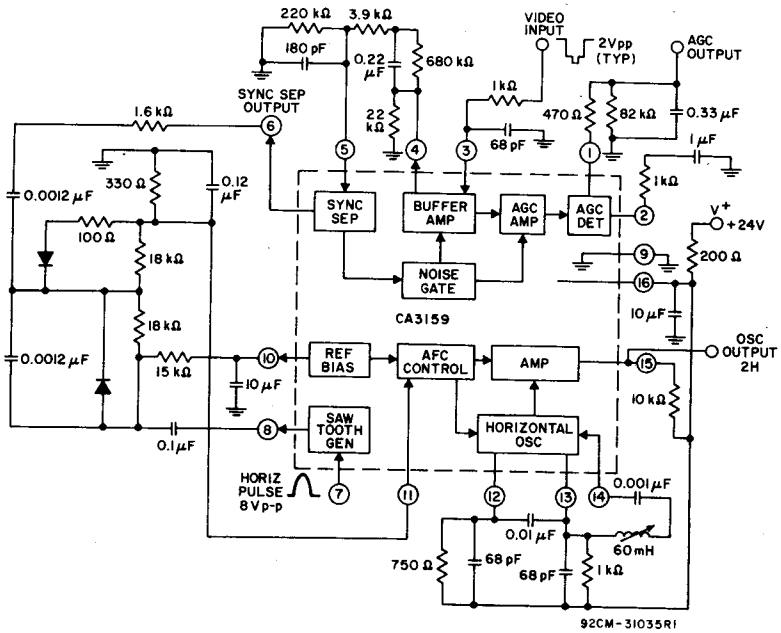


Fig. 1 — Functional block diagram of CA3159E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE . . . . . +30 V
DC SUPPLY CURRENT . . . . . 30 mA
DEVICE DISSIPATION:
Up to T_A = 55°C . . . . . 750 mW
Above T_A = 55°C . . . . . Derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . . −40 to +85°C
Storage . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10s max. . . . . +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 28 V, all switches open unless otherwise specified. (See Fig. 2)

CHARACTERISTIC	TEST CONDITIONS	TERM. MEAS.	TYPICAL VALUES	UNITS
AGC Voltage	S1, S9 closed	1	1.85	V
Noise Inverter[1]	S2, S9 closed	1	0.7	V
Shift Threshold[1]	S2, S3 closed	1	20	V
Sync Level	S1, S9 closed	4	18	V
Positive Pulse[2]	S5 closed	7	25	V
Positive Sawtooth[3]	S5, S6 closed	8	3	V
Sync Low	S3, S4 closed	6	1.5	V
Supply Current		16	20	mA
Free-Running Freq.[4]	S7,S8,S9 closed	15	31.5	kHz
Duty Cycle	S7,S8,S9 closed	15	48	%

1. A = 3 V, B = 1.2 V, − 1 mA to term. I
2. C = 0.2 mA
3. C = 0.2 mA, D = 5 mA
4. Adjust LI, V^+ = 20 V

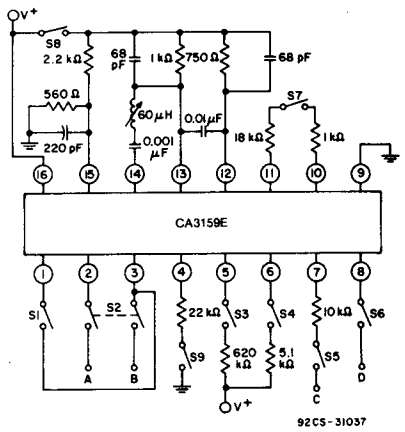
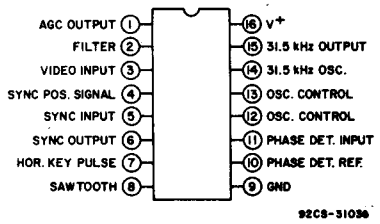


Fig. 2 – DC test circuit.

CA3159E
TERMINAL ASSIGNMENT



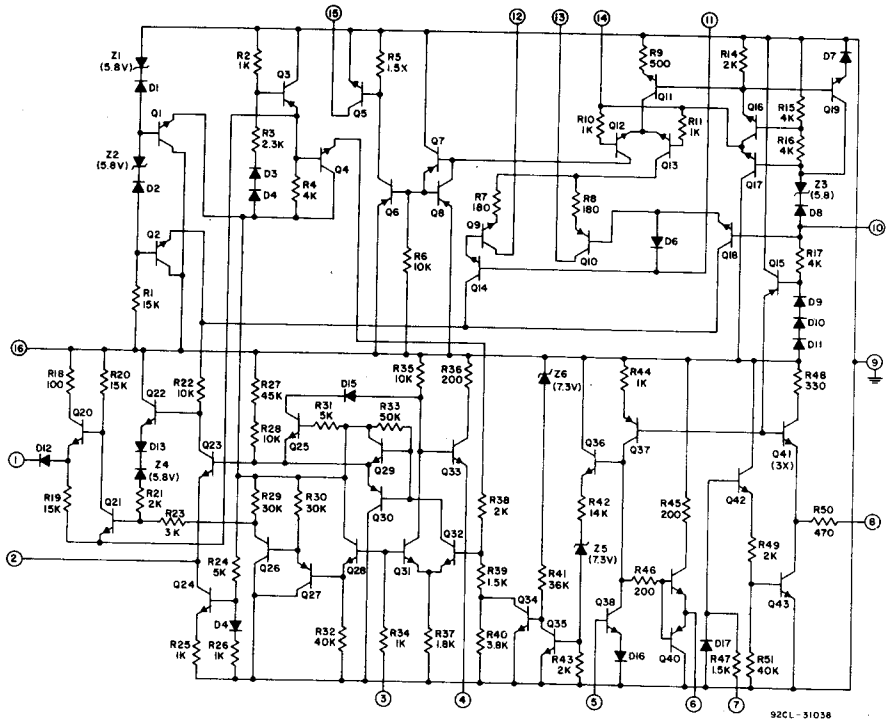


Fig. 3 — Schematic diagram of the CA3159E.

Circuit Description

The negative sync video input at terminal 3 is the detected video if. This video signal is buffered and V_{be} compensated by emitter-followers Q28, Q27, and Q26. The buffered video signal is applied between the base of Q21 and a temperature-stable 2-V reference. Q21 is normally in saturation, and the negative sync pulse imparts a positive swing to the base of Q20. Q20 is used as a peak rectifier driving a capacitor at terminal 1. The voltage at terminal 1 is the AGC control voltage that sets the if gain such that the sync pulses drop to just below the 2 V level, driving Q21 out of saturation.

The above description is for a normal video signal; the presence of noise pulses more negative than the sync tip level would lower the gain to that level, thus disturbing the picture. A gated noise-inversion threshold is provide at the base of Q32 to compensate for these noise pulses. The threshold is about 1.5 V during trace time, but is reduced to about 1 V during coincidence of the sync and flyback pulses. When the video signal is more negative than the noise threshold, Q32 conducts and pulls the base and emitter of Q30 low. Without noise, Q23 conducts 0.5 mA with its collector at 7 V, which holds Q22 in cutoff. Q23 has an emitter load provided by an external 1 kΩ resistor and a series capacitor: when its base is switched low, its collector switches high. The resulting flow of current in Q23 overrides the normal negative-going pulse in the direct signal path and holds Q21 in saturation.

The video input to terminal 3 also operates the sync channel, beginning with Q31. Because Q32 is normally cut off, Q31 acts as an amplifer with a moderate gain to its collector, and a positive sync signal appears at terminal 4. If the noise pulse is more negative than the noise threshold at the base of Q32, the base of Q30 is pulled down as discussed above. In addition to operating the AGC noise inverter, the Q30 current passes through Q25 to the amplifier load resistor, R35, and cancels the potentially positive pulse at that point.

The positive sync signal at terminal 4 is coupled through an RC network to terminal 5 for sync separation. In essence, the network permits Q38 to clamp the positive peaks, so the most positive part of the signal is amplified by Q38 while the rest is beyond cutoff. The separated sync, a negative pulse at the collector of Q38, follows two paths. First, the sync operates an output driver to terminal

CIRCUIT DESCRIPTION (cont'd)

6, which drives the outboard diode phase detector. Second, the negative pulse cuts off the current through Q36, which otherwise holds Q35 in saturation, thus enabling a current in R41 to turn Q34 on and thereby shift the noise threshold voltage.

Terminal 7 receives a positive flyback pulse that supplies R41 with the signal to complete the coincidence gate that alters the noise threshold when sync and flyback pulses are in phase. The buffered and clipped flyback pulse also turns Q43 on, which, in conjunction with an external integrating capacitor, forms a sawtooth waveform. This sawtooth (at flyback rate) is phase compared with the sync pulse that was separated from the video input.

The phase detector works against an internal bias point brought out to terminal 10, and the phase detector output applied to terminal 11 is slightly positive or negative relative to terminal 10. This voltage differential with terminal 10 determines the division of current between Q9 and Q10, which are part of the voltage controlled oscillator. The oscillator consists of the current source Q11, differential amplifier Q12 and Q13, and differential amplifier Q9 and Q10. The frequency is determined primarily by a series LC circuit connected between terminals 13 and 14 (terminals 12 and 13 have resistor loads to the positive supply). If the entire oscillator current passes through Q10 to terminal 13, the oscillator operates at the frequency at which the phase shift in the LC circuit is zero. If the current is sent through Q9 to terminal 12, however, it must go through an external capacitor between terminals 12 and 13 and then through the original LC circuit and the circuit is tuned differently. Intermediate proportions of current division will produce intermediate oscillator frequencies. The oscillator current output from Q12 provides base drive for the 31.5 kHz output at terminal 15.