

April 1994

Quad-Gated Inverting Power Drivers

Features

- Independent Over-Current Limiting on Each Output
- Independent Over-Temperature Limiting On Each Output
- Output Drivers Capable of Switching 700mA Load
- Inputs Compatible With TTL or 5V CMOS Logic
- Suitable For Resistive, Lamp or Inductive Loads
- Power-Frame Construction for Good Heat Dissipation
- Operational Temperature Ranges
 - CA3262A -40°C to +125°C
 - CA3262 -40°C to +85°C

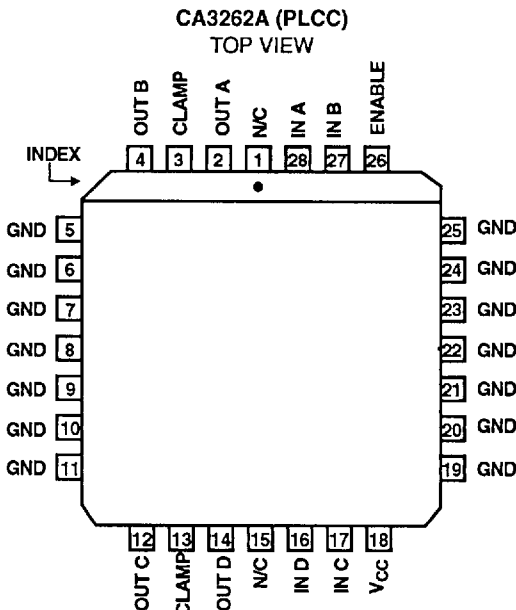
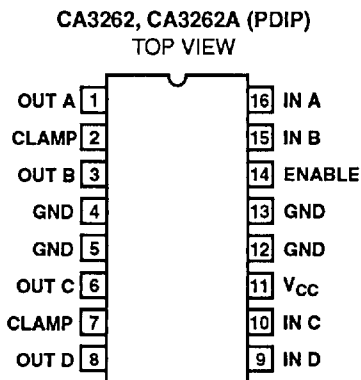
Applications

- Solenoid
- Relay
- Light
- Steppers
- Motors
- Displays

System Applications

- Automotive
- Appliance
- Industrial Control
- Robotics

Pinouts



Description

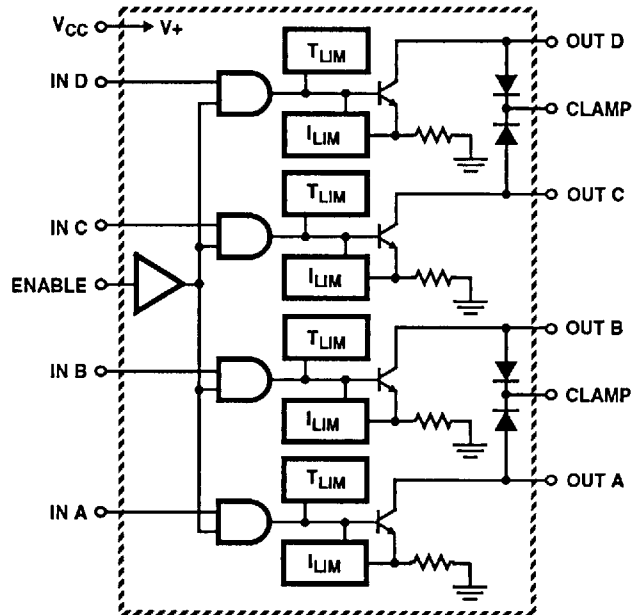
The CA3262 and CA3262A are used to interface low-level logic to high current loads. Each Power Driver has four inverting switches consisting of a non-inverting logic input stage and an inverting low-side driver output stage. All input stages have a common enable input. Each output device has independent current limiting (I_{LIM}) and thermal limiting (T_{LIM}) for protection from overload conditions. Steering diodes connected from each output (in pairs) to the Clamp pins may be used in conjunction with external zener diodes to protect the IC against overvoltage transients that result from inductive load switching. To allow for maximum heat transfer from the chip, all ground pins on the DIP and PLCC package are directly connected to the mounting pad of the chip. An integral heat spreading lead frame directly connects the bond pad and ground leads for good heat dissipation.

The CA3262 and CA3262A can drive four incandescent lamp loads without modulating their brilliance when the "cold" lamps are energized. Outputs may be parallel connected to drive high current loads. The maximum output current of each output is determined by the over-current limiting threshold which is typically 1.2A but may be as low as 0.7A.

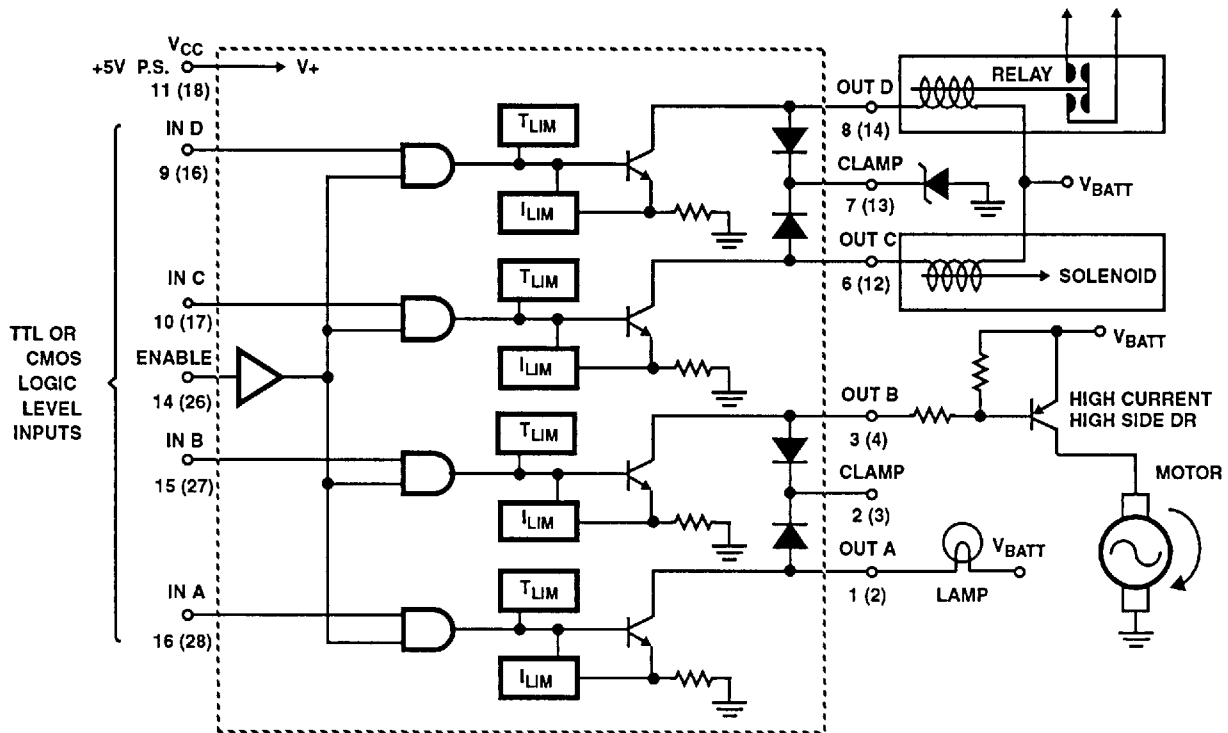
Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA3262E	-40°C to +85°C	16 Lead Plastic DIP
CA3262AE	-40°C to +125°C	16 Lead Plastic DIP
CA3262AQ	-40°C to +125°C	28 Lead PLCC

Functional Block Diagram



CA3262A, CA3262



TRUTH TABLE (Each Output)

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

PINS 4, 5, 12 & 13 GROUND (PACKAGE E)
 PINS 5-11 & 19-25 GROUND (PACKAGE Q)
 PIN #'S IN PARENTHESIS APPLY TO PACKAGE Q

FIGURE 1. QUAD INVERTING POWER DRIVER (QDR) SHOWN WITH TYPICAL APPLICATION LOADS

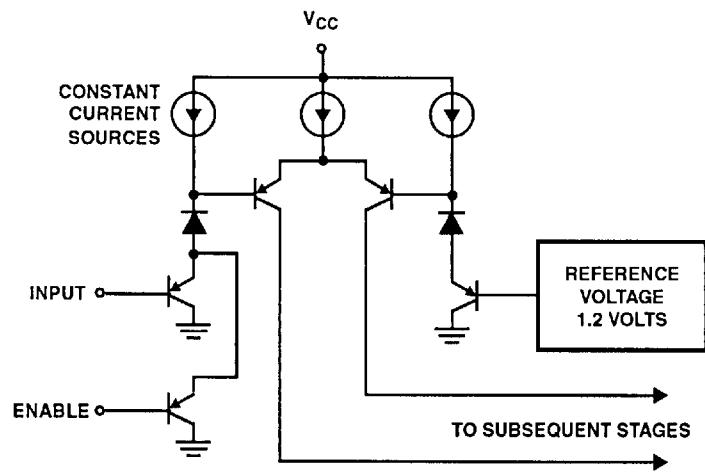


FIGURE 2. CA3262A EQUIVALENT SCHEMATIC OF ONE INPUT STAGE

Specifications CA3262A, CA3262

Absolute Maximum Ratings

Logic Supply Voltage, V_{CC}	7.0V
Logic Input Voltage, V_{IN}	15V
Output Voltage, V_{CEX}	60V
Output Sustaining Voltage, $V_{CE(SUS)}$	40V
Output Transient Current	(Note 1)
Output Load Current	(Note 2)
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
CA3262AE, CA3262AQ	-40°C to +125°C
CA3262E	-40°C to +85°C

Thermal Information

Thermal Resistance (Note 3)	θ_{JA}
CA3262AQ	45°C/W
CA3262E, CA3262AE	60°C/W
Power Dissipation, P_D	
CA3262E, CA3262AE	
Up to +60°C (Free Air)	1.5W
Above +60°C	Derate Linearly at 16.6mW/°C
Up to +90°C With Heat Sink (PC Board)	1.5W
Above +90°C;	
With Heat Sink (PC Board)	Derate Linearly at 25mW/°C
CA3262AQ	
Up to +85°C (Free Air)	1.5W
Above +85°C	Derate Linearly at 23mW/°C
Up to +105°C with Heat Sink (PC Board)	1.5W
Above +105°C;	
With Heat Sink (PC Board)	Derate Linearly at 33mW/°C
Maximum Junction Temperature	+150°C
Lead Temperature (Soldering 10s)	+265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{CC} = 5.5V$, $T_A = -40^\circ C$ to $+125^\circ C$ for CA3262A and $V_{CC} = 5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$ for CA3262 Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current	I_{CEX}	$V_{CE} = 60V$, $V_{ENABLE} = 0.8V$	-	-	100	-	0.6	50	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	Note 4	40	-	-	40	-	-	V
Collector Emitter Saturation Voltage (See Figures 4B & 5B)	$V_{CE(SAT)}$	$V_{IN} = 2V$, $V_{CC} = 4.75V$							
		$I_C = 100mA$	-	-	0.25	-	0.05	0.15	V
		$I_C = 200mA$	-	-	-	-	-	0.2	V
		$I_C = 300mA$	-	-	-	-	-	0.25	V
		$I_C = 400mA$	-	-	0.4	-	0.2	0.3	V
		$I_C = 500mA$	-	-	-	-	-	0.4	V
		$I_C = 600mA$	-	-	0.6	-	-	0.5	V
		$I_C = 700mA$, $T_A = -40^\circ C$	-	-	0.6	-	-	0.5	V
Input Low Voltage	V_{IL}		-	-	0.8	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	2	-	-	V
Input Low Current	I_{IL}	$V_{IN} = 0.8V$	-	-	10	-	0.75	10	μA
Input High Current	I_{IH}	$V_{IN} = V_{ENABLE} = 5.5V$, $I_C = 600mA$	-	-	10	-	-	10	μA
Supply Current, All Outputs ON, (See Figures 4A and 5A)	$I_{CC(ON)}$	$V_{IN} = 2V$, $V_{ENABLE} = 5.5V$, $I_{OUTA} = 250mA$, $I_{OUTB} = 250mA$, $I_{OUTC} = 250mA$, $I_{OUTD} = 250mA$	-	-	70	-	(Note 4)	55	mA
Supply Current, All Outputs OFF, (See Figures 4A and 5A)	$I_{CC(OFF)}$	$V_{IN} = 0V$	-	-	5	-	(Note 4)	5	mA
Clamp Diode Leakage Current	I_R	$V_R = 60V$	-	-	100	-	-	50	μA
Clamp Diode Forward Voltage, (See Figures 4D and 5D)	V_F	$I_F = 1A$, $V_{IN} = 0V$	-	-	1.7	-	-	1.7	V
		$I_F = 1.5A$, $V_{IN} = 0V$	-	-	2.1	-	-	2.1	V
Turn-On Delay, (See Figures 4C and 5C)	t_{PHL} , t_{PLH}	$I_{OUT} = 500mA$	-	-	8	-	-	8	μs
Over Current Limiting	I_{LIM}	$V_{OUT} = 2V$, $V_{IN} = 5.5V$, $V_{ENABLE} = 5.5V$	0.7	-	(Note 1)	0.7	-	(Note 1)	A

Specifications CA3262A, CA3262

Electrical Specifications $V_{CC} = 5.5V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$ for CA3262A and $V_{CC} = 5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$ for CA3262
Unless Otherwise Specified (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DESIGN PARAMETERS									
Over Temperature Limiting (Junction Temperature)	T_{LIM}		-	155	-	-	155	-	$^{\circ}C$
Input Capacitance, Input	C_{IN}		-	-	-	-	3	-	pF
Enable Capacitance	C_{EN}		-	-	-	-	4.4	-	pF

NOTES:

- The CA3262 and CA3262A have on-chip limiting for transient peak currents. Under short-circuit conditions with voltage applied to the collector of the output transistor and with the output transistor turned ON, the current will increase to 1.2A, typical. Over-Current Limiting protects a short circuit condition for a normal operating range of output supply voltage. During a short circuit condition, the output driver will shortly thereafter (approx. 5ms) go into Over-Temperature Limiting. While Over-Current Limiting may range to peak currents greater than 2A, each output will typically withstand a direct short circuit up to supply voltage levels of 16V. Excessive dissipation before thermal limiting occurs may cause damage to the chip for supply voltages greater than 18V. The CA3262 and CA3262A are rated to withstand peak current, cold turn-on conditions of #168 or #194 lamp loads.
- The total DC current for the CA3262 and CA3262A with all 4 outputs ON should not exceed the total of $(4 \times 0.7A + \text{Max. } I_{CC}) \sim 2.85A$. This level of current will significantly increase the chip temperature due to increased dissipation and may cause thermal shutdown in high ambient temperature conditions (See Absolute Maximum Ratings for Dissipation). Any one output may be allowed to exceed 0.7A but may be subject to Over-Current Limiting above the I_{LIM} min. limit of 0.7A. As a practical limit, no single output should be loaded to more than 1A max.
- Normal applications require a surface mount of the 28 lead PLCC package on a PC Board. The package has a power lead frame construction where ground pins 5 - 11 and 19 - 25 conduct heat from the frame to the PC Board. With approximately a 2 square inch copper area adjacent to the ground pins, the thermal resistance on the mounted package may be as low as $30^{\circ}C/W$.
- I_{CC} varies with temperature. Typically, $I_{CC(ON)}$ is 18mA at $+125^{\circ}C$ and 41mA at $-40^{\circ}C$. Typically, $I_{CC(OFF)}$ is 2.2mA at $+125^{\circ}C$ and 1.2mA at $-40^{\circ}C$.
- Tested with a switched-off 500mA Load (24Ω series resistance), $V_{BATT} = 12V$ and the outputs (V_{CE}) clamped to +40V maximum with an external zener diode.

Applications

Typical circuit configurations for applying the CA3262 and CA3262A are shown in the application circuit of Figure 1. To their rated capabilities, both circuits can be used to drive inductive, resistive and lamp loads. The CA3262A has a lower V_{SAT} than the CA3262 and is rated for $+125^{\circ}C$ ambient temperature applications. The CA3262 data sheet rating is $+85^{\circ}C$. Otherwise, the protection features described apply to both the CA3262 and CA3262A.

The maximum voltage for full load current switching is the output sustaining voltage, $V_{CE(SUS)}$ which should not exceed 40 Volts. To provide a means of over-voltage protection, on-chip steering diodes are connected from each output to one of two CLAMP pins. Over-voltage pulses may be generated from inductive load switching and must be clamped or limited to a peak voltage less than $V_{CE(SUS)}$. To limit an inductive voltage pulse, a zener diode should be connected to the appropriate CLAMP pin. When the voltage pulse exceeds the zener threshold, the excess energy is dumped to ground via the on-chip steering diode and the external zener diode.

The on-chip diodes may be used in a free-wheeling mode by connecting the CLAMP pins to an external clamp supply voltage. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supplies may be subject to large transient changes; including turn-ON and turn-OFF conditions where non-tracking conditions between supplies could allow forward conduction through the steering diodes. For all transient conditions of either method, the clamp voltage should be greater than the maximum supply voltage of the switching outputs and less than $V_{CE(SUS)}$.

Note that the rate of change of the output current during load switching is fast. Therefore, even small values of inductance, including the inductance of a few meters of hook-up wire to the load circuit, can generate voltage spikes of considerable amplitude at the output terminals and may require clamping to protect the device ratings.

Current-limiting is provided as protection for shorted or overloaded output conditions. Voltage is sampled across a small metal resistor in the emitter of each output stage. When the voltage exceeds a preset comparator level, drive is reduced to the output. Current limiting is sustained unless thermal conditions exceed the preset thermal shutdown temperature of $+155^{\circ}C$.

If an output is shorted, the remaining three outputs will continue to function normally unless the continued heat spreading is sufficient to raise the junction temperature at any other output to a level greater than $+155^{\circ}C$. High ambient temperature conditions may allow this to happen. The degree of interaction is minimized at chip layout design by separating the output devices, each to a separate corner of the chip.

As noted, the thermal resistance values of both the DIP and PLCC packages are improved by direct connection of the leads to the chip mounting pad. In free air, the junction-to-air thermal resistance, θ_{JA} is $+60^{\circ}C/W$ (typical) for the DIP package and $+42^{\circ}C/W$ (typical) for the PLCC package. This coefficient can be lowered to $+40^{\circ}C/W$ and $+30^{\circ}C/W$ respectively by increasing ground copper area on the PC board next to the ground pins of the IC.

CA3262A, CA3262

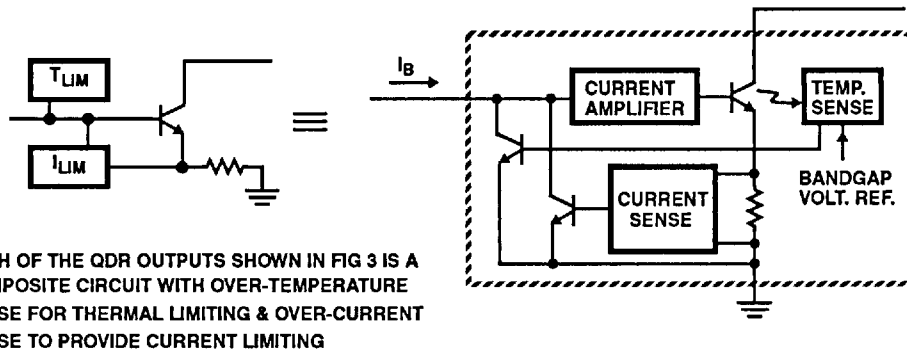


FIGURE 3. QUAD INVERTING POWER DRIVER (QDR) OUTPUT EQUIVALENT CIRCUIT

Typical Performance Curves

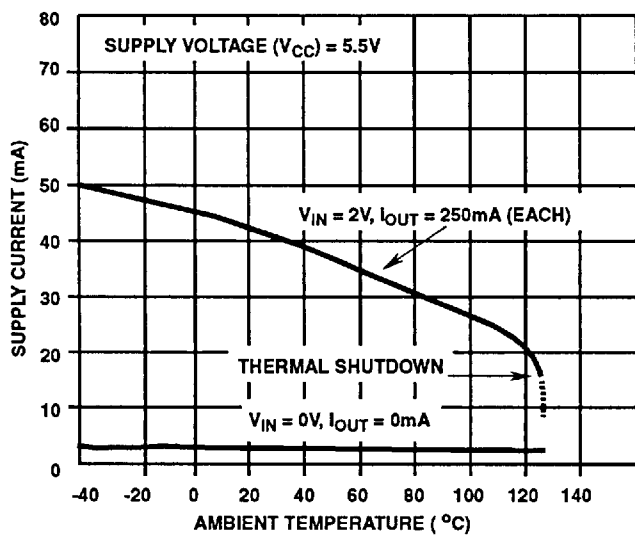


FIGURE 4A. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

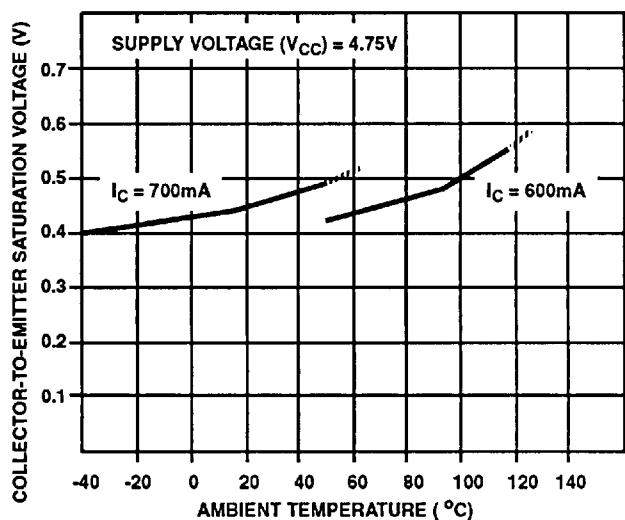


FIGURE 4B. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING POWER DRIVER OUTPUT

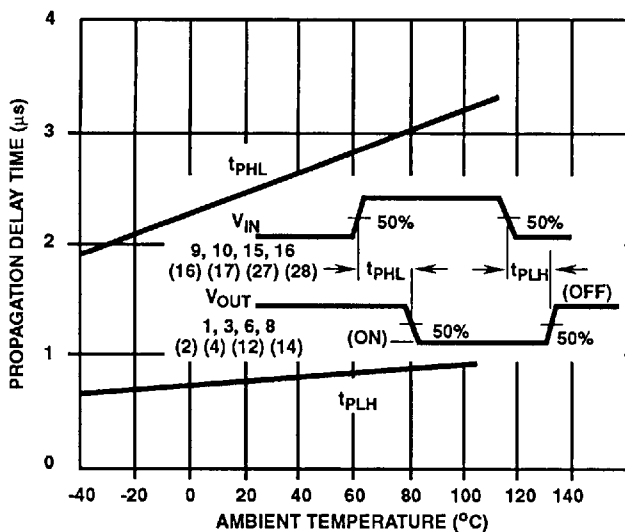


FIGURE 4C. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

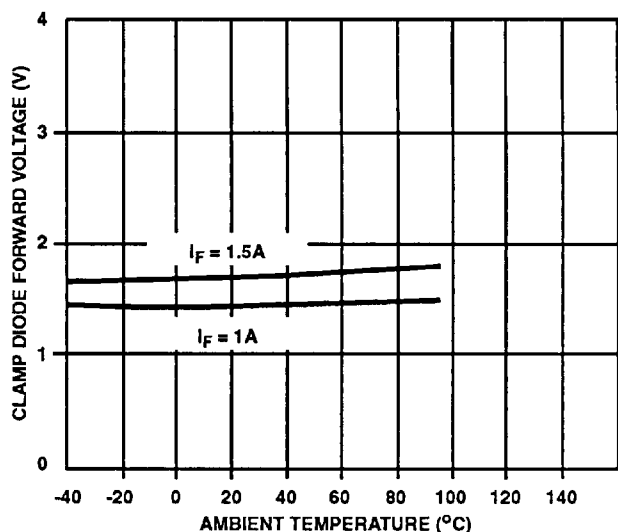


FIGURE 4D. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

FIGURE 4. TYPICAL CHARACTERISTICS OF THE CA3262E

CA3262A, CA3262

Typical Performance Curves (Continued)

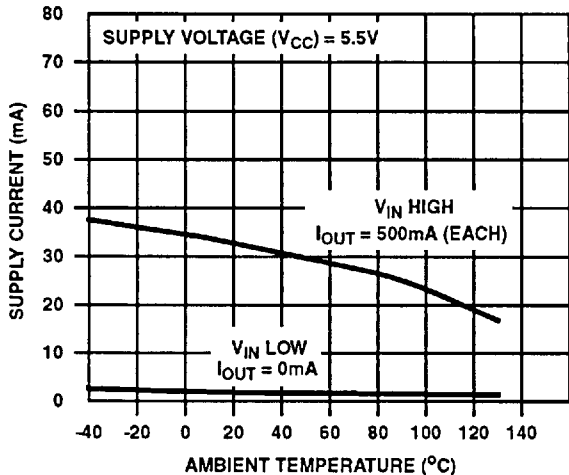


FIGURE 5A. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

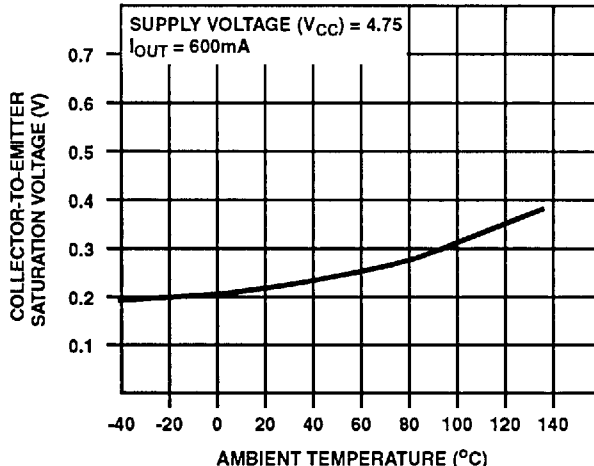


FIGURE 5B. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING-POWER DRIVER OUTPUTS

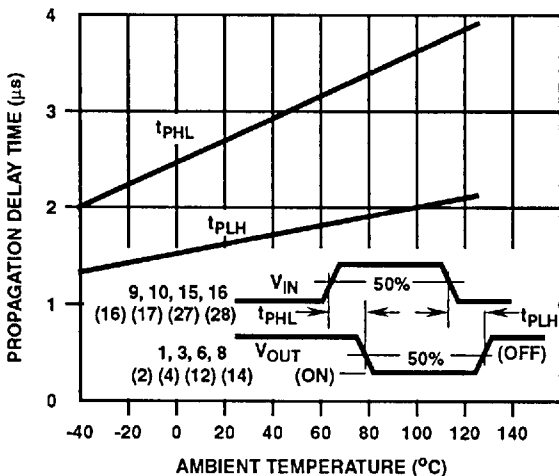


FIGURE 5C. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

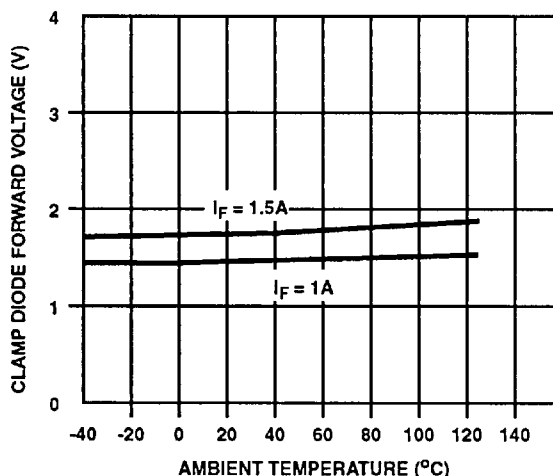


FIGURE 5D. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

FIGURE 5. TYPICAL CHARACTERISTICS OF THE CA3262AE & CA3262AQ

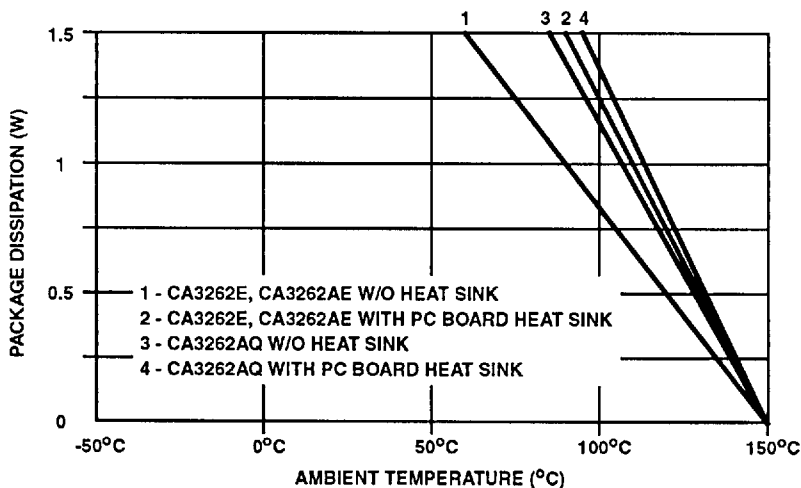


FIGURE 6. PACKAGE DISSIPATION RATING CHART