MICRO NETWORKS

LS/ISO 9001/EN 29001

MN5906

6-Bit, 50MHz CMOS FLASH A/D CONVERTER

FEATURES

- 6-Bit Resolution Plus Overflow Bit
- 50MHz Typical Conversion Rate
- Single +5V Operation
- T/H Not Required
- 50 MHz (min.) Full Power Bandwidth
- Low Input Capacitance
- Low Power (225mW, typ.)
- Small 18-Pin Ceramic or Plastic DIP; Plastic SOIC
- 3-State Outputs
- Optional Environmental Stress Screening
- Compliant MIL-STD-883 Option

DESCRIPTION

The MN5906 is a high-speed, low-power, monolithic CMOS Flash A/D converter. The MN5906 converts at an impressive 50MHz (typ) rate while digitizing analog input signals exceeding several times the Nyquist frequency. The device's pipelined flash architecture contains 64 auto-zeroed comparators, reference resistor ladder, decode logic and output 3-state latches. An intermediate tap is provided for user adjustments of integral linearity.

The converter provides six TTL-compatible output bits plus an overflow flag signal. Overflow can be used in conjunction with 3-state output controls to stack multiple MN5906's for higher resolution applications.

The MN5906 is available for commercial/industrial applications in ceramic side-brazed and plastic DIP packages and plastic SOIC packages for surface-mount applications. Designers of military electronic systems can chose the MN5906CDH/B for an Environmentally Stress Screened device or the MN5906CD/883 for a compliant MIL-STD-883, Non-JAN device.

Model Number	Package	Temperature Range	Mil
MN5906PD	Plastic DIP	0°C to +70°C	No
MN5906PS	Plastic SOIC	0°C to +70°C	No
MN5906CD	Ceramic DIP	0°C to +70°C	No
MN5906PDE	Plastic DIP	-25°C to +85°C	No
MN5906PSE	Plastic SOIC	-25°C to +85°C	No
MN5906CDE	Ceramic DIP	-25°C to +85°C	No
MN5906CDH	Ceramic DIP	-55°C to +125°C	No
MN5906CDH/B	Ceramic DIP	55°C to +125°C	Yes
MN5906CD/883	Ceramic DIP	-55°C to +125°C	Yes

APPLICATIONS

Video
RADAR Systems
Pulse Measurement Systems
Subranging A/D Converters
Synchronous Demodulation
Infrared Imaging
Communications
Flat Panel Displays
Medical Imaging
Disk Drive Read/Write

MICNS002

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April 1993

MN5906 6-Bit, 50MHz CMOS FLASH A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	55°C to +125°C
Specified Temperature Range	
MN5906PD, CD, PS	0°C to +70°C
MN5906PDE, CDE, PSE	25°C to +85°C
MN5906CDH, CDH/B, CD/883	55°C to +125°C
Storage Temperature Range	
MN5906PD, PDE, PS, PSE	65°C to +100°C
MN5906CDE, CDH, CDH/B, CD/883	−65°C to +150°C
Power Supply Voltages ($+V_{DD}$, Pins 5, 6)	−0.5 to +7.0 Volts
Digital Inputs (Pins 3, 4, 18)	−0.5 to $+V_{DD}$ +0.5 Volts
Analog Input (Pin 8)	−0.5 to $+V_{DD}$ +0.5 Volts

ORDERING INFORMATION

PART NUMBER **MN5906 CD H/B**

Select suffix "PD" for plastic DIP
"PS" for plastic SOIC or "CD" for ceramic DIP
Standard "PD", "PS" and "CD" are specified for 0°C to +70°C operation
Add "E" suffix to models for specified −25°C to +85°C operation
Add "H" suffix to "CD" models for specified −55°C to +125°C operation
Add "/B" suffix to "CD" models for Environmental Stress Screening
Add "/883" suffix to "CD" models for MIL-STD-883 compliant, Non-JAN devices

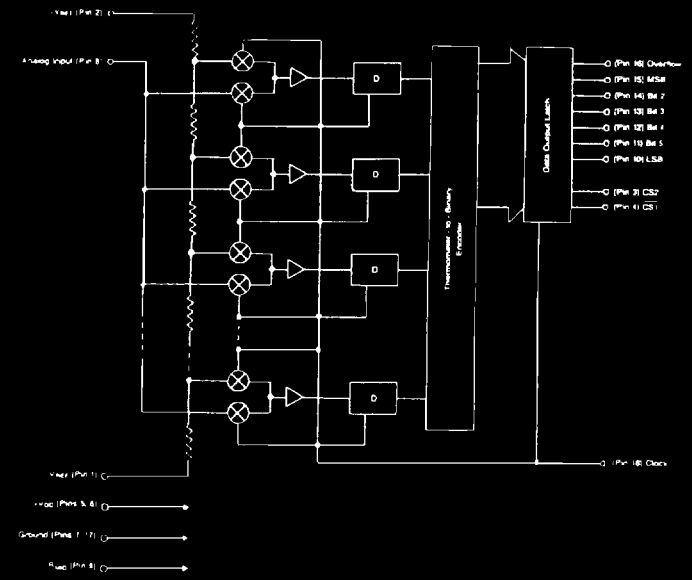
SPECIFICATIONS (T_A = +25°C, Supply Voltage $+V_{DD}$ = +5V, V_{REF} = +2.75V, f_{CLK} = 45 MHz unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		0 to V_{REF}		Volts
Input Capacitance		12		pf
Full Power Bandwidth	50			MHz
REFERENCE INPUTS				
Reference Voltage ($+V_{REF}$)		+2.75		Volts
Reference Ladder Resistance		90		Ω
Reference Ladder Tempco		0.3		Ω/°C
DIGITAL INPUTS				
Logic Levels: Logic "1"	+3.5			Volts
Logic "0"			+1.5	Volts
Logic Loading: Logic "1" (V_{IH} = +4.5V)		+1	+5	μA
Logic "0" (V_{IL} = +0.5V)		−1	−5	μA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (I_{OH} = 4mA)	+4.6			Volts
Logic "0" (I_{OL} = 4mA)			+0.4	Volts
TRANSFER CHARACTERISTICS				
Integral Linearity Error (Notes 1, 2)		± ½	±1	LSB
Differential Linearity Error (Notes 1, 3)		± ¼	± ¾	LSB
DYNAMIC PERFORMANCE				
Conversion Rate	45	50		MHz
Aperture Delay		5		nsec
Output Propagation Delay	8	12	18	nsec
Signal-to-(Noise and Distortion) Ratio (S/N+D)				
f_{AIN} = 1MHz		35		dB
f_{AIN} = 10MHz		33		dB
Spurious Free Dynamic Range (SFDR)				
f_{AIN} = 1MHz		44		dB
f_{AIN} = 10MHz		40		dB
POWER SUPPLY				
Power Supply Voltage ($+V_{DD}$ Supply)	+4.75	+5	+5.25	Volts
Power Supply Current ($+V_{DD}$ Supply)		+45	+50	mA

SPECIFICATION NOTES:

1. Measured while operating at specified conversion rate.
2. Integral Linearity Error is specified using transfer function endpoints (sometimes referred to as endpoint linearity).
3. Differential Linearity Error measurements are based on code transitions.

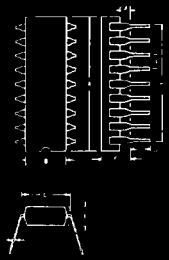
BLOCK DIAGRAM



PACKAGE OUTLINES

Package A
for "PD" devices

	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.845	0.925	21.47	23.49
B	0.240	0.280	6.10	7.11
C	0.300	0.325	7.62	8.25
D	0.008	0.015	0.204	0.381
E	0.115	0.195	2.93	4.95
F	—	0.210	—	5.33
G	0.125	0.200	3.18	5.05
H	0.800 BASIC		20.32 BASIC	
I	0.100 BASIC		2.54 BASIC	
J	0.015	0.060	0.380	1.52

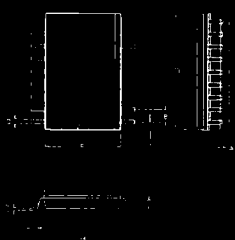


Package B
for all "CD" devices

	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.890	0.910	22.61	23.11
B	0.285	0.305	7.24	7.75
C	0.300	0.320	7.62	8.13
D	0.008	0.015	0.20	0.38
E	—	0.123	—	3.12
F	0.300 BASIC		7.62 BASIC	
G	0.140	0.160	3.56	4.06
H	0.800 BASIC		20.32 BASIC	
I	0.100 BASIC		2.54 BASIC	
J	0.025	0.045	0.64	1.14
K	0.016	0.020	0.41	0.51

Package C
for "PS" devices

	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
b	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.447	0.462	11.35	11.75
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.029		0.74	
L1	0.016	0.050	0.40	1.27



NOTES

Package dimensions conform to JEDEC specification MS-013AB Issue C (MAY 1990)

APPLICATIONS INFORMATION

DESCRIPTION OF OPERATION — The MN5906 CMOS Flash A/D converter operates in a pipelined fashion such that two operations are performed during each phase of the clock. In the first high phase of the clock, the 64 internal comparators are auto-zeroed. During the subsequent low phase of the clock, the analog input signal is sampled by the 64 comparators. The so-called "thermometer code" output of these comparators represents the digitized value of the sampled analog input signal. During the next high phase of the clock, the thermometer code of the "nth" conversion is latched internally and propagates through the internal encoder while the 64 comparators are auto-zeroed for the "n+1" conversion. Valid output data is latched to the digital outputs on the next negative clock transition while the "n+1" sample is taken by the 64 comparators. See the Timing Diagram.

LAYOUT AND GROUNDING CONSIDERATIONS — The MN5906 and other high-speed devices require that careful consideration be given to high-speed and low-noise design techniques. The pinout of the MN5906 has been carefully chosen to maintain as much separation of digital and analog signals as possible. The use of ground and power planes and signal shielding is highly recommended. Bypass capacitors of 0.01 and 0.001μf should be used and located as close to the device as possible.

It is also recommended that circuits interfacing with the MN5906 (such as data latches, etc.) be located within 2 inches of the device to avoid transmission line effects (rise and fall times of the MN5906 output drivers are 2nsec or less implying frequency components in the hundreds of MHz). It is recommended that a high speed amplifier offering low output impedance and high slew rate, such as a current feedback amplifier, should be used to drive the input of the MN5906.

EVALUATION BOARDS — The MN5906 is supported with an evaluation board, the MN5906EVB. This evaluation board embodies the concepts discussed above and is a complete subsystem. The MN5906EVB has an onboard reference, signal gain and offset circuits, and operates from user supplied ± 5V power supplies. The EVB accepts a 1Vp-p bipolar analog input signal and provides both digital (latched from a 74F574) and reconstructed analog (via the onboard D/A converter) output signals.

Please contact the factory for information regarding the MN5906EVB as well as additional applications information regarding the application of high-speed CMOS Flash A/D converters.

PIN DESCRIPTIONS

PIN	NAME	SYMBOL	DESCRIPTION
1, 2	Reference Inputs	$-V_{REF}$, $+V_{REF}$	Bottom and top of the reference resistor string. $-V_{REF}$ normally tied to GND. $+V_{REF}$ normally tied to +2.75 Volts.
3	3-State Control (Overflow and Data Bits)	CS2	Overflow bit valid when CS2 = Logic "1". Output bits and overflow bit in high-impedance state when CS2 = Logic "0". See Truth Table.
4	3-State Control (Data Bits)	$\overline{CS1}$	Data bits valid when $\overline{CS1}$ = Logic "0". Data bits in high-impedance state when $\overline{CS1}$ = Logic "1". $\overline{CS1}$ is a "don't care" (X) when CS2 is a Logic "0". See Truth Table.
5, 6	Power Supply	$+V_{DD}$	Connected to +5V Supply for normal operation.
7	Ground	GND	Connected to System Analog Ground plane.
8	Analog Input	AIN	Connect analog input signal to be digitized. Nominally 0V to $+V_{REF}$.
9	Reference Resistor Midpoint	Mid-R	Midpoint tap to resistor ladder.
10, 11, 12, 13, 14, 15	Data Output Bits	B6-B1	Digital Output Bits.
16	Overflow Bit	OF	Set to a Logic "1" when analog input exceeds $+V_{REF} - ½LSB$.
17	Ground	GND	Connected to System Analog Ground plane.
18	Clock	CLK	Clock Input.

DIGITAL OUTPUT CODING

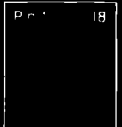
ANALOG INPUT	OF	MSB					LSB
$+V_{REF}$	1	1	1	1	1	1	1
$+V_{REF} - ½LSB$	0	1	1	1	1	1	1
$+V_{REF} - 1LSB$	0	1	1	1	1	1	0
$+V_{REF} - 3/2LSB$	0	1	1	1	1	1	0
$+½V_{REF} + ½LSB$	0	1	0	0	0	0	0
$+½V_{REF} - ½LSB$	0	0	0	0	0	0	0
$+½V_{REF} - 3/2LSB$	0	0	1	1	1	1	0
$+½LSB$	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Analog inputs indicated are the theoretical values for the transitions of codes indicated above. With the converter continuously converting, the output bit indicated as 0 will change from Logic "0" to Logic "1" or vise versa as the input voltage passes through the indicated level.

TRUTH TABLE

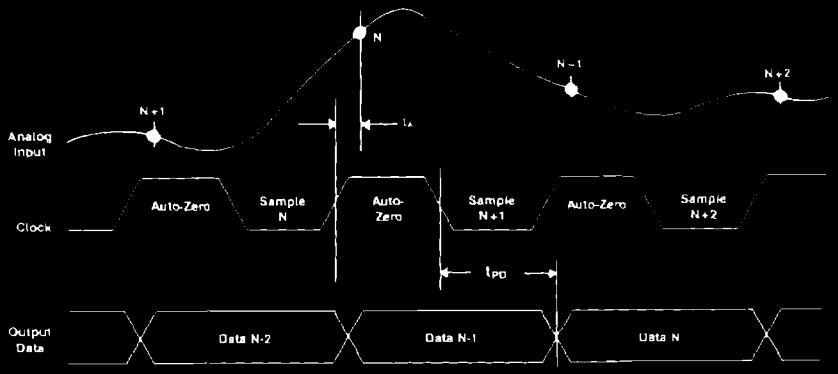
$\overline{CS1}$	CS2	B1 - B6	OF
0	1	Valid	Valid
1	1	High-Z	Valid
X	0	High-Z	High-Z

PIN DESIGNATIONS



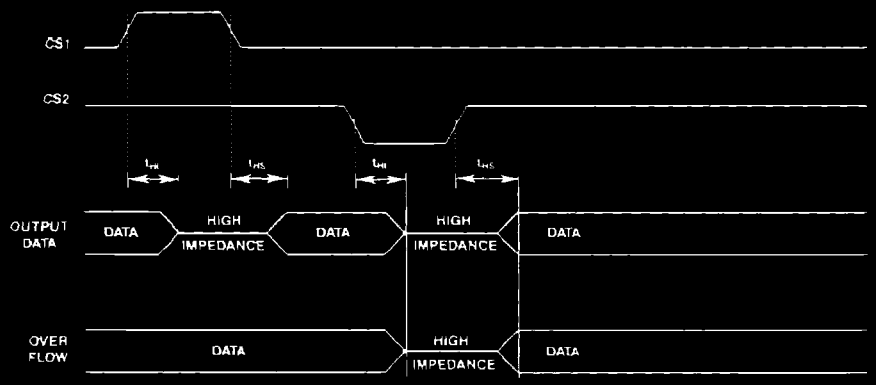
1	$-V_{REF}$	18	Clock Input
2	$+V_{REF}$	17	Ground
3	3-State Control (CS2)	16	Overflow
4	3-State Control ($\overline{CS1}$)	15	Bit 1 (MSB)
5	$+V_{DD}$ Supply	14	Bit 2
6	$+V_{DD}$ Supply	13	Bit 3
7	Ground	12	Bit 4
8	Analog Input	11	Bit 5
9	Reference Ladder Midpoint	10	Bit 6 (LSB)

TIMING DIAGRAM



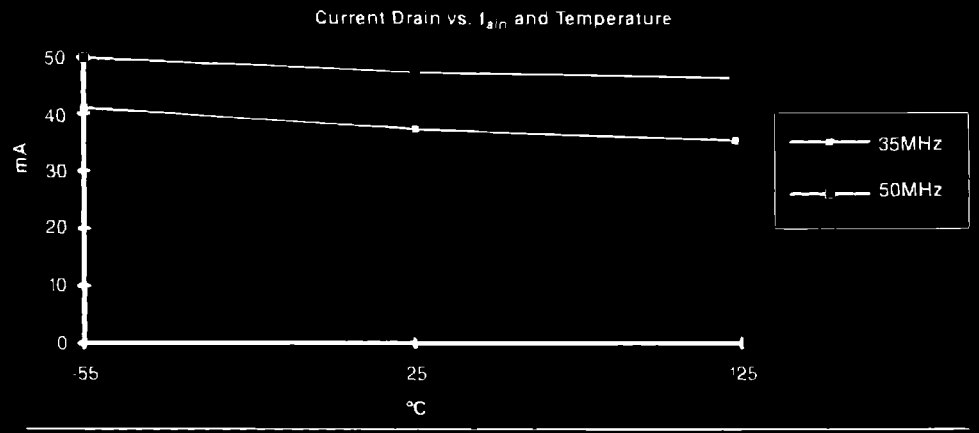
TIMING NOTES:
1. Aperture Delay (t_A) is 5nsec (typ.)
2. Output Propagation Delay (logic) is 25nsec (typ.)

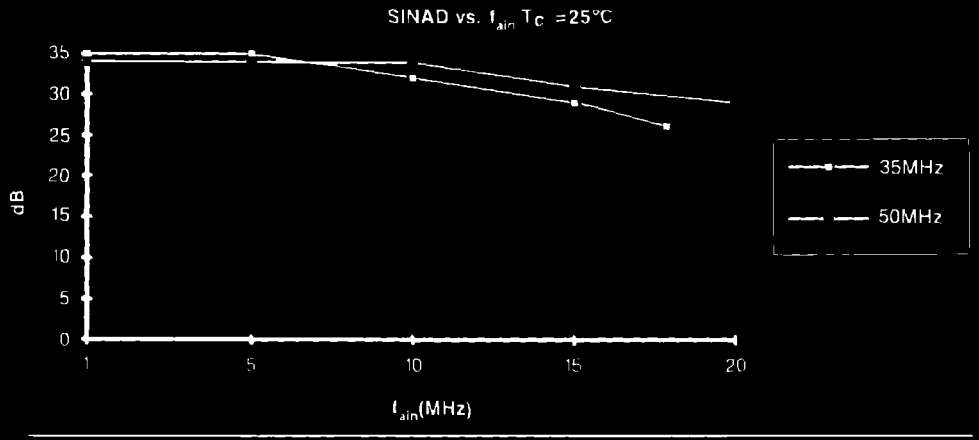
3-STATE TIMING

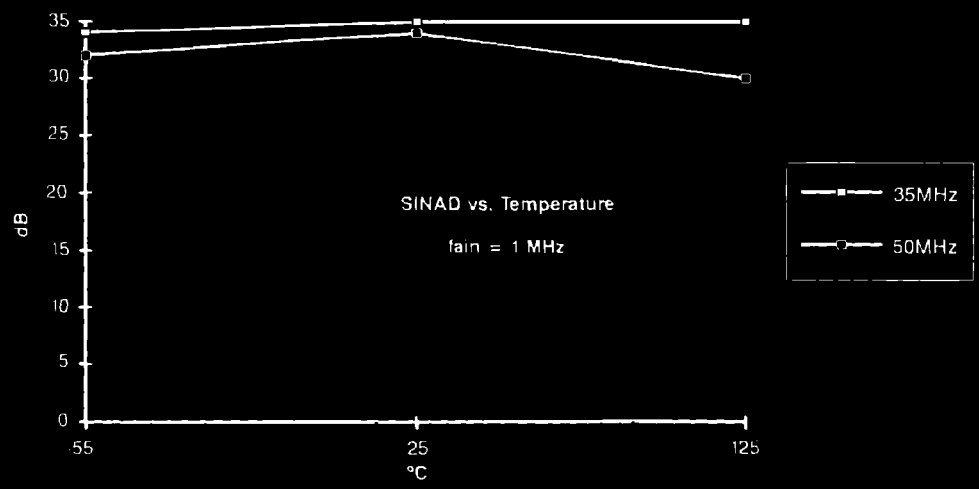


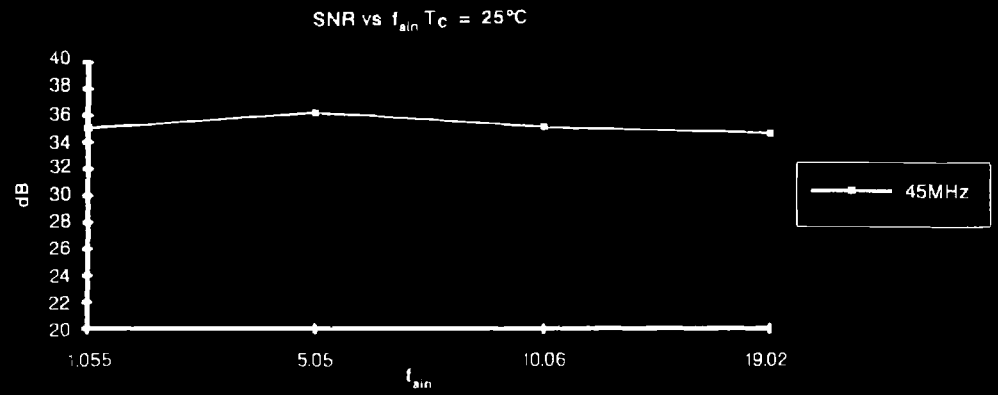
OUTPUT ENABLE TIMING

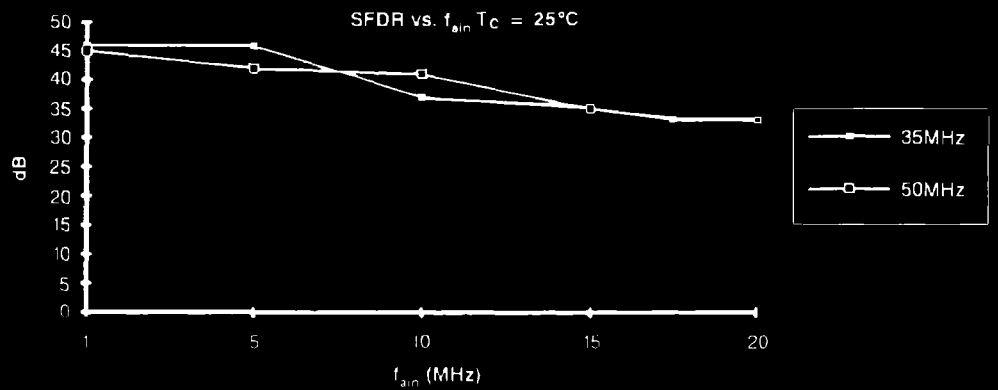
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HL}	Output Float Delay	10	12	15	nsec
t_{HS}	Output Enable	4	7	10	nsec

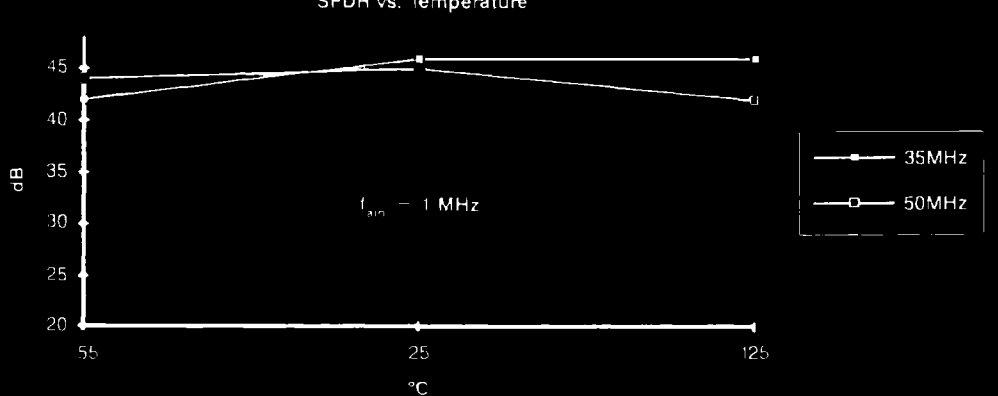

Current Drain vs. f_{ain} and Temperature
50
40
30
20
10
0
mA
-55
25
125
°C
35MHz
50MHz

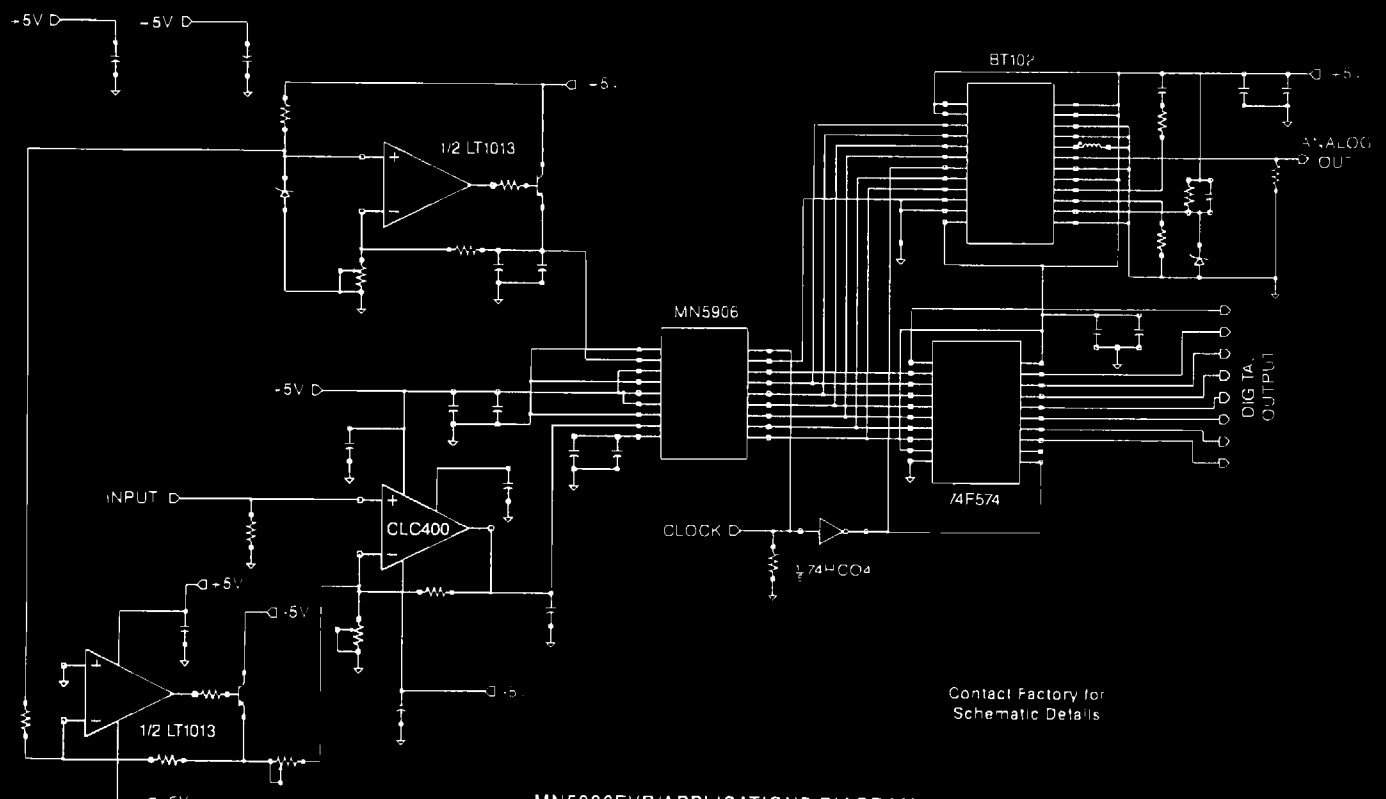

SINAD vs. f_{ain} T_C =25°C
35
30
25
20
15
10
5
0
dB
1
5
10
15
20
f_{ain}(MHz)
35MHz
50MHz


35
30
25
20
15
10
5
0
dB
SINAD vs. Temperature
fain = 1 MHz
-55
25
125
°C
35MHz
50MHz


SNR vs f_{ain} T_C = 25°C
40
38
36
34
32
30
28
26
24
22
20
dB
1.055
5.05
10.06
19.02
f_{ain}
45MHz


SFDR vs. f_{ain} T_C = 25°C
50
45
40
35
30
25
20
15
10
5
0
dB
1
5
10
15
20
f_{ain} (MHz)
35MHz
50MHz


SFDR vs. Temperature
45
40
35
30
25
20
dB
f_{ain} = 1 MHz
55
25
125
°C
35MHz
50MHz



MN5906EVB/APPLICATIONS DIAGRAM