SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B

DESCRIPTION

The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

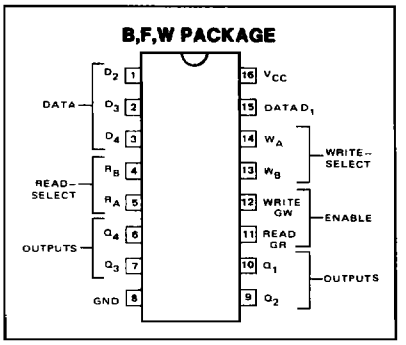
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable of the 54/74LS170 are buffered to lower the drive requirements to one Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

PIN CONFIGURATION



READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

WRITE FUNCTION TABLE

(See Notes A, B, and C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q=D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q=D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q=D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q=D
X	X	H	Q_0	Q_0	Q_0	Q_0

NOTES:

A. H = high level, L = low level, X = irrelevant.

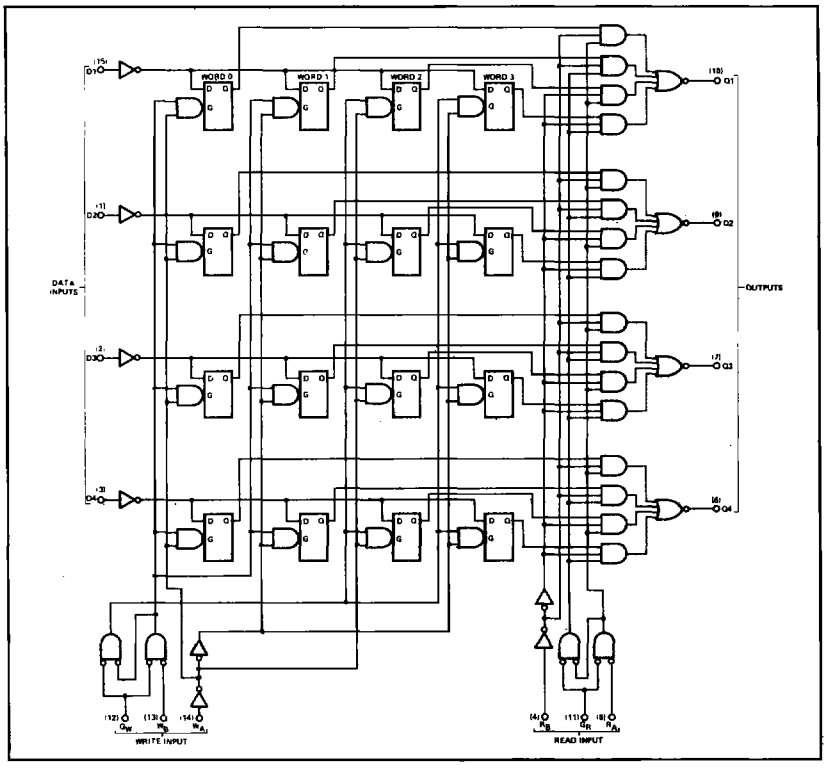
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_0 = The level of Q before the indicated input conditions were established.

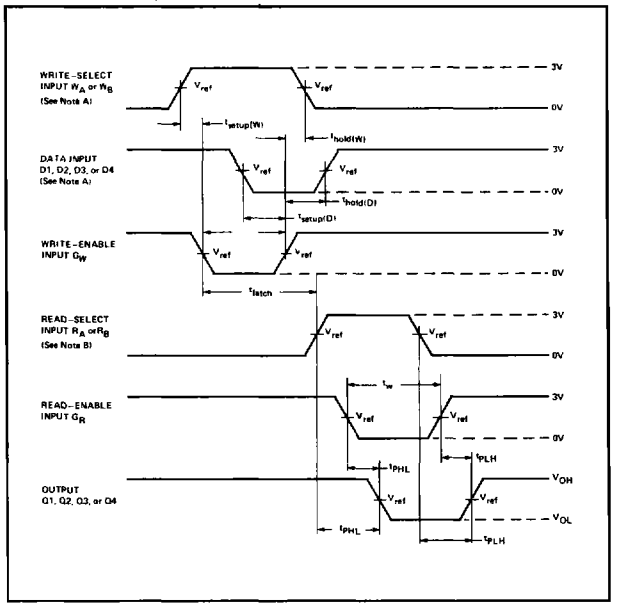
D. W0B1 = The first bit of word 0, etc.

LOGIC

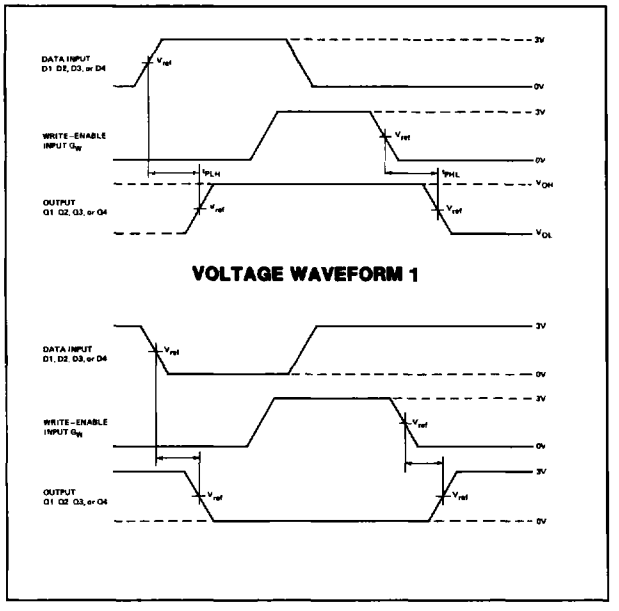
BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
FIGURE 1



VOLTAGE WAVEFORM 1

VOLTAGE WAVEFORM 2
FIGURE 2

NOTES:

A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. In Figure 2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

D. $V_{ref} = 1.3V$.

Load circuits are shown at the front of book (open collector outputs).

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_w Width of pulse			25			25			ns
t_{Setup} Input setup time	Data	Write Enable	10			10			ns
	Write Enable	Write Select	15			15			
t_{Hold} Input hold time	Data	Write Enable	15			15			ns
	Write Enable	Write Select	5			5			
t_{Latch}			25			25			ns
Propagation delay time									
t_{PLH} Low-to-high	Read Enable	Any Q		10	15		20	30	
t_{PHL} High-to-low				20	30		20	30	
t_{PLH} Low-to-high	Read Select	Any Q		23	35		25	40	
t_{PHL} High-to-low				30	40		24	40	
t_{PLH} Low-to-high	Write Enable	Any Q		25	40		30	45	
t_{PHL} High-to-low				34	45		26	40	
t_{PLH} Low-to-high	Data	Any Q		20	30		30	45	
t_{PHL} High-to-low				30	45		22	35	

Load circuit and typical waveforms are shown at the front of section.